Smart Green-Mode PWM Controller with Multiple Protections

REV: 00

General Description

The LD7523 is a low startup current, current mode PWM controller with green-mode power-saving operation. The SOP-8/DIP-8 package integrated functions such as the leading- edge blanking of the current sensing, internal slope compensation, line compensation, and several protection features. The protection functions include cycle-by-cycle current limit, OVP, OLP, and brownout protection. It provides the users a high efficiency, low external component counts solution for AC/DC power applications.

Furthermore, to satisfy various protection requirements, both latch-mode protection and auto-recoverable protection can be easily achieved by configuring LD7523 on different operation modes.

The special green-mode control is not only to achieve the low power consumption but also to offer a non-audible-noise operation when the LD7523 is operating under light load or no load condition.

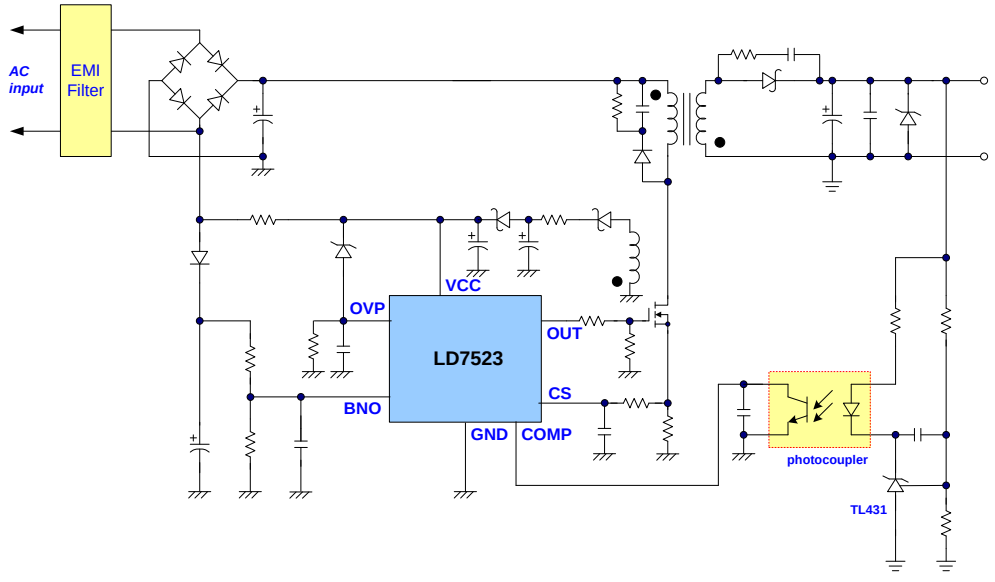
Features

- High-Voltage CMOS Process with Excellent ESD protection
- Very Low Startup Current (< 35μA)
- Current Mode Control
- Non-audible-noise Green Mode Control
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS Pin
- Internal Slope Compensation
- Programmable Line Compensation
- OVP (Over Voltage Protection)
- OLP (Over Load Protection)
- Brownout Protection
- Built in OLP De-Latch Timer
- 500mA Driving Capability

Applications

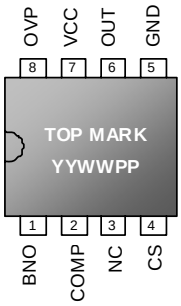
- Switching AC/DC Adaptor and Battery Charger
- Open Frame Switching Power Supply
- LCD Monitor/TV Power

Typical Application



Pin Configuration

SOP-8 & DIP-8(TOP VIEW)



YY : Year code (D: 2004, E: 2005…..)
WW : Week code
: Production code

Ordering Information

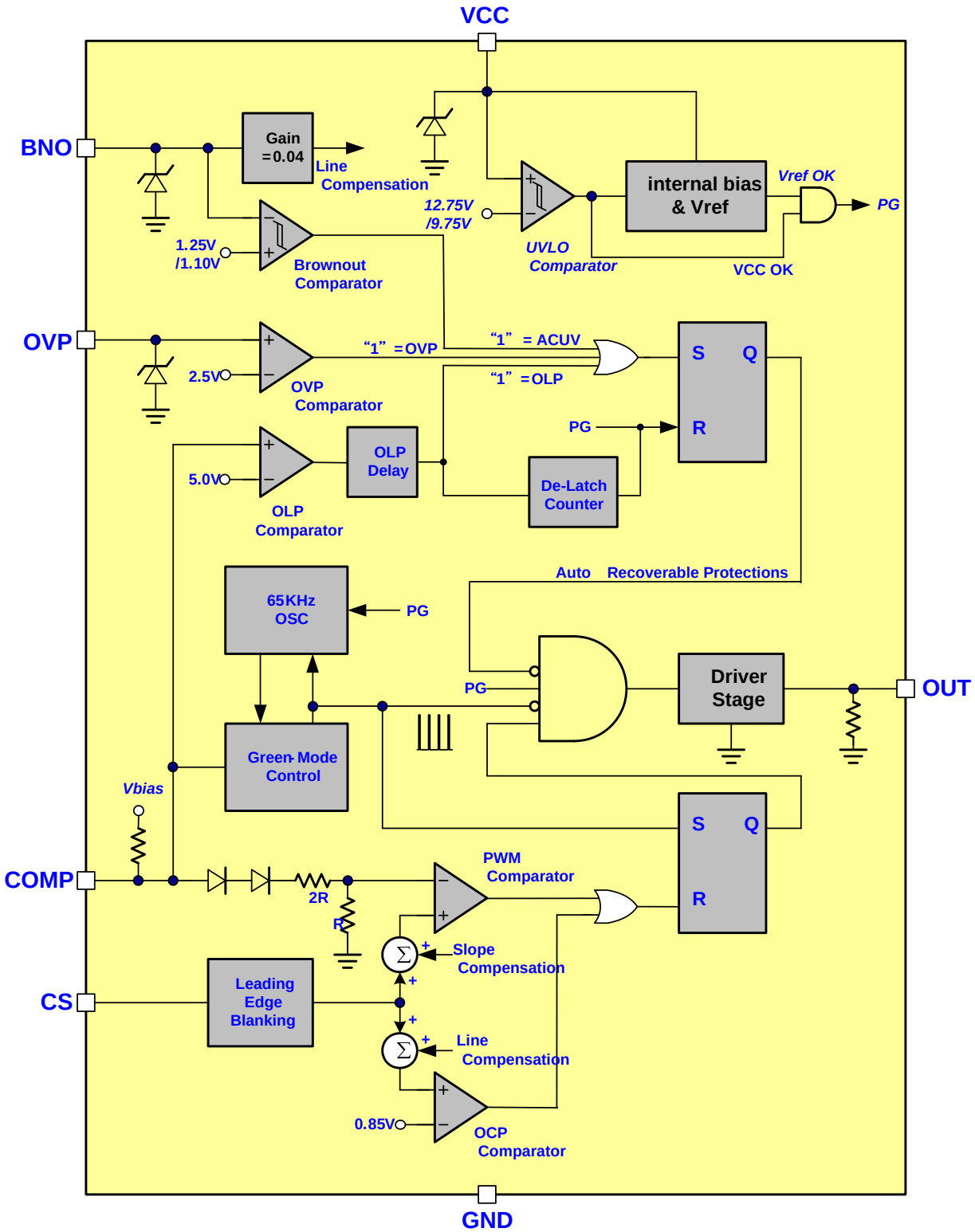
Part number	Package		TOP MARK	Shipping
LD7523 GS	SOP-8	Green Package	LD7523GS	2500 /tape & reel
LD7523 GN	DIP-8	Green Package	LD7523GN	3600/tube /carton

The LD7523 is ROHS Complaint/ Green Package.

Pin Descriptions

PIN	NAME	FUNCTION
1	BNO	Brownout Protection Pin. Connect a resistor divider between this pin and bulk capacitor voltage to set the brownout level and line compensation. When the voltage of this pin fall below threshold voltage, the PWM output will be shut off.
2	COMP	Voltage feedback pin (same as the COMP pin in UC384X). Connect it with a photo-coupler to close the control loop and achieve the regulation.
3	NC	NC
4	CS	Current sense pin, connect to sense the MOSFET current
5	GND	Ground
6	OUT	Gate drive output to drive the external MOSFET
7	VCC	Supply voltage pin
8	OVP	This pin is active-high to provide the OVP function. Connecting a zener or a resistor voltage divider to Vcc will set the OVP level. Once the voltage rise above 2.5V, the OVP will be tripped and the gate drive off. Short this pin to ground to disable the OVP function.

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	-0.3V~30V
COMP, BNO, CS	-0.3V ~7V
OUT	-0.3V ~Vcc+0.3V
Maximum Junction Temperature	150°C
Operating Ambient Temperature Range	-40°C to 85°C
Operating Junction Temperature Range	-40°C to 125°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOP-8)	160°C/W
Package Thermal Resistance (DIP-8)	100°C/W
Power Dissipation (SOP-8, at Ambient Temperature = 85°C)	400mW
Power Dissipation (DIP-8, at Ambient Temperature = 85°C)	650mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model	2.5KV
ESD Voltage Protection, Machine Model	250V
Gate Output Current	500mA

Caution:

Stresses beyond the ratings specified in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=12.0V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (VCC Pin)					
Startup Current			20	35	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=0V		3.5		mA
	V_{COMP}=3V		2.7		mA
	Protection Mode (note 1)		0.70		mA
UVLO (off)		9.0	9.75	10.7	V
UVLO (on)		12.0	12.75	13.5	V
Voltage Feedback (Comp Pin)					
Short Circuit Current	V_{COMP}=0V		2.5	4.0	mA
Green Mode Threshold VCOMP			2.35		V
Current Sensing (CS Pin)					
Maximum Input Voltage, $V_{CS(OFF)}$	V_{BNO}=0V (note 2)	0.80	0.85	0.90	V
	V_{BNO}=1.30V	0.748	0.798	0.848	V
	V_{BNO}=3.75V	0.650	0.700	0.750	V
Leading Edge Blanking Time			350		nS
Input impedance		1		NA	MΩ
Delay to Output			200		nS
Gate Drive Output (OUT Pin)					
Output Low Level	V_{CC}=15V, Io=20mA			1.0	V
Output High Level	V_{CC}=15V, Io=20mA	9.0			V
Rising Time	V_{CC}=15V,Load Cap.=1000pF		50	160	nS
Falling Time	V_{CC}=15V ,Load Cap.=1000pF		30	60	nS
Oscillator					
Frequency		60	65	70	KHz
Green Mode Frequency			20		KHz
Frequency Temp. Stability	(-40°C –85°C)		3		%
Frequency Voltage Stability	(VCC=12V-30V)		1		%

Electrical Characteristics (Continued)

(T_A = +25°C unless otherwise stated, V_{CC}=12.0V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Brownout Protection & Line Compensation (BNO Pin)					
Brownout Turn-On Trip Level		1.20	1.25	1.30	V
Brownout Turn-Off Trip Level		1.05	1.10	1.15	V
Saturation Voltage on LINE Pin	I_{BNO}<1.5uA		5.0		V
Line Compensation Ratio			0.04		V/V
Over Voltage Protection (OVP Pin)					
OVP Trip Level		2.35	2.50	2.65	V
OVP de-bounce time			200		μS
Saturation Voltage on OVP Pin	I_{OVP}<1.5uA		5.0		V
OLP (Over Load Protection)					
OLP Trip Level	$V_{COMP(OLP)}$	4.5	5.0	5.5	V
OLP Delay Time	V_{COMP}>5.0V		60		mS
OLP De-Latch Counter			500		mS
Soft Start					
Soft Start Duration		5	7.5	10	mS

Note 1: When OVP, OLP Protection is tripped.

Note 2: Guaranteed by design because Vcs(off) can't be measured when V_{BNO}=0V.

Typical Performance Characteristics

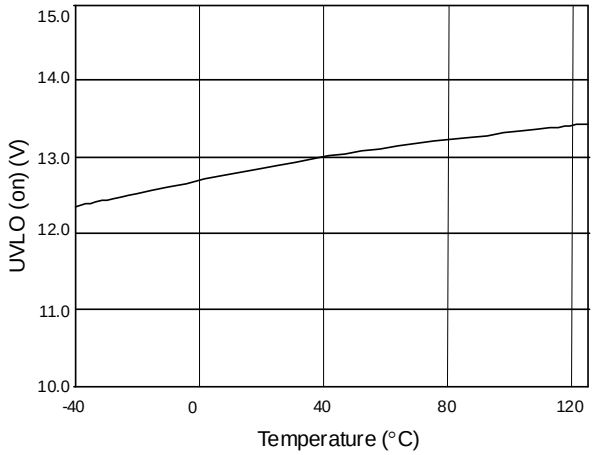


Fig. 1 UVLO (on) vs. Temperature

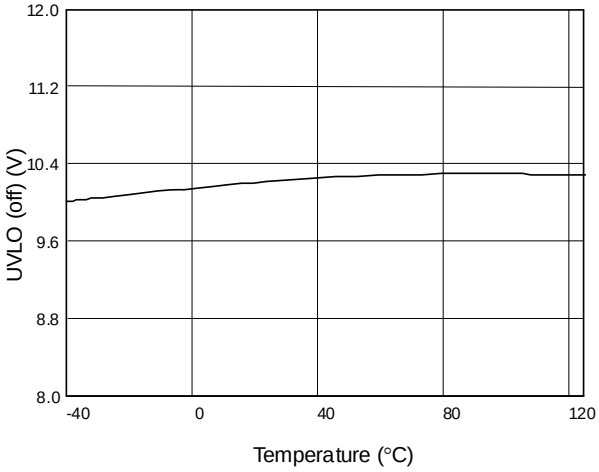


Fig. 2 UVLO (off) vs. Temperature

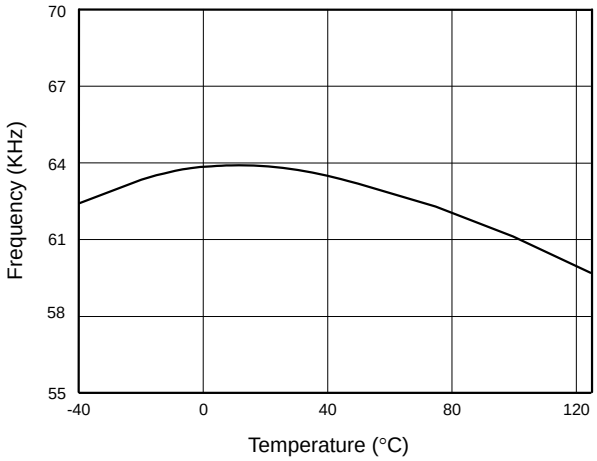


Fig. 3 Frequency vs. Temperature

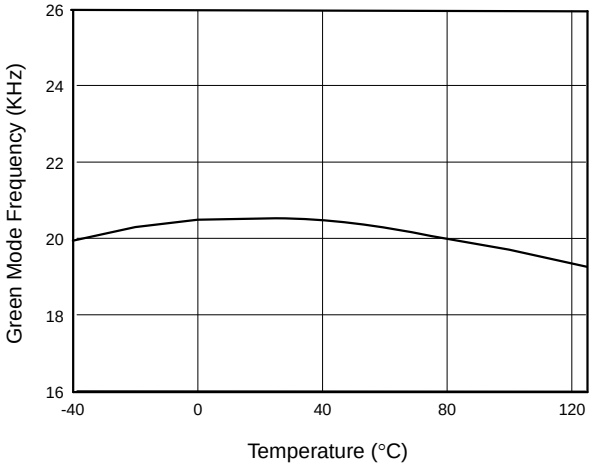


Fig. 4 Green Mode Frequency vs. Temperature

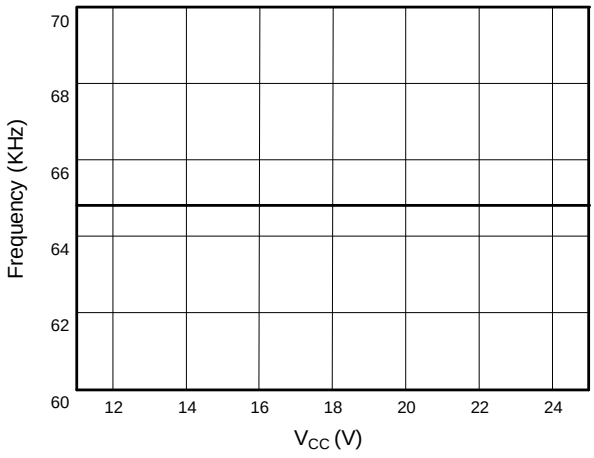


Fig. 5 Frequency vs. V_{CC}

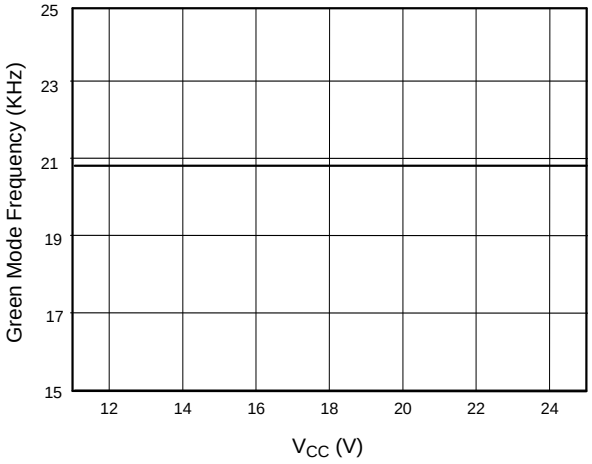


Fig. 6 Green Mode Frequency vs. V_{CC}

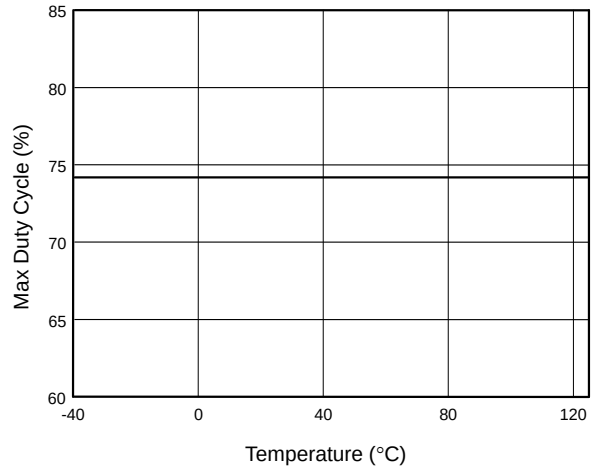


Fig. 7 Max Duty Cycle vs. Temperature

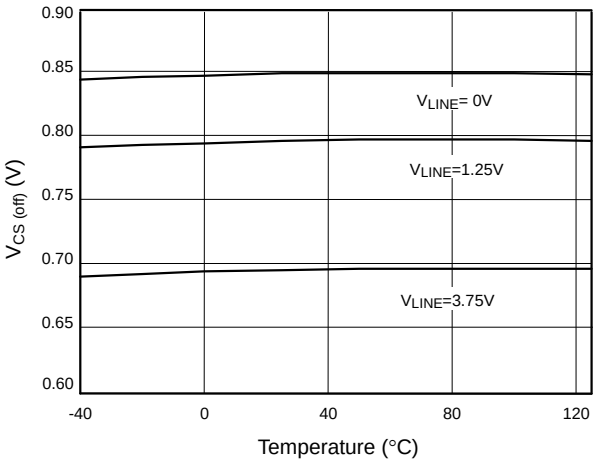


Fig. 8 Vcs (off) vs. Temperature

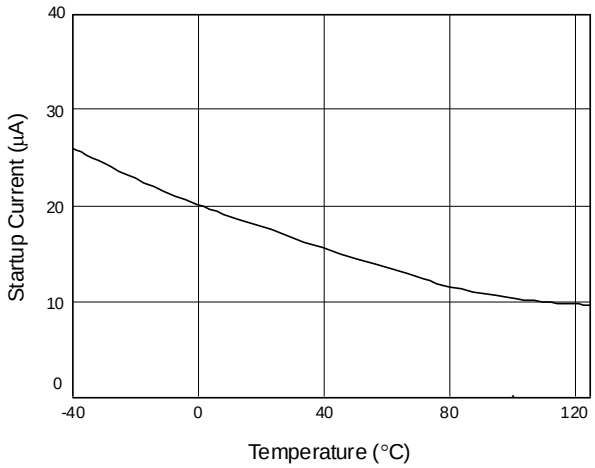


Fig. 9 Startup Current vs. Temperature

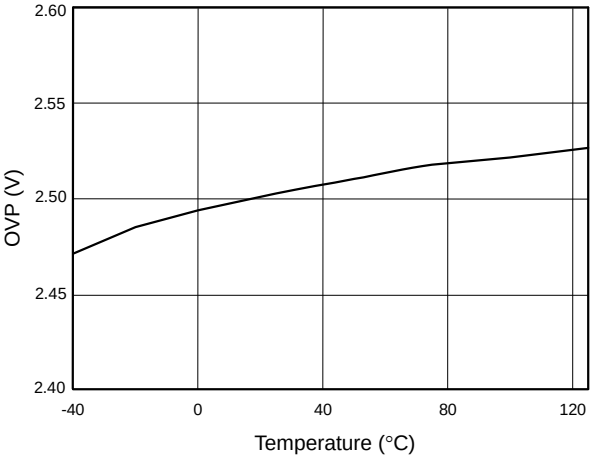


Fig. 10 OVP-Trip Level vs. Temperature

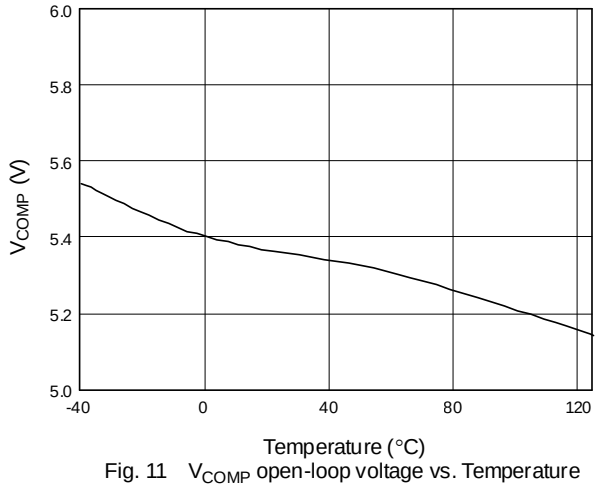


Fig. 11 V_{COMP} open-loop voltage vs. Temperature

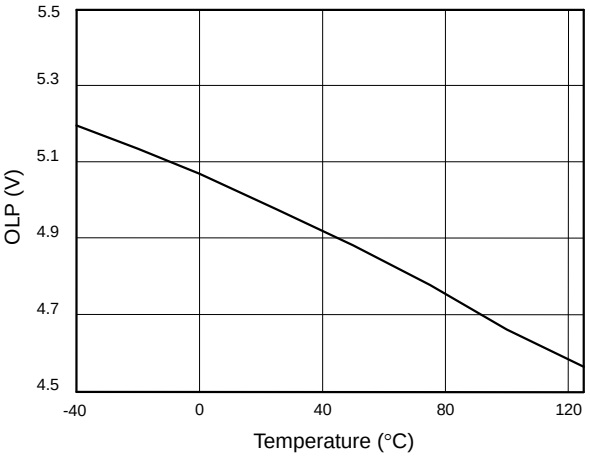


Fig. 12 OLP-Trip Level vs. Temperature

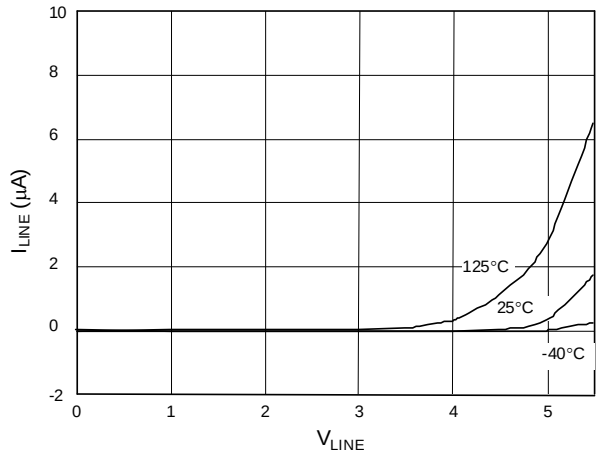


Fig. 13 V_{LINE} vs. I_{LINE}

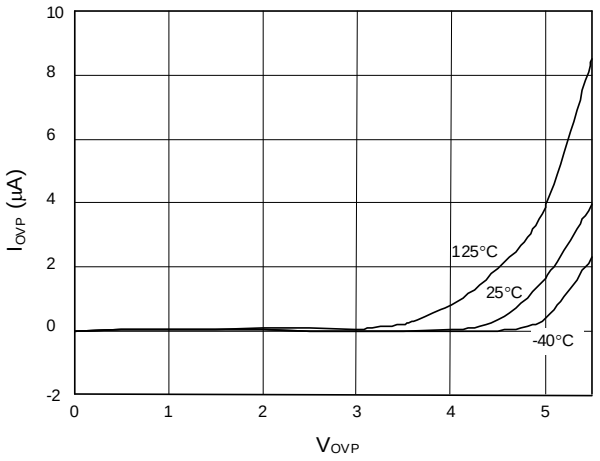


Fig. 14 V_{OVP} vs. I_{OVP}

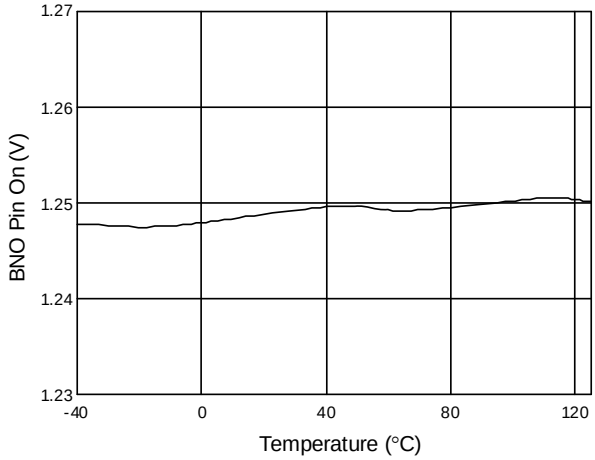


Fig. 15 BNO Pin On Level vs. Temperature

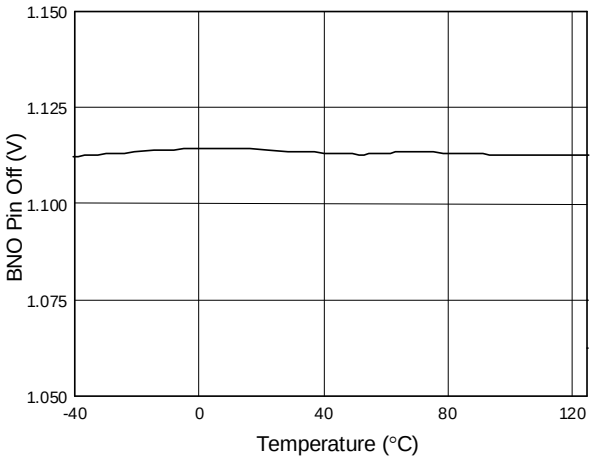


Fig. 16 BNO Pin Off Level vs. Temperature

Application Information

Operation Overview

As long as the green power requirement becomes a trend and the power saving is getting more and more important for the switching power supplies and switching adapters, traditional PWM controllers are not able to support such new requirements. Furthermore, the cost and size limitation forces the PWM controllers to powerfully integrate more functions for reducing the external part counts. The LD7523 is targeted on such applications and provides an easy and cost effective solution; its detailed features are described as below.

Under Voltage Lockout (UVLO)

An UVLO comparator is implemented in it to detect the voltage on the VCC pin, for assuring the supply voltage high enough to turn on the LD7523 PWM controller and to drive the power MOSFET. As shown in Fig. 19, a hysteresis is built in to prevent the shutdown due to the voltage dip during startup. The turn-on and turn-off threshold levels are set at 12.75V and 9.75V, respectively.

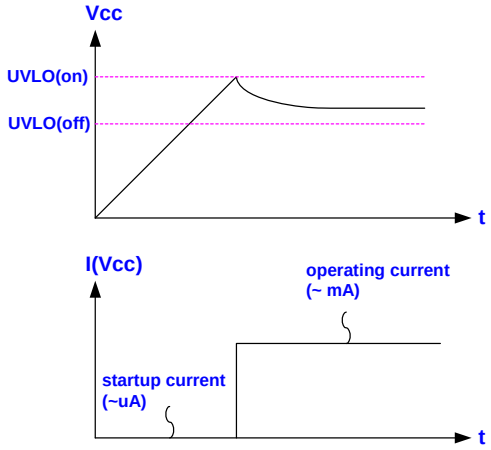


Fig. 19

Startup Current and Startup Circuit

The typical startup circuit for the LD7523 is shown in Fig. 20. During the startup transient, the Vcc is lower than UVLO threshold and thus there is no gate pulse produced from the LD7523 to drive power MOSFET. Therefore, the current through R1 will provide the startup current and to charge the capacitor C1. Once upon the Vcc voltage is high enough to turn on the LD7523 and further to deliver the gate drive signal, the supply current is provided from the auxiliary winding of the transformer. Lower startup current requirement for the PWM controller will help to increase the maximum value on R1 and then reduce the power consumption on R1. By using CMOS process and the special circuit design, the maximum startup current of LD7523 is only 35μA.

If a higher resistance value of the R1 is chosen, it usually takes more time to start up. To carefully select the value of R1 and C1 will optimize the power consumption and startup time.

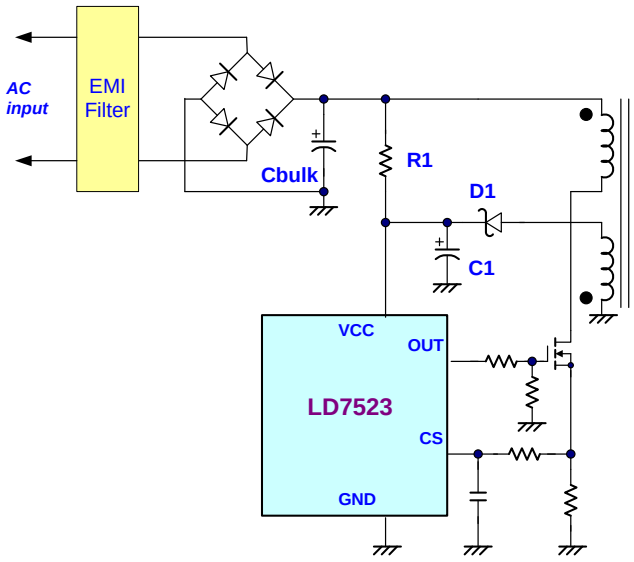


Fig. 20

Output Stage and Maximum Duty-Cycle

An output stage of a CMOS buffer, with typical 500mA driving capability, is incorporated to drive a power

MOSFET directly. And the maximum duty-cycle of LD7523 is limited to 75% to avoid the transformer saturation.

Oscillator and Switching Frequency

The switching frequency of LD7523 is fixed as 65KHz internally to provide the optimized operations by considering the EMI performance, thermal treatment, component sizes and transformer design.

Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 in the secondary side through the photo-coupler to the COMP pin of LD7523. The input stage of LD7523, like the UC384X, has 2 diodes voltage offset before feeding into the voltage divider with 1/3 ratio, that is,

$$V_{+(PWM_{COMPARATOR})} = \frac{1}{3} \times (V_{COMP} - 2V_F)$$

A pulling-high resistor is embedded internally to eliminate the requirement of another resistor in the external circuit.

Dual-Oscillator Green-Mode Operation

There are many different topologies implemented in different chips for the green-mode or power saving requirements, such as “burst-mode control”, “skipping-cycle mode”, “variable off-time control “…etc. The basic operation theory of all these approaches intends to reduce the switching cycles under light-load or no-load condition either by skipping some switching pulses or reduce the switching frequency.

By using this dual-oscillator control, the green-mode frequency can be well controlled and further to avoid the generation of audible noise.

Internal Slope Compensation

A fundamental issue of current mode control is the stability problem when its duty-cycle is over 50%. To stabilize the control loop, slope compensation is required in the traditional UC384X design by injecting the ramp signal from the RT/CT pin through a coupling capacitor. In the LD7523, the internal slope compensation circuit has been internally implemented to simplify the external circuit design.

Current Sensing, Leading-Edge Blanking

The typical current mode PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. The LD7523 detects the primary MOSFET current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set as 0.85V. Thus the MOSFET peak current can be calculated as:

$$I_{PEAK(MAX)} = \frac{(0.85 - V_{LINE\_COMPENSATION})}{R_S}$$

A 350nS leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike. However, the total pulse width of the turn-on spike is decided by the output power, circuit design and PCB layout. It is strongly recommended to adopt a smaller R-C filter (as shown in figure 21) to avoid the CS pin being damaged by the negative turn-on spike.

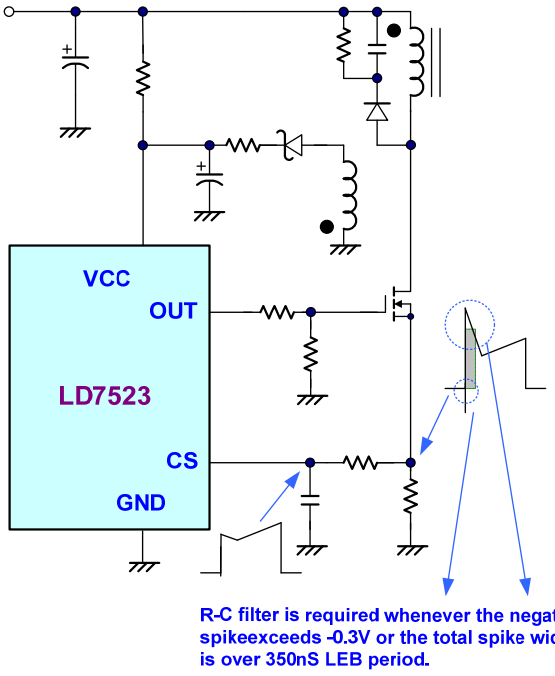


Fig. 21

Brownout Protection & Line Compensation

The LD7523 employs BNO pin to set the brownout protection point and the line voltage OVP point though BNO pin.

The voltage across the BNO pin is proportional to the bulk capacitor voltage, referred as the line voltage. A brownout comparator is implemented to detect the abnormal line condition. As soon as the condition is detected, it will shut down the controller to prevent the damage. Figure 22 shows the operation. When V_{BNO} falls below 1.25V, the gate output will be kept off even Vcc has already achieved UVLO($_{ON}$). It therefore makes Vcc hiccup between UVLO($_{ON}$) and UVLO($_{OFF}$). Unless the line voltage is large enough to pull V_{BNO} larger than 1.25V, the gate output will not start switching even when the next UVLO($_{ON}$) is tripped. A hysteresis is implemented to prevent the false trigger during turn-on and turn-off.

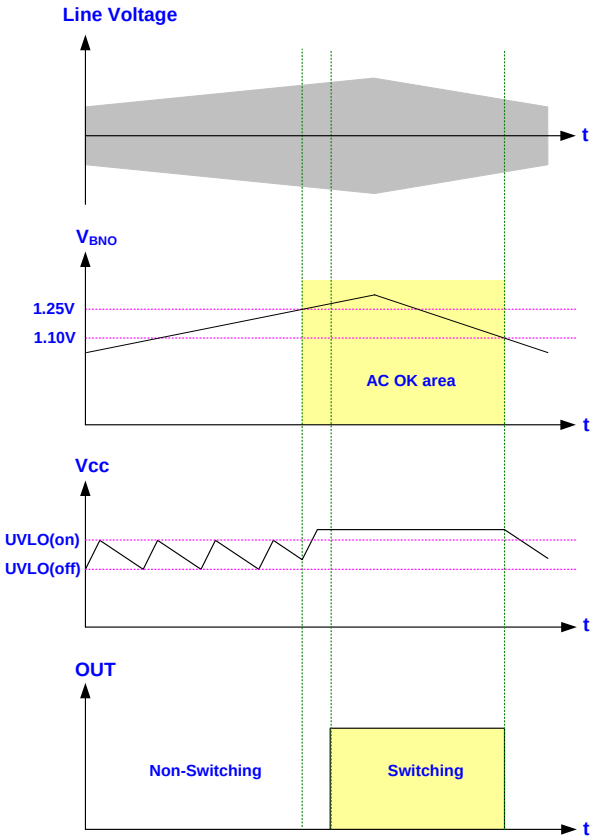


Fig. 22

Meanwhile, LD7523 detects the voltage across BNO pin to feed the line compensation signal to the current sense circuit. Figure 23 shows the circuit. The OCP level of high-line and low-line can be set to a very close point.

The voltage gain from the BNO voltage to line compensation is 0.04 (V/V). The relationship between BNO pin voltage and the line compensation is illustrated in figure 24.

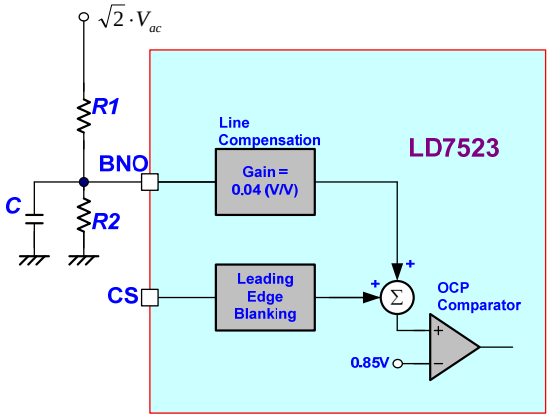


Fig. 23

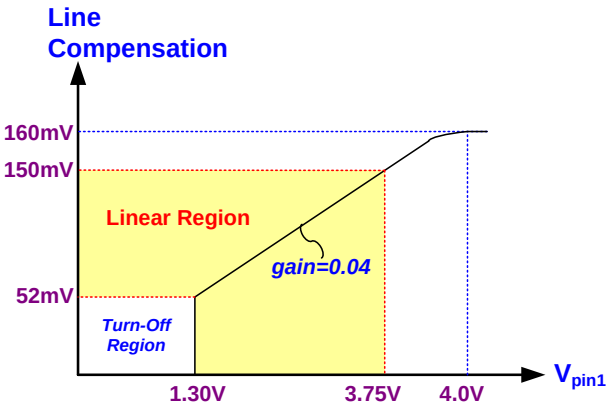


Fig. 24

Over Load Protection (OLP)

To protect the circuit from damage under over load condition or short condition, a smart OLP function is implemented in the LD7523. Figure 25 shows the waveforms of the OLP operation. In such cases, the feedback system will force the feedback voltage loop toward the saturation and pull the voltage of COMP pin (VCOMP) to high. Once the VCOMP trips the OLP threshold of 5.0V and stays for more than 60mS, the protection will be activated and then turns off the gate output to stop the switching of power circuit. The 60mS delay time is to prevent the false trigger from the power-on and turn-off transient.

The Fig. 26 shows the other application example. The VCC of LD7523 will be supplied by an auxiliary source voltage (e.g. standby power) instead. Once the voltage of COMP pin trips the OLP threshold voltage (5.0V) and stays for more than 60mS, OUT pin will stop switching soon. The VCC voltage will not descend since VCC is supplied by an auxiliary voltage source. Otherwise, the internal OLP de-latch counter will active and count for a skipping duration (500mS). It is called as OLP SKIP DURATION. The OUT pin will stop switching until the OLP de-latch counter is reset and then resume to normal switching.

By using such protection mechanism, the average input power can be reduced to minimum level to control the component temperature and stress within the safety operation area.

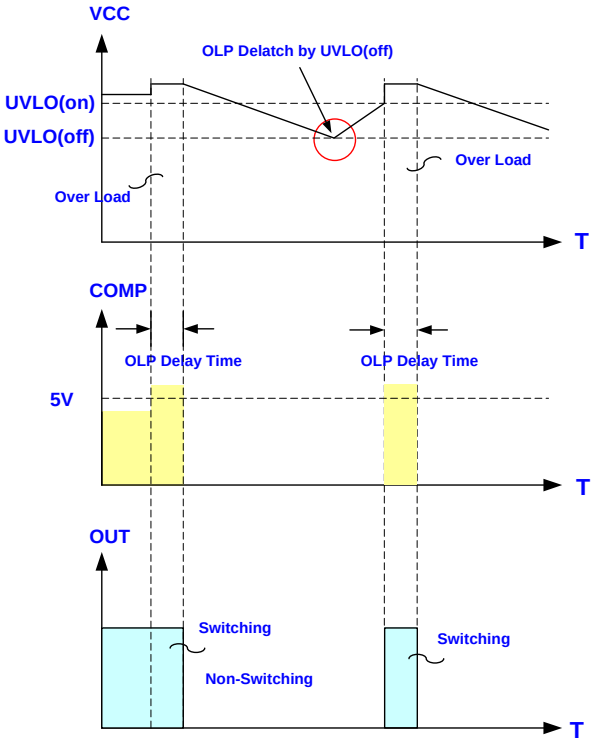


Fig. 25

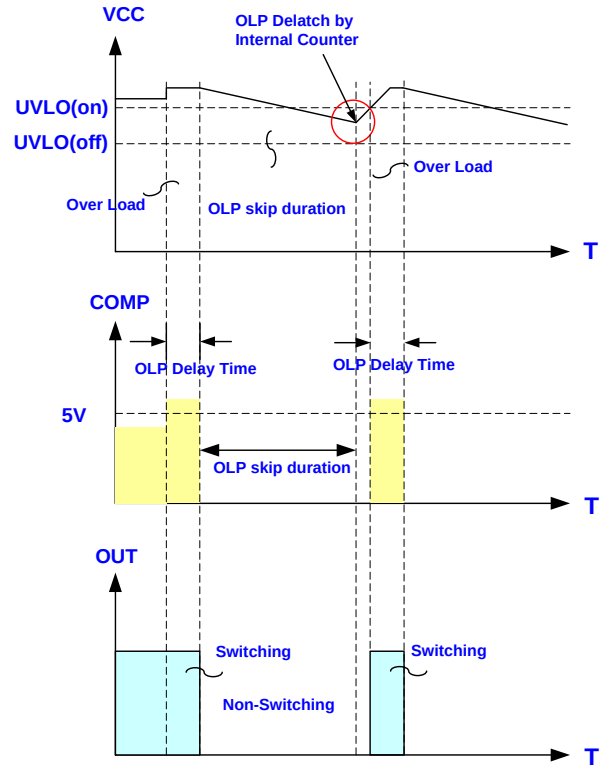


Fig. 26

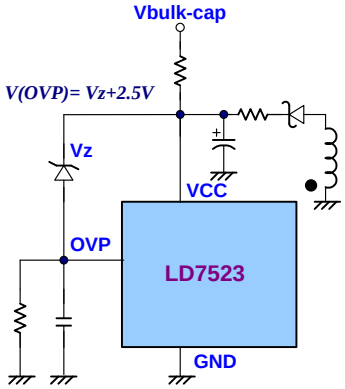


Fig. 27

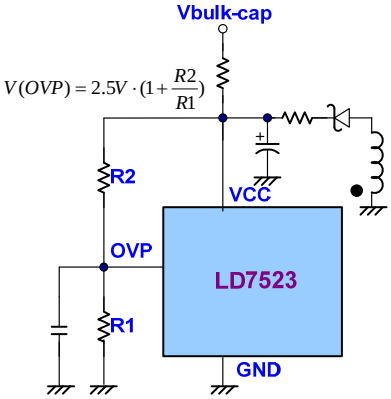


Fig. 28

Over Voltage Protection (OVP)

To prevent the component from damage due to fault condition, LD7523 is implemented with protection through the OVP pin. Figure 27 and figure 28 show 2 different configurations to program the OVP setting point --- zener detection and voltage divider. It provides zero bias current during normal operation so that it will not affect the startup timing, as figure 27. But the tolerance of OVP trip point will be larger due to the distribution of the breakdown voltage of zener diode.

On the other hand, using the circuit of figure 28 will be beneficial from the minimum cost and higher OVP accuracy, but it requires larger value of R1 and R2 to avoid affecting on startup timing by the load effect.

As shown in figure 29, if the voltage on the OVP pin rise above threshold voltage of 2.5V, the output gate drive circuit will be shutdown simultaneous in order to stop switching the power MOSFET. But if the voltage on the OVP pin drops below 2.5V, it will automatically resume to the normal operation on the next UVLO(on) level.

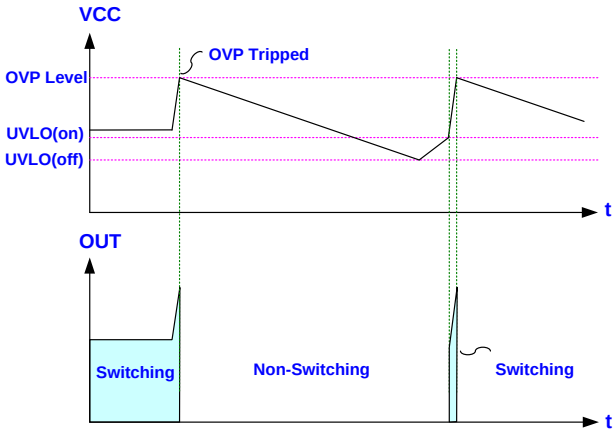


Fig. 29

Summary of Protections

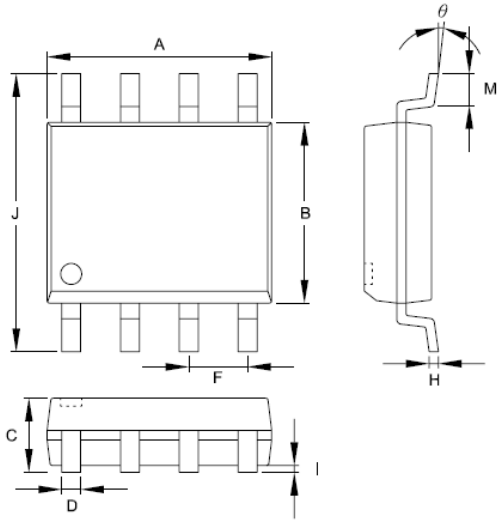
There are several ways to control the on/off of LD7523. The details are listed as the table below.

	Turn Off	Operation
COMP	Comp Pin < 1.4V	Cycle by Cycle Mode Non-latch
OLP	Comp Pin > 5.0V	Hiccup Mode Non-latch
OVP	OVP Pin > 2.5 V	Re-start after next UVLO(on)
Brownout	BNO Pin < 1.25V with Hysteresis	Cycle by cycle mode Non-latch

Table 1

Package Information

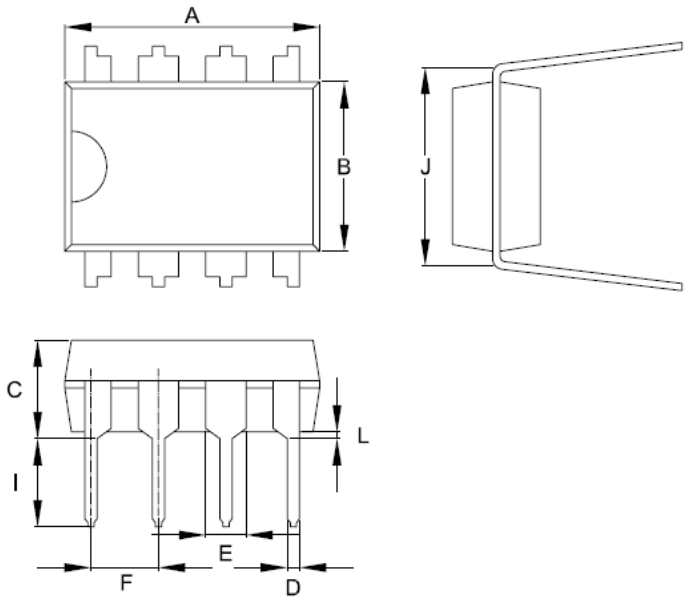
SOP-8



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.229	0.007	0.009
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Information

DIP-8



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	9.017	10.160	0.355	0.400
B	6.096	7.112	0.240	0.280
C	-----	5.334	------	0.210
D	0.356	0.584	0.014	0.023
E	1.143	1.778	0.045	0.070
F	2.337	2.743	0.092	0.108
I	2.921	3.556	0.115	0.140
J	7.366	8.255	0.29	0.325
L	0.381	------	0.015	--------

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

Rev.	Date	Change Notice
00	6/16/2009	Original Specification.