

CA-IS36xx High-performance, 5kV_{RMS} Reinforced Digital Isolators with Integrated high-efficiency, Low-emissions DC-DC Converter

1 Features

- **Integrated High-efficiency DC-DC Converter without-chip Transformer**
 - Regulated output options: 3.3 V or 5.0 V
 - Up to 650mW output power
 - Soft-start to limit inrush current and overshoot
 - Overload and short-circuit protection
 - Thermal shutdown
 - Low emissions
- **Robust Galvanic Isolation of Digital Signals**
 - High lifetime: > 40 years
 - Withstands 5kV_{RMS} for 60s
 - ±150 kV/μs typical CMTI
 - Schmitt trigger inputs
- **Interfaces Directly with Most Micros and FPGAs**
 - Data rate: DC to 150Mbps
 - 3V to 5.5V single supply operation, also provide individual logic supply input (CA-IS36xxLVW and CA-IS36xxHVW devices only)
 - Default output *High* (CA-IS362xH, CA-IS364xH) and *Low* (CA-IS362xL, CA-IS364xL) Options
- **Best in class propagation delay and skew**
 - 10ns typical propagation delay
 - 2ns propagation delay skew (chip -to-chip)
 - 1ns pulse width distortion
- **No Start-Up Initialization Required**
- **Wide-body SOIC16-WB(W) package**
- **Wide operating temperature range: -40°C to 125°C**
- **Safety Regulatory Approvals**
 - VDE 0884-11 Reinforced Isolation
 - UL According to UL1577
 - IEC 62368-1, IEC 61010-1, IEC 60950-1, GB 4943.1-2011 certifications (Pending)

2 Applications

- Industrial automation systems
- Motor control
- Medical equipment
- Test and Measurement

3 General Description

The CA-IS36xx family integrated signal and power isolation devices simplify system design and reduce board area. These devices are high-performance, dual-channel and four-channel, unidirectional reinforced digital isolators with up to 5kV_{RMS} isolation rating and ultra-fast data rate. The integrated isolated DC-DC converter provides up to 650mW of isolated power and different output voltage configurations. These devices offer high electromagnetic immunity and low emissions while isolating different ground domains and block high-voltage/high-current transients from sensitive or human interface circuitry. Each isolation channel has a logic input and output buffer separated by capacitive silicon dioxide (SiO₂) insulation barrier, the integrated Schmitt trigger on each input provide excellent noise immunity.

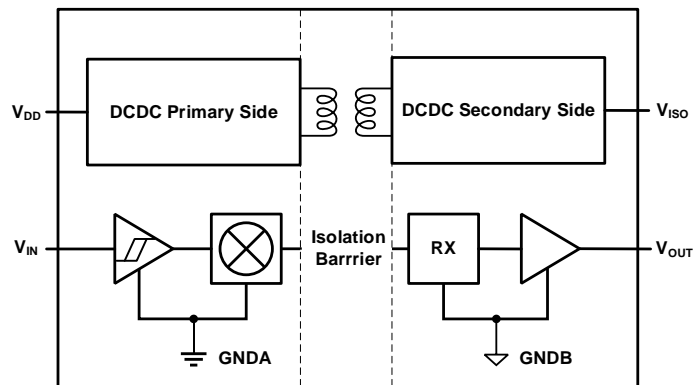
The CA-IS3620/CA-IS3621 devices are dual-channel digital isolators and the CA-IS3640/CA-IS3641/CA-IS3642/CA-IS3643/CA-IS3644 devices are quad-channel digital isolators. They offer all possible unidirectional channel configurations to accommodate any 2-channel or 4-channel digital I/Os design, including SPI, RS-485, and digital I/O applications, see Name Convention for more detail, also Table 5-1 shows the detail configurations of digital signal transmission direction for each part. The CA-IS36xx family also features different default outputs. When the input is either not powered or is open-circuit, the default output is low for devices with suffix L and high for devices with suffix H, see the Ordering Information for suffixes associated with each option. The individual logic supply input of CA-IS36xxLVW and CA-IS36xxHVW devices allows fully compatible +3.3V and +5.0V logic on side-A digital lines.

The CA-IS36xx family devices are specified over the -40°C to +125°C operating temperature range and are available in 16-pin SOIC wide body package.

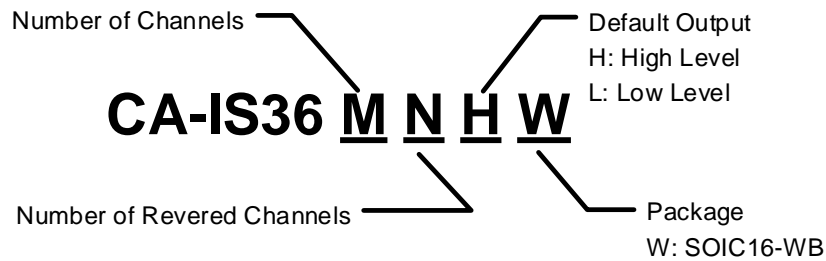
Device Information

| PART NUMBER | PACKAGE | BODY SIZE(NOM) |
|-------------|--------------|--------------------|
| CA-IS3620 | SOIC16-WB(W) | 10.30 mm × 7.50 mm |
| CA-IS3621 | | |
| CA-IS3640 | | |
| CA-IS3641 | | |
| CA-IS3642 | | |
| CA-IS3643 | | |
| CA-IS3644 | | |

Simplified Functional Diagram



4 Name Convention



5 Ordering Information
Table 5-1. Ordering Information

| Ordering Part Number | Number of Inputs A Side | Number of Inputs B Side | Default Output | Pin 7 | Isolation Rating (kV) | Package |
|----------------------|-------------------------|-------------------------|----------------|------------------|-----------------------|-----------|
| CA-IS3620LW | 2 | 0 | L | NC | 5.0 | SOIC16-WB |
| CA-IS3621LW | 1 | 1 | L | NC | 5.0 | SOIC16-WB |
| CA-IS3640LW | 4 | 0 | L | NC | 5.0 | SOIC16-WB |
| CA-IS3640HW | 4 | 0 | H | NC | 5.0 | SOIC16-WB |
| CA-IS3641LW | 3 | 1 | L | NC | 5.0 | SOIC16-WB |
| CA-IS3641HW | 3 | 1 | H | NC | 5.0 | SOIC16-WB |
| CA-IS3642LW | 2 | 2 | L | NC | 5.0 | SOIC16-WB |
| CA-IS3642HW | 2 | 2 | H | NC | 5.0 | SOIC16-WB |
| CA-IS3643LW | 1 | 3 | L | NC | 5.0 | SOIC16-WB |
| CA-IS3643HW | 1 | 3 | H | NC | 5.0 | SOIC16-WB |
| CA-IS3644LW | 0 | 4 | L | NC | 5.0 | SOIC16-WB |
| CA-IS3644HW | 0 | 4 | H | NC | 5.0 | SOIC16-WB |
| CA-IS3640LVW | 4 | 0 | L | V _{DDL} | 5.0 | SOIC16-WB |
| CA-IS3640HVW | 4 | 0 | H | V _{DDL} | 5.0 | SOIC16-WB |
| CA-IS3641LVW | 3 | 1 | L | V _{DDL} | 5.0 | SOIC16-WB |
| CA-IS3641HVW | 3 | 1 | H | V _{DDL} | 5.0 | SOIC16-WB |
| CA-IS3642LVW | 2 | 2 | L | V _{DDL} | 5.0 | SOIC16-WB |
| CA-IS3642HVW | 2 | 2 | H | V _{DDL} | 5.0 | SOIC16-WB |
| CA-IS3643LVW | 1 | 3 | L | V _{DDL} | 5.0 | SOIC16-WB |
| CA-IS3643HVW | 1 | 3 | H | V _{DDL} | 5.0 | SOIC16-WB |
| CA-IS3644LVW | 0 | 4 | L | V _{DDL} | 5.0 | SOIC16-WB |
| CA-IS3644HVW | 0 | 4 | H | V _{DDL} | 5.0 | SOIC16-WB |

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6 Revision History

| Revision Number | Description | Page Changed |
|-----------------|--|--------------|
| Version 1.00 | N/A | N/A |
| Version 1.00 | Updated pin descriptions, removed package information table. | 5, 30 |
| Version 1.02 | Added Bypass Capacitors Selections. | 29 |
| Version 1.03 | Added PCB Layout Guidelines section. | 29 |
| Version 1.04 | Added new parts of CA-IS364_VW, | 3 |
| | Updated PCB layout Guidelines. | 26 |
| | Add supply configuration | 29 |
| Version 1.05 | Updated VDE and UL certification by adding certification number. | 9 |
| | Update POD | 31 |
| Version 1.06 | Updated UL and CQC certification information | 7 |

7 Pin Configuration and Functions

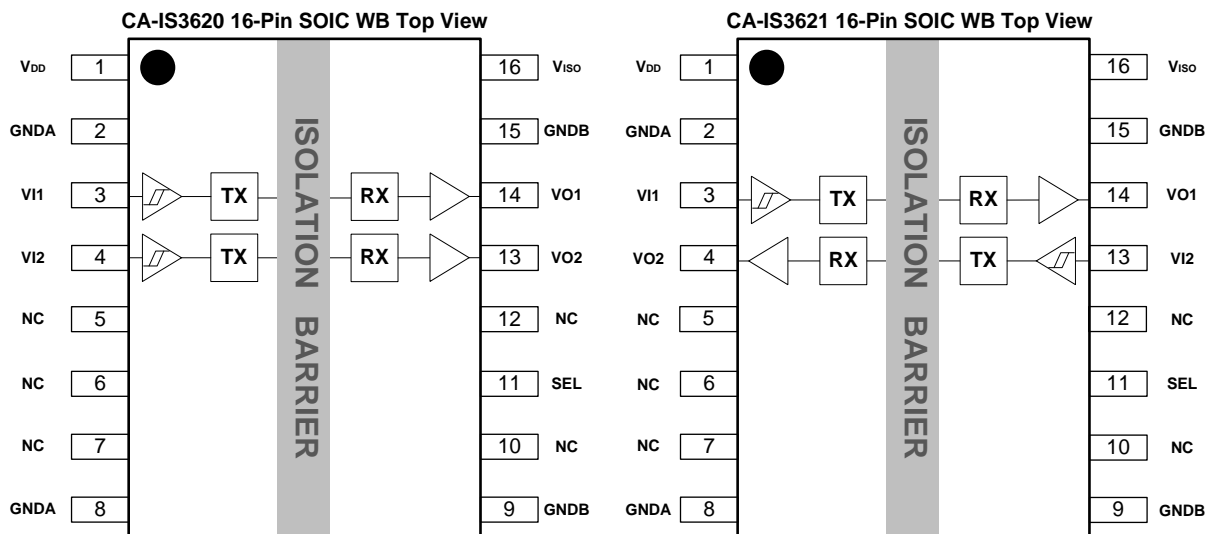


Figure 7-1. CA-IS362x pin configuration

Table 7-1. CA-IS362x Pin Description and Functions

| 16-SOIC(W) Pin# | | Name | Type | Description |
|-----------------|-----------|------------------|-------------|--|
| CA-IS3620 | CA-IS3621 | | | |
| 1 | 1 | V _{DD} | Supply | Power supply for side A. Bypass to GNDA with 10μF 0.1μF capacitors. |
| 2, 8 | 2, 8 | GNDA | Ground | Ground reference for side A. |
| 3 | 3 | VI1 | Digital I/O | Digital input 1 on side A/B, corresponds to logic output 1 on side B/A. |
| 4 | 13 | VI2 | Digital I/O | Digital input 2 on side A/B, corresponds to logic output 2 on side B/A. |
| 5, 6, 7 | 5, 6, 7 | NC | --- | Not internally connected. These pins can be left open or tied to V _{DD} or GNDA. |
| 10, 12 | 10, 12 | NC | No Connect | Not internally connected. These pins can be left open or tied to V _{ISO} or GNDB. |
| 9, 15 | 9, 15 | GNDB | Ground | Ground reference for side B. |
| 11 | 11 | SEL | Digital I/O | V _{ISO} output selection pin, see Table 10-3. V _{ISO} = 5 V, when SEL is connected to V _{ISO} . V _{ISO} = 3.3 V, when SEL is connected to GNDB or left floating. |
| 13 | 4 | VO2 | Digital I/O | Digital output 2 on side B/A, VO2 is the logic output for the VI2 input on side A/B. |
| 14 | 14 | VO1 | Digital I/O | Digital output 1 on side B/A, VO1 is the logic output for the VI1 input on side A/B. |
| 16 | 16 | V _{ISO} | Supply | Output of the isolated DC-DC converter. Bypass to GNDB with 10μF 0.1μF capacitors. The 0.1μF capacitor should be placed as close as possible to the pin. |

Note:

- Logic-Supply Input. V_{DDL} can be different voltage from V_{DD} supply, which allows fully compatible +3.3V and +5.0V logic on side-A digital lines.

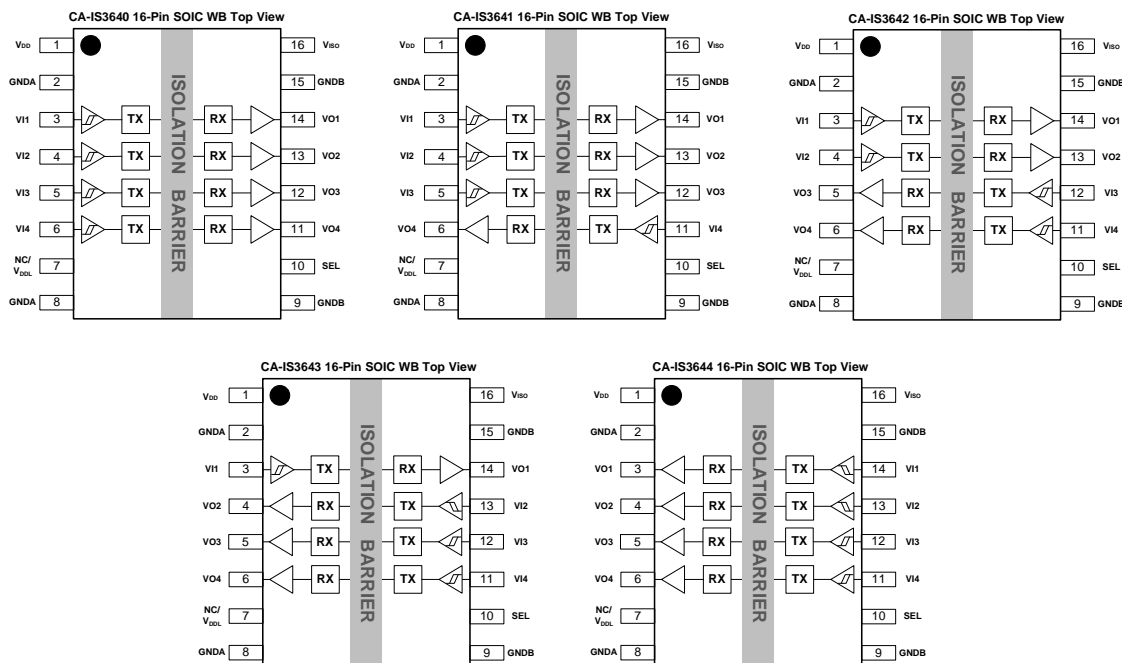


Figure 7-2. CA-IS364x pin configuration

Table 7-2. CA-IS364x Pin Description and Functions

| 16-SOIC(W) Pin# | | | | | Name | Type | Description |
|-----------------|-----------|-----------|-----------|-----------|------------------|-------------|---|
| CA-IS3640 | CA-IS3641 | CA-IS3642 | CA-IS3643 | CA-IS3644 | | | |
| 1 | 1 | 1 | 1 | 1 | V _{DD} | Supply | Power supply for side A. Bypass to GNDA with 10μF 0.1μF capacitors. |
| 2, 8 | 2, 8 | 2, 8 | 2, 8 | 2, 8 | GNDA | Ground | Ground reference for side A. |
| 3 | 3 | 3 | 3 | 14 | VI1 | Digital I/O | Digital input 1 on side A/B, corresponds to logic output 1 on side B/A. |
| 4 | 4 | 4 | 13 | 13 | VI2 | Digital I/O | Digital input 2 on side A/B, corresponds to logic output 2 on side B/A. |
| 5 | 5 | 12 | 12 | 12 | VI3 | Digital I/O | Digital input 3 on side A/B, corresponds to logic output 3 on side B/A. |
| 6 | 11 | 11 | 11 | 11 | VI4 | Digital I/O | Digital input 4 on side A/B, corresponds to logic output 4 on side B/A. |
| 7 | 7 | 7 | 7 | 7 | NC | --- | Not internally connected for the CA-IS364xLW and CA-IS364xHW devices. |
| 9, 15 | 9, 15 | 9, 15 | 9, 15 | 9, 15 | GNDB | Ground | Ground reference for side B. |
| 10 | 10 | 10 | 10 | 10 | SEL | Digital I/O | V _{ISO} selection pin, see Table 10-3. V _{ISO} = 5 V, when SEL is connected to V _{ISO} ; V _{ISO} = 3.3 V, when SEL is connected to GNDB or left floating. |
| 11 | 6 | 6 | 6 | 6 | VO4 | Digital I/O | Digital output 4 on side B/A, VO4 is the logic output for the VI4 input on side A/B. |
| 12 | 12 | 5 | 5 | 5 | VO3 | Digital I/O | Digital output 3 on side B/A, VO3 is the logic output for the VI3 input on side A/B. |
| 13 | 13 | 13 | 4 | 4 | VO2 | Digital I/O | Digital output 2 on side B/A, VO2 is the logic output for the VI2 input on side A/B. |
| 14 | 14 | 14 | 14 | 3 | VO1 | Digital I/O | Digital output 1 on side B/A, VO1 is the logic output for the VI1 input on side A/B. |
| 16 | 16 | 16 | 16 | 16 | V _{ISO} | Supply | Output of the isolated DC-DC converter. Bypass to GNDB with 10μF 0.1μF capacitors. |

Note:
 1. Logic-Supply Input. V_{D_{DL}} can be different voltage from V_{DD} supply, which allows fully compatible +3.3V and +5.0V logic on side-A digital lines.

8 Specifications

8.1 Absolute Maximum Ratings^{1, 2}

| | | MIN | MAX | UNIT |
|------------------------------------|-------------------------------|------|-----------------------------------|------|
| V _{DD} , V _{DDL} | Supply voltage | -0.5 | 6.0 | V |
| V _{ISO} | Isolated supply voltage | -0.5 | 6.0 | V |
| V _{IO} | Voltage at VIx, VOx, SEL pins | -0.5 | V _{DD} +0.5 ³ | V |
| I _O | Output current | -20 | 20 | mA |
| T _J | Junction temperature | | 150 | °C |
| T _{STG} | Storage temperature | -65 | 150 | °C |

Notes:

- The stresses listed under “Absolute Maximum Ratings” are stress ratings only, not for functional operation condition. Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device.
- All voltage values are with respect to the local ground terminal (GNDA or GNDB) and are peak voltage values.
- Maximum voltage must not be exceed 6 V.

8.2 ESD Ratings

| | | VALUE | UNIT |
|--|--|-------|------|
| V _{ESD} Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ¹ | ±6000 | V |
| | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ² | ±2000 | |

Notes:

- Per JEDEC document JEP155, 500V HBM allows safe manufacturing of standard ESD control process.
- Per JEDEC document JEP157, 250V CDM allows safe manufacturing of standard ESD control process.

8.3 Recommended Operating Conditions

| | | MIN | TYP | MAX | UNIT |
|------------------|---------------------------|------------------------------------|-----|-----|------|
| V _{DD} | Supply Voltage | 3.15 | | 5.5 | V |
| V _{DDL} | Logic Supply Voltage | 2.375 | | 5.5 | V |
| I _{OH} | High-level Output Current | V _{DDO} ¹ = 5V | -4 | | mA |
| | | V _{DDO} = 3.3V | -2 | | |
| I _{OL} | Low-level Output Current | V _{DDO} = 5V | | 4 | mA |
| | | V _{DDO} = 3.3V | | 2 | |
| V _{IH} | High-level Input Voltage | 2.0 | | | V |
| V _{IL} | Low-level Input Voltage | | | 0.8 | V |
| DR | Data Rate | 0 | | 150 | Mbps |
| T _A | Ambient Temperature | -40 | 25 | 125 | °C |

Note:

- V_{DDO} = Output-side supply, V_{ISO}.

8.4 Thermal Information

| THERMAL METRIC | CA-IS36xx | UNIT |
|---|-----------|------|
| | SOIC16-WB | |
| R _{θJA} Junction-to-ambient thermal resistance | 68.5 | °C/W |

8.5 Power Rating

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|-----|-----|-----|------|
| P _D Maximum Power Dissipation | V _{DD} = 5.5V, V _{ISO} = 5V, I _{ISO} = 130mA, all the input signal is 50% duty circle square and C _L = 15pF. | | | 1 | W |

8.6 Insulation Specifications

| PARAMETR | | TEST CONDITIONS | VALUE | UNIT |
|--|---|---|------------|-----------|
| | | | W | |
| CLR | External clearance | Shortest terminal-to-terminal distance through air | 8 | mm |
| CPG | External creepage | Shortest terminal-to-terminal distance across the package surface | 8 | mm |
| DTI | Distance through the insulation | Minimum internal gap (internal clearance) | 19 | μm |
| CTI | Comparative tracking index | DIN EN 60112 (VDE 0303-11); IEC 60112 | >400 | V |
| | Material group | According to IEC 60664-1 | II | |
| | Overvoltage category per IEC 60664-1 | Rated mains voltage $\leq 300 V_{RMS}$ | I-IV | |
| | | Rated mains voltage $\leq 400 V_{RMS}$ | I-IV | |
| | | Rated mains voltage $\leq 600 V_{RMS}$ | I-III | |
| DIN V VDE V 0884-11:2017-01¹ | | | | |
| V_{IORM} | Maximum repetitive peak isolation voltage | AC voltage (bipolar) | 1414 | V_{PK} |
| V_{IOWM} | Maximum working isolation voltage | AC voltage; Time dependent dielectric breakdown (TDDB) Test | 1000 | V_{RMS} |
| | | DC voltage | 1414 | V_{DC} |
| V_{IOTM} | Maximum transient isolation voltage | $V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production) | 7070 | V_{PK} |
| V_{IOSM} | Maximum surge isolation voltage ² | Test method per IEC 60065, 1.2/50 μs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ (qualification) | 6250 | V_{PK} |
| Q_{pd} | Apparent charge ³ | Method a, after input/output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, $t_{ini} = 60$ s; $V_{pd(m)} = 1.2 \times V_{IORM}$, $t_m = 10$ s | ≤ 5 | pC |
| | | Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, $t_{ini} = 60$ s; $V_{pd(m)} = 1.6 \times V_{IORM}$, $t_m = 10$ s | ≤ 5 | |
| | | Method b1, at routine test (100% production) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$, $t_{ini} = 1$ s; $V_{pd(m)} = 1.875 \times V_{IORM}$, $t_m = 1$ s | ≤ 5 | |
| C_{IO} | Barrier capacitance, input to output ⁴ | $V_{IO} = 0.4 \times \sin(2\pi ft)$, f = 1 MHz | ~0.5 | pF |
| R_{IO} | Isolation resistance | $V_{IO} = 500$ V, $T_A = 25^\circ\text{C}$ | $>10^{12}$ | Ω |
| | | $V_{IO} = 500$ V, $100^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ | $>10^{11}$ | |
| | | $V_{IO} = 500$ V at $T_S = 150^\circ\text{C}$ | $>10^9$ | |
| | Pollution degree | | 2 | |
| UL² | | | | |
| $V_{ISO(max)}$ | Maximum withstanding isolation voltage | $V_{TEST} = V_{ISO}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production) | 5000 | V_{RMS} |
| Notes: | | | | |
| 1. This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits. | | | | |
| 2. Devices are immersed in oil during surge characterization test. | | | | |
| 3. The characterization charge is discharging charge (pd) caused by partial discharge. | | | | |
| 4. Capacitance and resistance are measured with all pins on field-side and logic-side tied together. | | | | |

8.7 Safety-Related Certifications

| VDE | CSA(Pending) | UL | CQC | TUV(Pending) |
|--|--|--|---|---|
| Certified according to DIN VDE V 0884-11:2017-01 | Certified according to IEC 60950-1 and IEC 60601-1 | Recognized under UL 1577 Component Recognition Program | Certified according to GB4943.1-2011 | Certified according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A2:2013 |
| <p>Basic isolation: Maximum transient isolation voltage: 7070Vpk Maximum repetitive-peak isolation voltage: 849 Vpk Maximum surge isolation voltage: 6250Vpk.</p> <p>Reinforced isolation: Maximum transient isolation voltage: 7070Vpk Maximum repetitive-peak isolation voltage: 1414 Vpk Maximum surge isolation voltage: 6250Vpk.(Pending)</p> | | Protection voltage: 5kV _{RMS} | | |
| Certificate number: 40054252 | | Certificate number: E511334-20210507 | Certificate number: 15801-DK001041-202302080 | |

8.8 Electrical Characteristics

5 V Input, 5 V output

$V_{DD} = V_{DDL} = 5 V \pm 10\%$, $T_A = -40$ to 125°C , SEL shorted to V_{ISO} (over recommended operating conditions, unless otherwise specified)

| Parameters | | Test Conditions | Min. | Typ. | Max. | Unit |
|-----------------|--|---|-------------------|-------------------|------|-------------------|
| V_{ISO} | Isolated supply voltage | $I_{ISO} = 0$ to 130mA | 4.75 | 5 | 5.25 | V |
| I_{ISO} | Maximum load current ¹ | Data-rate of each channel: DR<1Mbps CA-IS3644LW/CA-IS3644LVW/ CA-IS3644HW/CA-IS3644HVW Data-rate of each channel: DR = 100Mbps | | 130 | | mA |
| | | CA-IS3621LW CA-IS3643LW/CA-IS3643LVW/ CA-IS3643HW/CA-IS3643HVW Data-rate of each channel: DR = 100Mbps | | 120 | | |
| | | CA-IS3620LW CA-IS3642LW/CA-IS3642LVW/ CA-IS3642HW/CA-IS3642HVW Data-rate of each channel: DR = 100Mbps | | 110 | | |
| | | CA-IS3641LW/CA-IS3641LVW/ CA-IS3641HW/CA-IS3641HVW Data-rate of each channel: DR = 100Mbps | | 100 | | |
| | | CA-IS3641LW/CA-IS3641LVW/ CA-IS3641HW/CA-IS3641HVW Data-rate of each channel: DR = 100Mbps | | 90 | | |
| | | CA-IS3640LW/CA-IS3640LVW/ CA-IS3640HW/CA-IS3640HVW Data-rate of each channel: DR = 100Mbps | | 80 | | |
| $V_{ISO(LINE)}$ | DC line regulation | $I_{ISO}=50\text{mA}$, $V_{DD}=4.5\text{V}$ to 5.5V | | 2 | | mV/V |
| $V_{ISO(LOAD)}$ | DC load regulation | $I_{ISO}=0$ to 130mA | | 1% | | |
| EFF | Efficiency@maximum load current | $I_{ISO} = 130\text{mA}$, $C_{LOAD} = 0.1\mu\text{F} 10\mu\text{F}$; $V_I = V_{DDI}^2$ (CA-IS36xxL); $V_I = 0\text{V}$ (CA-IS36xxH) | | 53% | | |
| $V_{DD(UVLO+)}$ | V_{DD} undervoltage threshold when supply voltage is rising | | | 2.75 | 3.05 | V |
| $V_{DD(UVLO-)}$ | V_{DD} undervoltage threshold when supply voltage is falling | | 2.0 | 2.35 | | V |
| $V_{HYS(UVLO)}$ | V_{DD} undervoltage threshold hysteresis | | | 0.40 | | V |
| I_{IH} | High-level input leakage current | $V_{IH}=V_{DDI}^1$ at V _{Ix} or B _x or SEL | | | 20 | μA |
| I_{IL} | Low-level input leakage current | $V_{IL}=0\text{V}$ at V _{Ix} or B _x or SEL | -20 | | | μA |
| V_{OH} | High-level output voltage | $I_{OL}=-4\text{mA}$, see Figure 9-1 | $V_{DDO}^2 - 0.4$ | $V_{DDO}^2 - 0.2$ | | V |
| V_{OL} | Low-level output voltage | $I_{OL}=4\text{mA}$, see Figure 9-1 | | 0.2 | 0.4 | V |
| CMTI | Common-mode transient immunity | $V_I = V_{DDI}^1$ or 0V , $V_{CM}=1500\text{V}$, see Figure 9-2 | 100 | 150 | | kV/ μs |
| $V_{ISO(RIP)}$ | Output ripple on isolated supply (pk-pk) | V_{ISO} shorted to GNDB | | 50 | | mV |
| I_{ISO} | V_{ISO} output current for external load ² | | | 60 | | mV |

Notes:

- The maximum V_{ISO} output current will be decreased with the data rate increased to each isolation channel. Also, the available output current will be reduced when $T_A > 85^\circ\text{C}$, see Figure 8-11. to Figure 8-16. the maximum output current of V_{ISO} vs. temperature.
- V_{DDI} = input side supply; V_{DDO} = output side supply.

5 V Input, 3.3V Output
 $V_{DD} = V_{DDL} = 5\text{ V} \pm 10\%$, $T_A = -40\text{ to }125^\circ\text{C}$, SEL shorted to GNDB (over recommended operating conditions, unless otherwise specified)

| Parameters | | Test Conditions | Min | Typ | Max | Unit |
|-----------------|--|--|-------------------|-------------------|------|-------------------|
| V_{ISO} | Isolated supply voltage | $I_{ISO} = 0\text{ to }130\text{mA}$ | 3.13 | 3.3 | 3.47 | V |
| I_{ISO} | Maximum load current ¹ | Data-rate of each channel: DR<1Mbps | | 130 | | mA |
| | | CA-IS3644LW/CA-IS3644LVW/ CA-IS3644HW/CA-IS3644HVW Data-rate of each channel: DR = 100Mbps | | 120 | | |
| | | CA-IS3621LW CA-IS3643LW/CA-IS3643LVW/ CA-IS3643HW/CA-IS3643HVW Data-rate of each channel: DR = 100Mbps | | 110 | | |
| | | CA-IS3620LW CA-IS3642LW/CA-IS3642LVW/ CA-IS3642HW/CA-IS3642HVW Data-rate of each channel: DR = 100Mbps | | 100 | | |
| | | CA-IS3641LW/CA-IS3641LVW/ CA-IS3641HW/CA-IS3641HVW Data-rate of each channel: DR = 100Mbps | | 90 | | |
| | | CA-IS3640LW/CA-IS3640LVW/ CA-IS3640HW/CA-IS3640HVW Data-rate of each channel: DR = 100Mbps | | 80 | | |
| $V_{ISO(LINE)}$ | DC line regulation | $I_{ISO}=50\text{mA}$, $V_{DD}=4.5\text{V to }5.5\text{V}$ | | 2 | | mV/V |
| $V_{ISO(LOAD)}$ | DC load regulation | $I_{ISO}=0\text{ to }130\text{mA}$ | | 1% | | |
| EFF current | Efficiency@maximum load | $I_{ISO} = 130\text{mA}$, $C_{LOAD} = 0.1\mu\text{F} \parallel 10\mu\text{F}$; $V_I = V_{DDI}^2$ (CA-IS36xxL); $V_I = 0\text{V}$ (CA-IS36xxH) | | 42% | | |
| $V_{DD(UVLO+)}$ | V_{DD} undervoltage threshold when supply voltage is rising | | | 2.75 | 3.05 | V |
| $V_{DD(UVLO-)}$ | V_{DD} undervoltage threshold when supply voltage is falling | | 2.0 | 2.35 | | V |
| $V_{HYS(UVLO)}$ | V_{DD} undervoltage threshold hysteresis | | | 0.4 | | V |
| I_{IH} | High-level input leakage current | $V_{IH}=V_{DDI}^1$ at V _{Ix} or B _x or EN _x or SEL | | | 20 | μA |
| I_{IL} | Low-level input leakage current | $V_{IL}=0\text{V}$ at V _{Ix} or B _x or EN _x or SEL | -20 | | | μA |
| V_{OH} | High-level output voltage | $I_{OL}=-4\text{mA}$, see Figure 9-1 | $V_{DDO}^2 - 0.4$ | $V_{DDO}^2 - 0.2$ | | V |
| V_{OL} | Low-level output voltage | $I_{OL}=4\text{mA}$, see Figure 9-1 | | 0.2 | 0.4 | V |
| CMTI | Common-mode transient immunity | $V_I = V_{DDI}^1$ or 0V, $V_{CM}=1500\text{V}$, see Figure 9-2 | 100 | 150 | | kV/ μs |
| $V_{ISO(RIP)}$ | Output ripple on isolated supply (pk-pk) | V_{ISO} shorted to GNDB | | 50 | | mA |
| I_{ISO} | V_{ISO} output current for external load ² | | | 50 | | mV |

Notes:

- The maximum V_{ISO} output current will be decreased with the data rate increased to each isolation channel. Also, the available output current will be reduced when $T_A > 85^\circ\text{C}$, see Figure 8-11. to Figure 8-16. the maximum output current of V_{ISO} vs. temperature.
- V_{DDI} = input side supply; V_{DDO} = output side supply.

CA-IS3620, CA-IS3621
CA-IS3640, CA-IS3641, CA-IS3642, CA-IS3643, CA-IS3644
Version 1.06, 2023/03/14

Shanghai Chipanalog Microelectronics Co., Ltd.

3.3V Input, 3.3 V Output
 $V_{DD} = V_{DDL} = 3.3 V \pm 10\%$, $T_A = -40$ to 125°C , SEL shorted to GNDB (over recommended operating conditions, unless otherwise specified)

| Parameters | | Test Conditions | Min | Typ | Max | Unit |
|-----------------|--|--|-------------------|-------------------|------|-------------------|
| V_{ISO} | Isolated supply voltage | $I_{ISO} = 0$ to 75mA | 3.13 | 3.3 | 3.47 | V |
| I_{ISO} | Maximum load current ¹ | Data-rate of each channel: DR<1Mbps | | 75 | | mA |
| | | CA-IS3644LW/CA-IS3644LVW/ CA-IS3644HW/CA-IS3644HVW Data-rate of each channel: DR = 100Mbps | | 65 | | |
| | | CA-IS3621LW CA-IS3643LW/CA-IS3643LVW/ CA-IS3643HW/CA-IS3643HVW Data-rate of each channel: DR = 100Mbps | | 60 | | |
| | | CA-IS3620LW CA-IS3642LW/CA-IS3642LVW/ CA-IS3642HW/CA-IS3642HVW Data-rate of each channel: DR = 100Mbps | | 55 | | |
| | | CA-IS3641LW/CA-IS3641LVW/ CA-IS3641HW/CA-IS3641HVW Data-rate of each channel: DR = 100Mbps | | 50 | | |
| | | CA-IS3640LW/CA-IS3640LVW/ CA-IS3640HW/CA-IS3640HVW Data-rate of each channel: DR = 100Mbps | | 45 | | |
| $V_{ISO(LINE)}$ | DC line regulation | $I_{ISO} = 50\text{mA}$, $V_{DD} = 3\text{V}$ to 3.6V | | 2 | | mV/V |
| $V_{ISO(LOAD)}$ | DC load regulation | $I_{ISO} = 0$ to 75mA | | 1% | | |
| EFF | Efficiency@maximum load current | $I_{ISO} = 75\text{mA}$, $C_{LOAD} = 0.1\mu\text{F} 10\mu\text{F}$; $V_I = V_{DDI}^2$ (CA-IS36xxL); $V_I = 0\text{V}$ (CA-IS36xxH) | | 47% | | |
| $V_{DD(UVLO+)}$ | V_{DD} undervoltage threshold when supply voltage is rising | | | 2.75 | 3.05 | V |
| $V_{DD(UVLO-)}$ | V_{DD} undervoltage threshold when supply voltage is falling | | 2.1 | 2.35 | | V |
| $V_{HYS(UVLO)}$ | V_{DD} undervoltage threshold hysteresis | | | 0.4 | | V |
| I_{IH} | High-level input leakage current | $V_{IH} = V_{DDI}^2 @ V_{IX}$ or SEL | | | 20 | μA |
| I_{IL} | Low-level input leakage current | $V_{IL} = 0\text{V} @ V_{IX}$ or SEL | -20 | | | μA |
| V_{OH} | High-level output voltage | $I_{OL} = -4\text{mA}$, see Figure 9-1 | $V_{DDO}^2 - 0.4$ | $V_{DDO}^2 - 0.2$ | | V |
| V_{OL} | Low-level output voltage | $I_{OL} = 4\text{mA}$, see Figure 9-1 | | 0.2 | 0.4 | V |
| CMTI | Common-mode transient immunity | $V_I = V_{DDI}^1$ or 0V , $V_{CM} = 1500\text{V}$, see Figure 9-2 | 100 | 150 | | kV/ μs |
| $V_{ISO(RIP)}$ | Output ripple on isolated supply (pk-pk) | V_{ISO} shorted to GNDB | | 36 | | mA |
| I_{ISO} | V_{ISO} output current for external load ² | | | 45 | | mV |

Notes:

- The maximum V_{ISO} output current will be decreased with the data rate increased to each isolation channel. Also, the available output current will be reduced when $T_A > 85^\circ\text{C}$, see Figure 8-11. to Figure 8-16. the maximum output current of V_{ISO} vs. temperature.
- V_{DDI} = input side supply; V_{DDO} = output side supply.

8.9 Supply Current Characteristics
5 V Input, 5 V Output
 $V_{DD} = V_{DDL} = 5\text{ V} \pm 10\%$, $T_A = -40$ to 125°C , SEL shorted to V_{ISO} (over recommended operating conditions, unless otherwise specified)

| Parameters | | Test Conditions | Min | Typ | Max | Unit |
|--|----------------|---|-----|-----|-----|------|
| CA-IS3620 | | | | | | |
| I_{DD}^2 | Supply current | No external I_{LOAD} ; $V_I = V_{DDI}^1$ (CA-IS3620L) | | 12 | 18 | mA |
| | | No external I_{LOAD} ; $V_I = 0\text{V}$ (CA-IS3620L) | | 10 | 15 | |
| | | All channels input 1Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 12 | 18 | |
| | | All channels input 10Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 24 | 36 | |
| | | All channels input 100Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 56 | 84 | |
| CA-IS3621 | | | | | | |
| I_{DD}^2 | Supply current | No external I_{LOAD} ; $V_I = V_{DDI}^1$ (CA-IS3621L) | | 13 | 19 | mA |
| | | No external I_{LOAD} ; $V_I = 0\text{V}$ (CA-IS3621L); | | 9 | 14 | |
| | | All channels input 1Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 11 | 17 | |
| | | All channels input 10Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 23 | 35 | |
| | | All channels input 100Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 42 | 63 | |
| | | All channels input 1Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 9 | 14 | |
| | | All channels input 10Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 20 | 30 | |
| | | All channels input 100Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 30 | 45 | |
| CA-IS3640 | | | | | | |
| I_{DD}^2 | Supply current | No external I_{LOAD} ; $V_I = 0\text{V}$ (CA-IS3640H); $V_I = V_{DDI}^1$ (CA-IS3640L) | | 17 | 26 | mA |
| | | No external I_{LOAD} ; $V_I = 0\text{V}$ (CA-IS3640L); $V_I = V_{DDI}^1$ (CA-IS3640H) | | 13 | 20 | |
| | | All channels input 1Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 16 | 24 | |
| | | All channels input 10Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 22 | 33 | |
| | | All channels input 100Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 76 | 115 | |
| Notes: | | | | | | |
| 1. V_{DDI} = input side supply; V_{DDO} = output side supply. | | | | | | |
| 2. For the CA-IS36xxVW, the I_{DD} is the total supply current from V_{DD} and V_{DDL} . | | | | | | |

Supply Current Characteristics Continued (5 V Input, 5 V Output)

| Parameters | | Test Conditions | Min | Typ | Max | Unit |
|--|----------------|--|-----|-----|-----|------|
| CA-IS3641 | | | | | | |
| I_{DD}^2 | Supply current | No external I_{LOAD} ; $V_I=0V$ (CA-IS3641H); $V_I=V_{DDI}^1$ (CA-IS3641L) | | 19 | 29 | mA |
| | | No external I_{LOAD} ; $V_I=0V$ (CA-IS3641L); $V_I=V_{DDI}^1$ (CA-IS3641H) | | 13 | 20 | |
| | | All channels input 1Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | | 16 | 24 | |
| | | All channels input 10Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | | 22 | 33 | |
| | | All channels input 100Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | | 66 | 99 | |
| CA-IS3642 | | | | | | |
| I_{DD}^2 | Supply current | No external I_{LOAD} ; $V_I=0V$ (CA-IS3642H); $V_I=V_{DDI}^1$ (CA-IS3642L) | | 18 | 27 | mA |
| | | No external I_{LOAD} ; $V_I=0V$ (CA-IS3642L); $V_I=V_{DDI}^1$ (CA-IS3642H) | | 13 | 20 | |
| | | All channels input 1Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | | 15 | 23 | |
| | | All channels input 10Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | | 20 | 30 | |
| | | All channels input 100Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | | 62 | 93 | |
| CA-IS3643 | | | | | | |
| I_{DD}^2 | Supply current | No external I_{LOAD} ; $V_I=0V$ (CA-IS3643H); $V_I=V_{DDI}^1$ (CA-IS3643L) | | 18 | 27 | mA |
| | | No external I_{LOAD} ; $V_I=0V$ (CA-IS3643L); $V_I=V_{DDI}^1$ (CA-IS3643H) | | 13 | 20 | |
| | | All channels input 1Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | | 16 | 24 | |
| | | All channels input 10Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | | 20 | 30 | |
| | | All channels input 100Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | | 62 | 93 | |
| CA-IS3644 | | | | | | |
| I_{DD}^2 | Supply current | No external I_{LOAD} ; $V_I=0V$ (CA-IS3644H); $V_I=V_{DDI}^1$ (CA-IS3644L) | | 18 | 27 | mA |
| | | No external I_{LOAD} ; $V_I=0V$ (CA-IS3644L); $V_I=V_{DDI}^1$ (CA-IS3644H) | | 13 | 20 | |
| | | All channels input 1Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | | 14 | 21 | |
| | | All channels input 10Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | | 17 | 26 | |
| | | All channels input 100Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | | 45 | 68 | |
| Notes: | | | | | | |
| 1. V_{DDI} = input side supply; V_{DDO} = output side supply. | | | | | | |
| 2. For the CA-IS36xxVW, the I_{DD} is the total supply current from V_{DD} and V_{DDL} . | | | | | | |

5 V Input, 3.3 V Output
 $V_{DD} = V_{DDL} = 5\text{ V} \pm 10\%$, $T_A = -40$ to 125°C , SEL shorted to GNDB (over recommended operating conditions, unless otherwise specified)

| Parameters | | Test Conditions | Min | Typ | Max | Unit |
|--|----------------|---|-----|-----|-----|------|
| CA-IS3620 | | | | | | |
| I_{DD}^2 | Supply current | No external I_{LOAD} ; $V_I = V_{DDI}^1$ (CA-IS3620L) | | 11 | 17 | mA |
| | | No external I_{LOAD} ; $V_I = 0\text{V}$ (CA-IS3620L); | | 9 | 14 | |
| | | All channels input 1Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 10 | 15 | |
| | | All channels input 10Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 18 | 27 | |
| | | All channels input 100Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 34 | 51 | |
| CA-IS3621 | | | | | | |
| I_{DD}^2 | Supply current | No external I_{LOAD} ; $V_I = V_{DDI}^1$ (CA-IS3621L) | | 12 | 18 | mA |
| | | No external I_{LOAD} ; $V_I = 0\text{V}$ (CA-IS3621L); | | 9 | 14 | |
| | | All channels input 1Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 9 | 14 | |
| | | All channels input 10Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 16 | 24 | |
| | | All channels input 100Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 32 | 48 | |
| | | All channels input 1Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 7 | 11 | |
| | | All channels input 10Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 14 | 21 | |
| | | All channels input 100Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 30 | 45 | |
| CA-IS3640 | | | | | | |
| I_{DD}^2 | Supply current | No external I_{LOAD} ; $V_I = 0\text{V}$ (CA-IS3640H); $V_I = V_{DDI}^1$ (CA-IS3640L) | | 15 | 23 | mA |
| | | No external I_{LOAD} ; $V_I = 0\text{V}$ (CA-IS3640L); $V_I = V_{DDI}^1$ (CA-IS3640H) | | 11 | 18 | |
| | | All channels input 1Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 13 | 19 | |
| | | All channels input 10Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 17 | 26 | |
| | | All channels input 100Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 50 | 75 | |
| Notes: | | | | | | |
| 1. V_{DDI} = input side supply; V_{DDO} = output side supply, V_{ISO} . | | | | | | |
| 2. For the CA-IS36xxVW, the I_{DD} is the total supply current from V_{DD} and V_{DDL} . | | | | | | |

Supply Current Characteristics Continued (5 V Input, 3.3 V Output)

| Parameters | | Test Conditions | Min | Typ | Max | Unit |
|--|----------------|--|-----|-----|-----|------|
| CA-IS3641 | | | | | | |
| I_{DD}^2 | Supply current | No external I_{LOAD} ; $V_I=0V$ (CA-IS3641H); $V_I=V_{DDI}^1$ (CA-IS3641L) | 16 | 24 | | mA |
| | | No external I_{LOAD} ; $V_I=0V$ (CA-IS3641L); $V_I=V_{DDI}^1$ (CA-IS3641H) | 11 | 18 | | |
| | | All channels input 1Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | 13 | 20 | | |
| | | All channels input 10Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | 16 | 24 | | |
| | | All channels input 100Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | 47 | 71 | | |
| CA-IS3642 | | | | | | |
| I_{DD}^2 | Supply current | No external I_{LOAD} ; $V_I=0V$ (CA-IS3642H); $V_I=V_{DDI}^1$ (CA-IS3642L) | 16 | 24 | | mA |
| | | No external I_{LOAD} ; $V_I=0V$ (CA-IS3642L); $V_I=V_{DDI}^1$ (CA-IS3642H) | 11 | 18 | | |
| | | All channels input 1Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | 13 | 20 | | |
| | | All channels input 10Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | 16 | 24 | | |
| | | All channels input 100Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | 46 | 69 | | |
| CA-IS3643 | | | | | | |
| I_{DD}^2 | Supply current | No external I_{LOAD} ; $V_I=0V$ (CA-IS3643H); $V_I=V_{DDI}^1$ (CA-IS3643L) | 16 | 24 | | mA |
| | | No external I_{LOAD} ; $V_I=0V$ (CA-IS3643L); $V_I=V_{DDI}^1$ (CA-IS3643H) | 11 | 18 | | |
| | | All channels input 1Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | 13 | 20 | | |
| | | All channels input 10Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | 15 | 23 | | |
| | | All channels input 100Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | 44 | 66 | | |
| CA-IS3644 | | | | | | |
| I_{DD}^2 | Supply current | No external I_{LOAD} ; $V_I=0V$ (CA-IS3644H); $V_I=V_{DDI}^1$ (CA-IS3644L) | 16 | 24 | | mA |
| | | No external I_{LOAD} ; $V_I=0V$ (CA-IS3644L); $V_I=V_{DDI}^1$ (CA-IS3644H) | 11 | 18 | | |
| | | All channels input 1Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | 13 | 20 | | |
| | | All channels input 10Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | 15 | 23 | | |
| | | All channels input 100Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | 43 | 66 | | |
| Notes: | | | | | | |
| 1. V_{DDI} = input side supply; V_{DDO} = output side supply, V_{ISO} . | | | | | | |
| 2. For the CA-IS36xxVW, the I_{DD} is the total supply current from V_{DD} and V_{DDL} . | | | | | | |

3.3 V Input, 3.3 V Output
 $V_{DD} = V_{DDL} = 3.3 \text{ V} \pm 10\%$, $T_A = -40 \text{ to } 125^\circ\text{C}$, SEL shorted to GND (over recommended operating conditions, unless otherwise specified)

| Parameters | | Test Conditions | Min | Typ | Max | Unit |
|--|----------------|---|-----|-----|-----|------|
| CA-IS3620 | | | | | | |
| I_{DD}^2 | Supply current | No external I_{LOAD} ; $V_I = V_{DDI}^1$ (CA-IS3620L) | | 10 | 15 | mA |
| | | No external I_{LOAD} ; $V_I = 0\text{V}$ (CA-IS3620L); | | 8 | 12 | |
| | | All channels input 1Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 11 | 17 | |
| | | All channels input 10Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 19 | 29 | |
| | | All channels input 100Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 40 | 60 | |
| CA-IS3621 | | | | | | |
| I_{DD}^2 | Supply current | No external I_{LOAD} ; $V_I = V_{DDI}^1$ (CA-IS3621L) | | 12 | 18 | mA |
| | | No external I_{LOAD} ; $V_I = 0\text{V}$ (CA-IS3621L); | | 8 | 12 | |
| | | All channels input 1Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 10 | 15 | |
| | | All channels input 10Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 18 | 27 | |
| | | All channels input 100Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 31 | 46 | |
| | | All channels input 1Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 9 | 14 | |
| | | All channels input 10Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 16 | 24 | |
| | | All channels input 100Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 21 | 32 | |
| CA-IS3640 | | | | | | |
| I_{DD}^2 | Supply current | No external I_{LOAD} ; $V_I = 0\text{V}$ (CA-IS3640H); $V_I = V_{DDI}^1$ (CA-IS3640L) | | 16 | 24 | mA |
| | | No external I_{LOAD} ; $V_I = 0\text{V}$ (CA-IS3640L); $V_I = V_{DDI}^1$ (CA-IS3640H) | | 12 | 18 | |
| | | All channels input 1Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 15 | 23 | |
| | | All channels input 10Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 18 | 27 | |
| | | All channels input 100Mbps, 50% duty cycle square wave clock signal, $C_L = 15\text{pF}$ each channel, no external I_{LOAD} . | | 57 | 86 | |
| Note: | | | | | | |
| 1. V_{DDI} = input side supply; V_{DDO} = output side supply, V_{ISO} . | | | | | | |
| 2. For the CA-IS36xxVW, the I_{DD} is the total supply current from V_{DD} and V_{DDL} . | | | | | | |

Supply Current Characteristics Continued (3.3 V Input, 3.3 V Output)

| Parameters | | Test Conditions | Min | Typ | Max | Unit |
|--|----------------|--|-----|-----|-----|------|
| CA-IS3641 | | | | | | |
| I_{DD}^2 | Supply current | No external I_{LOAD} ; $V_I=0V$ (CA-IS3641H); $V_I=V_{DDI}^1$ (CA-IS3641L) | 16 | 24 | | mA |
| | | No external I_{LOAD} ; $V_I=0V$ (CA-IS3641L); $V_I=V_{DDI}^1$ (CA-IS3641H) | 12 | 18 | | |
| | | All channels input 1Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | 15 | 23 | | |
| | | All channels input 10Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | 18 | 27 | | |
| | | All channels input 100Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | 50 | 75 | | |
| CA-IS3642 | | | | | | |
| I_{DD}^2 | Supply current | No external I_{LOAD} ; $V_I=0V$ (CA-IS3642H); $V_I=V_{DDI}^1$ (CA-IS3642L) | 17 | 25 | | mA |
| | | No external I_{LOAD} ; $V_I=0V$ (CA-IS3642L); $V_I=V_{DDI}^1$ (CA-IS3642H) | 12 | 18 | | |
| | | All channels input 1Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | 14 | 21 | | |
| | | All channels input 10Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | 17 | 26 | | |
| | | All channels input 100Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | 46 | 69 | | |
| CA-IS3643 | | | | | | |
| I_{DD}^2 | Supply current | No external I_{LOAD} ; $V_I=0V$ (CA-IS3643H); $V_I=V_{DDI}^1$ (CA-IS3643L) | 18 | 27 | | mA |
| | | No external I_{LOAD} ; $V_I=0V$ (CA-IS3643L); $V_I=V_{DDI}^1$ (CA-IS3643H) | 12 | 18 | | |
| | | All channels input 1Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | 14 | 21 | | |
| | | All channels input 10Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | 16 | 24 | | |
| | | All channels input 100Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | 40 | 60 | | |
| CA-IS3644 | | | | | | |
| I_{DD}^2 | Supply current | No external I_{LOAD} ; $V_I=0V$ (CA-IS3644H); $V_I=V_{DDI}^1$ (CA-IS3644L) | 18 | 27 | | mA |
| | | No external I_{LOAD} ; $V_I=0V$ (CA-IS3644L); $V_I=V_{DDI}^1$ (CA-IS3644H) | 12 | 18 | | |
| | | All channels input 1Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | 14 | 21 | | |
| | | All channels input 10Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | 16 | 24 | | |
| | | All channels input 100Mbps, 50% duty cycle square wave clock signal, $C_L=15pF$ each channel, no external I_{LOAD} . | 36 | 54 | | |
| Notes: | | | | | | |
| 1. V_{DDI} = input side supply; V_{DDO} = output side supply, V_{ISO} . | | | | | | |
| 2. For the CA-IS36xxVW, the I_{DD} is the total supply current from V_{DD} and V_{DDL} . | | | | | | |

8.10 Timing Characteristics

5 Input, 5V Output

$V_{DD} = V_{DDL} = 5\text{ V} \pm 10\%$, $T_A = -40$ to 125°C , SEL shorted to V_{ISO} (over recommended operating conditions, unless otherwise specified)

| Parameters | | Test Conditions | Min | Typ | Max | Unit |
|-----------------------|--|-----------------|-----|------|------|------|
| DR | Data rate | | 0 | | 150 | Mbps |
| PW_{minL} | Minimum Pulse Width | | | | 5.0 | ns |
| t_{PLH} , t_{PHL} | Propagation Delay Time | See Figure 9-1 | | 10.0 | 20.0 | ns |
| PWD | Pulse Width Distortion $ t_{PLH} - t_{PHL} $ | | 0.2 | 4.5 | ns | |
| $t_{rk(o)}$ | Channel-to-channel Output Skew Time ¹ | See Figure 9-1 | | 0.4 | 2.5 | ns |
| $t_{rk(pp)}$ | Chip-to-chip skew time ² | | | 2.0 | 4.5 | ns |
| t_r | Output Signal Rise Time | See Figure 9-1 | | 2.5 | 4.0 | ns |
| t_f | Output Signal Fall Time | See Figure 9-1 | | 2.5 | 4.0 | ns |

Notes:

- t_{sk} is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
- $t_{rk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

5 V Input, 3.3 V Output

$V_{DD} = V_{DDL} = 5\text{ V} \pm 10\%$, $T_A = -40$ to 125°C , SEL shorted to GND (over recommended operating conditions, unless otherwise specified)

| Parameters | | Test Conditions | Min | Typ | Max | Unit |
|-----------------------|--|-----------------|-----|------|------|------|
| DR | Data rate | | 0 | | 150 | Mbps |
| PW_{minL} | Minimum Pulse Width | | | | 5.0 | ns |
| t_{PLH} , t_{PHL} | Propagation Delay Time | See Figure 9-1 | | 10.0 | 20.0 | ns |
| PWD | Pulse Width Distortion $ t_{PLH} - t_{PHL} $ | | 0.2 | 4.5 | ns | |
| $t_{rk(o)}$ | Channel-to-channel Output Skew Time ¹ | See Figure 9-1 | | 0.4 | 2.5 | ns |
| $t_{rk(pp)}$ | Chip-to-chip skew time ² | | | 2.0 | 4.5 | ns |
| t_r | Output Signal Rise Time | See Figure 9-1 | | 2.5 | 4.0 | ns |
| t_f | Output Signal Fall Time | See Figure 9-1 | | 2.5 | 4.0 | ns |

Notes:

- t_{sk} is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
- $t_{rk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

3.3 V Input, 3.3 V Output

$V_{DD} = V_{DDL} = 3.3\text{ V} \pm 10\%$, $T_A = -40$ to 125°C , SEL shorted to GND (over recommended operating conditions, unless otherwise specified)

| Parameters | | Test Conditions | Min | Typ | Max | Unit |
|-----------------------|--|-----------------|-----|------|------|------|
| DR | Data rate | | 0 | | 150 | Mbps |
| PW_{minL} | Minimum Pulse Width | | | | 5.0 | ns |
| t_{PLH} , t_{PHL} | Propagation Delay Time | See Figure 9-1 | | 10.0 | 20.0 | ns |
| PWD | Pulse Width Distortion $ t_{PLH} - t_{PHL} $ | | 0.2 | 4.5 | ns | |
| $t_{rk(o)}$ | Channel-to-channel Output Skew Time ¹ | See Figure 9-1 | | 0.4 | 2.5 | ns |
| $t_{rk(pp)}$ | Chip-to-chip skew time ² | | | 2.0 | 4.5 | ns |
| t_r | Output Signal Rise Time | See Figure 9-1 | | 2.5 | 4.0 | ns |
| t_f | Output Signal Fall Time | See Figure 9-1 | | 2.5 | 4.0 | ns |

Notes:

- t_{sk} is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
- $t_{rk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

8.11 Typical Characteristics

| | |
|--|--|
| | |
| <p>Figure 8-1. V_{DD} quiescent current, all inputs connected to logic HIGH or logic LOW, $V_{DD} = 5V$, $V_{ISO} = 5V$</p> | <p>Figure 8-2. V_{DD} supply current for the CA-IS3641HW at different data rate ; $V_{DD} = 5V$, $V_{ISO} = 5V$</p> |
| | |
| <p>Figure 8-3. V_{DD} quiescent current, all inputs connected to logic HIGH or logic LOW, $V_{DD} = 5V$, $V_{ISO} = 3.3V$</p> | <p>Figure 8-4. V_{DD} supply current for the CA-IS3641HW at different data rate ; $V_{DD} = 5V$, $V_{ISO} = 3.3V$</p> |
| | |
| <p>Figure 8-5. V_{DD} quiescent current, all inputs connected to logic HIGH or logic LOW, $V_{DD} = 3.3V$, $V_{ISO} = 3.3V$</p> | <p>Figure 8-6. V_{DD} supply current for the CA-IS3641HW at different data rate ; $V_{DD} = 3.3V$, $V_{ISO} = 3.3V$</p> |

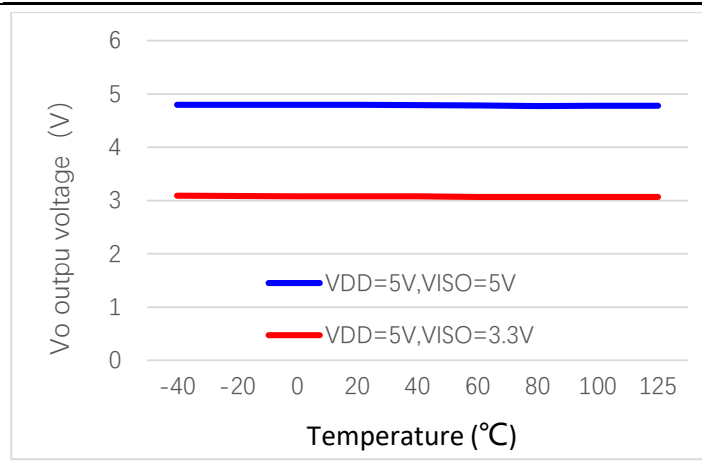


Figure 8-7. $V_O = \text{High}$, pull-down current = 4mA

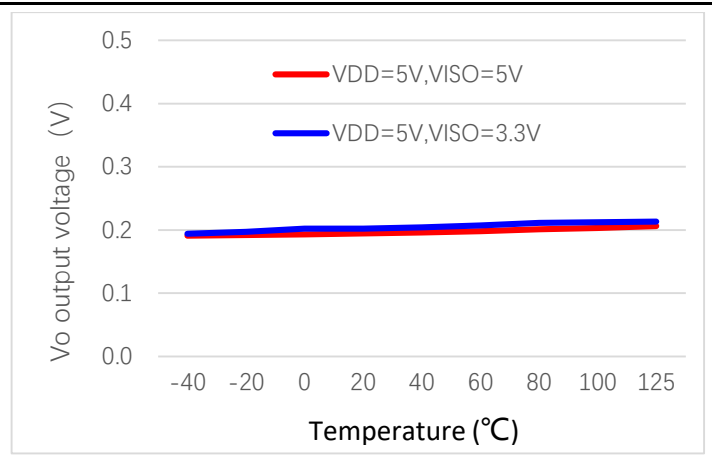


Figure 8-8. $V_O = \text{Low}$, pull-up current = 4mA

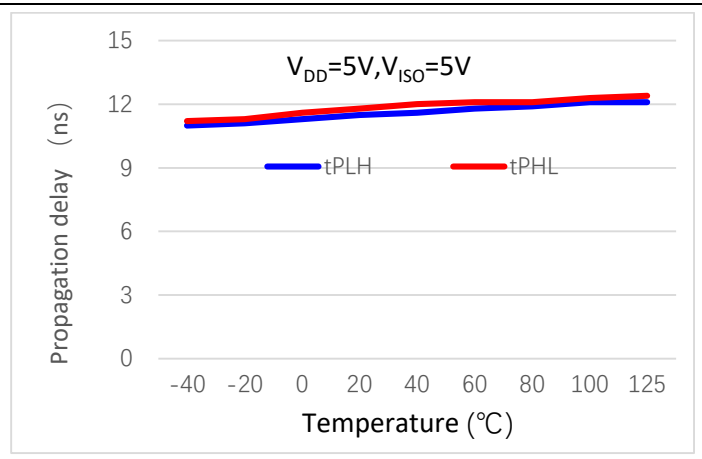


Figure 8-9. Propagation delay time vs. temperature,
 $V_{DD} = 5V$, $V_{ISO} = 5V$

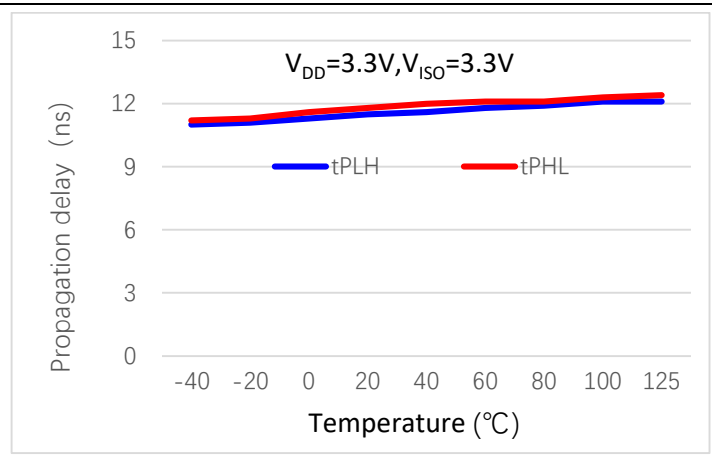


Figure 8-10. Propagation delay time vs. temperature,
 $V_{DD} = 3.3V$, $V_{ISO} = 3.3V$

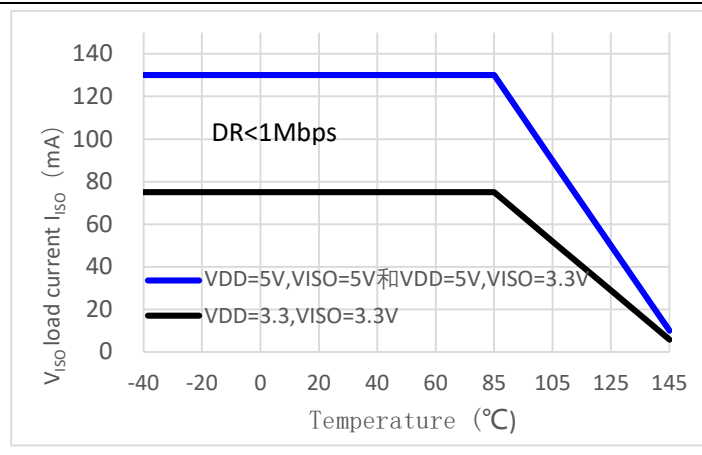


Figure 8-11.
All of CA-IS36xx devices
Maximum output current from V_{ISO} vs. temperature
DR < 1Mbps

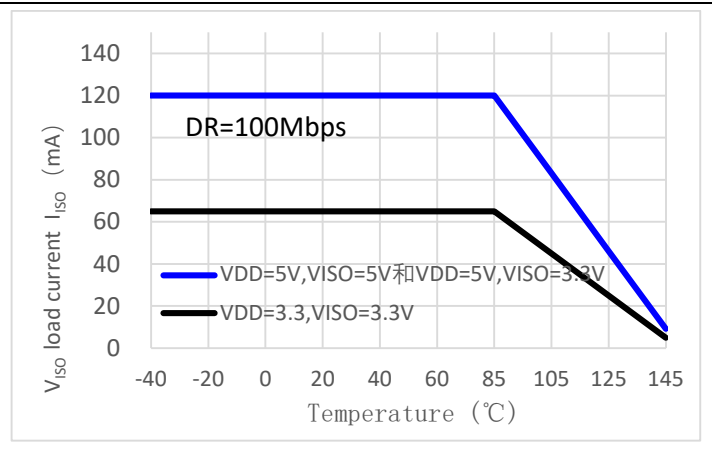


Figure 8-12.
CA-IS3621LW/CA-IS3621LVW/CA-IS3621HW/CA-IS3621HVV/
CA-IS3643LW/CA-IS3643LVW/CA-IS3643HW/CA-IS3643HVV
Maximum output current from V_{ISO} vs. temperature
DR = 100Mbps

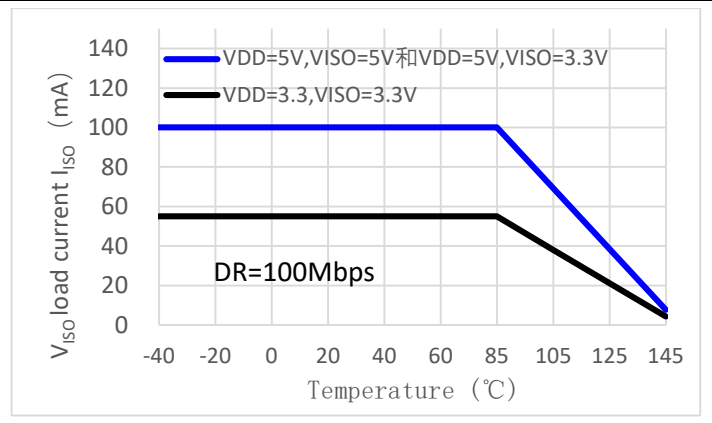
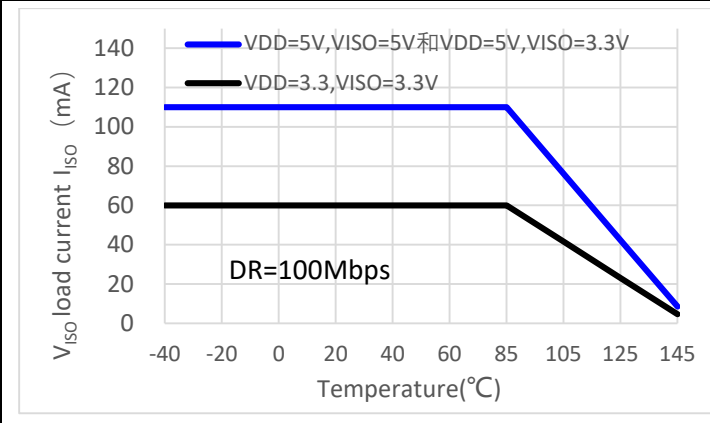


Figure 8-13.
CA-IS3621LW/CA-IS3621LVW/CA-IS3621HW/CA-IS3621HVW/
CA-IS3643LW/CA-IS3643LVW/CA-IS3643HW/CA-IS3643HVW
Maximum output current from V_{ISO} vs. temperature
DR = 100Mbps

Figure 8-14.
CA-IS3620LW/CA-IS3620LVW/ CA-IS3620HW/CA-IS3620HVW/
CA-IS3642LW/CA-IS3642LVW/CA-IS3642HW/CA-IS3642HVW
Maximum output current from V_{ISO} vs. temperature
DR = 100Mbps

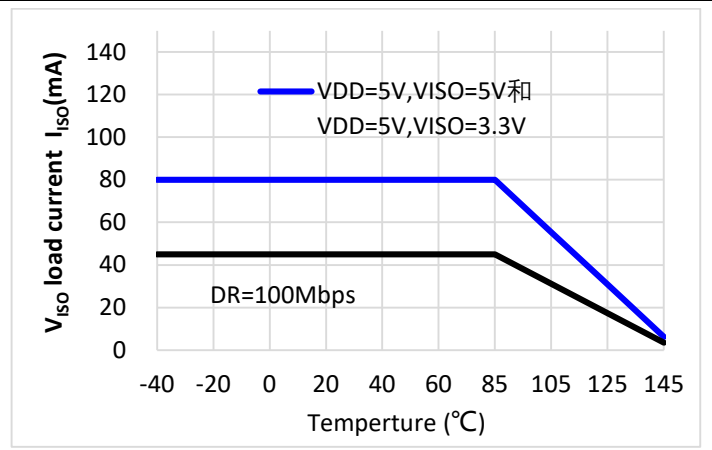
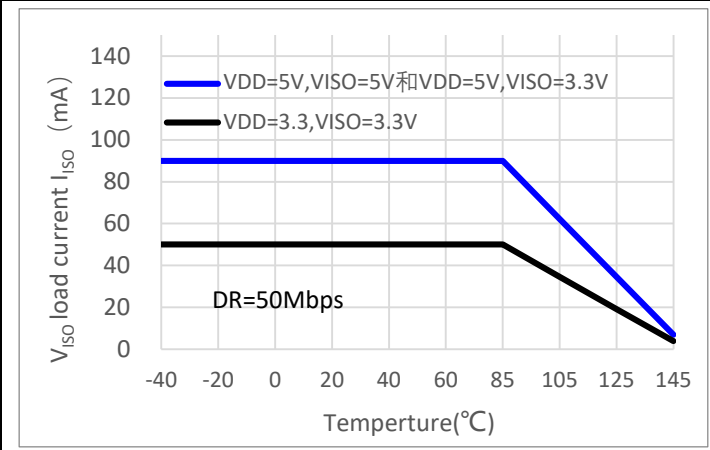


Figure 8-15.
CA-IS3641LW/CA-IS3641LVW/CA-IS3641HW/CA-IS3641HVW
Maximum output current from V_{ISO} vs. temperature
DR = 100Mbps

Figure 8-16.
CA-IS3640LW/CA-IS3640LVW/CA-IS3640HW/CA-IS3640HVW
Maximum output current from V_{ISO} vs. temperature
DR = 100Mbps

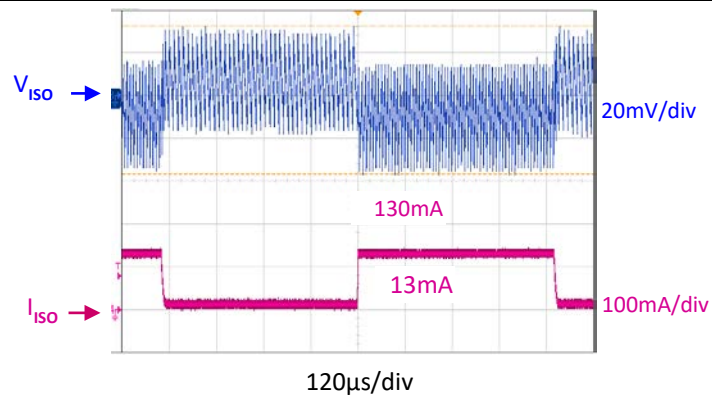
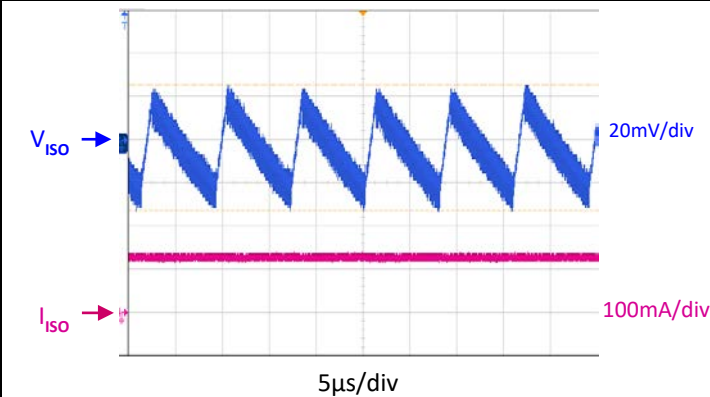
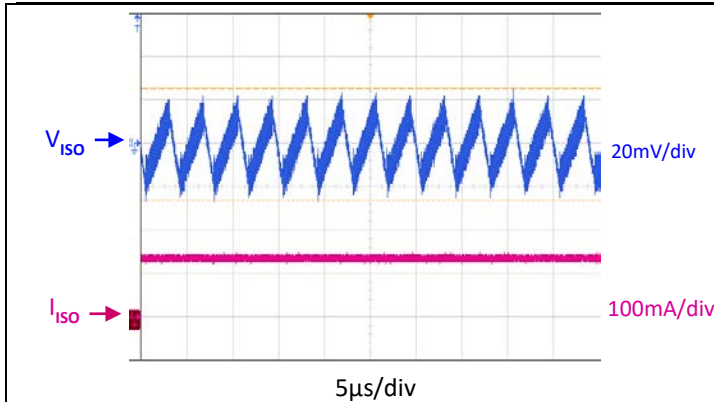
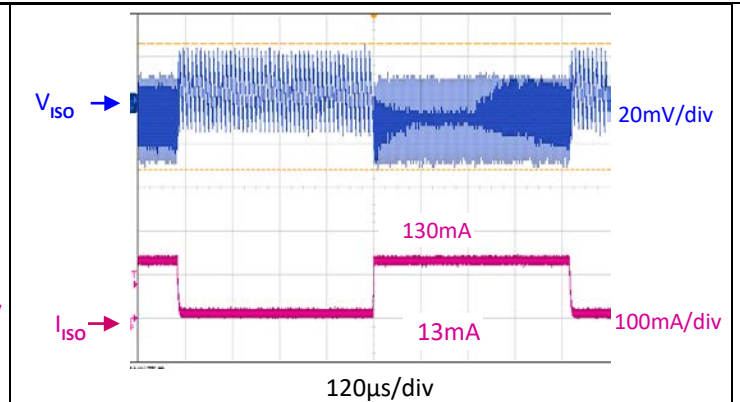
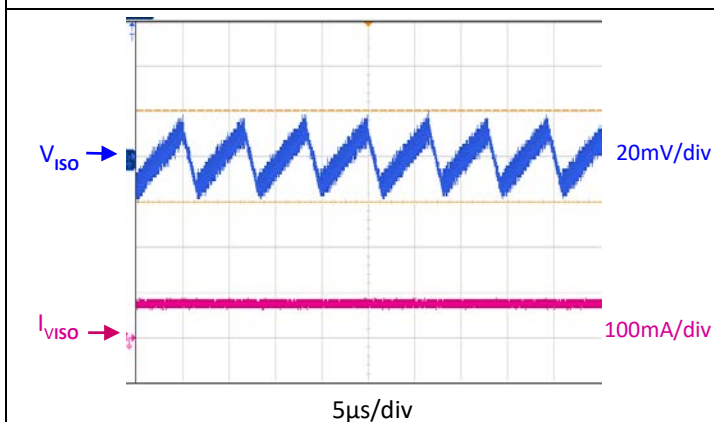
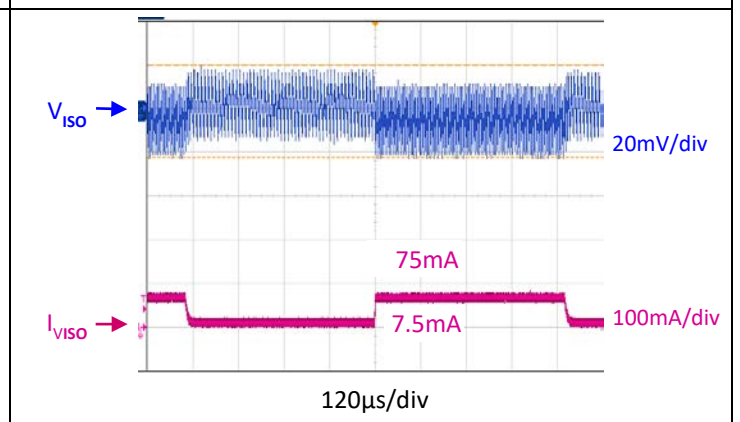
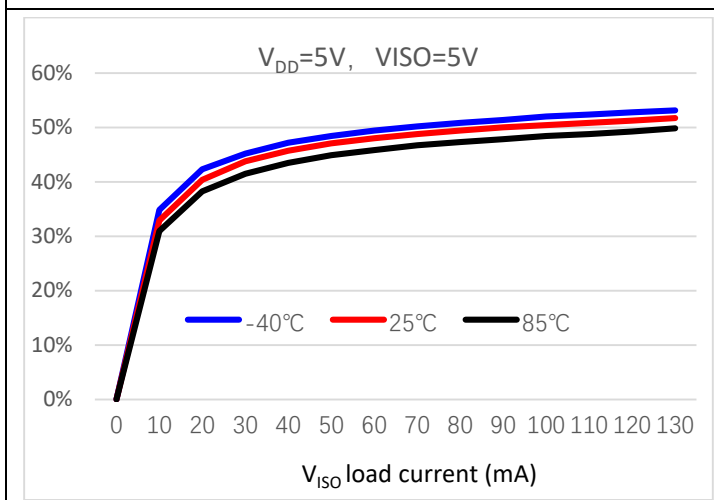
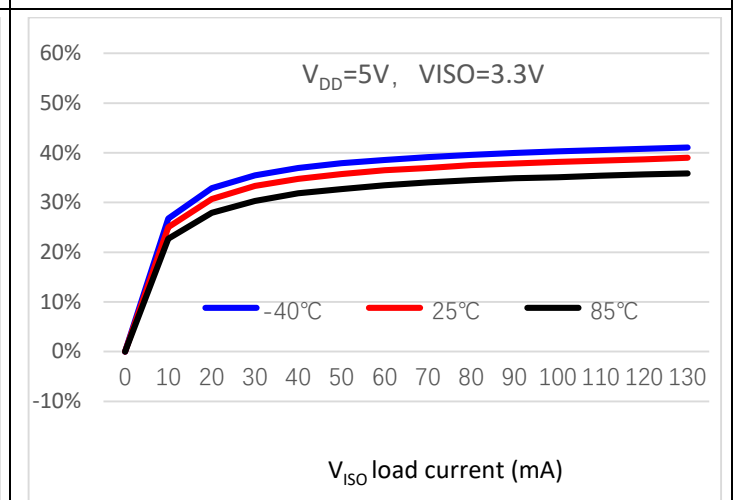


Figure 8-17. $V_{DD} = 5V$, $V_{ISO} = 5.0V$, $I_{ISO} = 130mA$;
 V_{ISO} ripple voltage @ 130mA load current: 58mV

Figure 8-18. $V_{DD} = 5V$, $V_{ISO} = 5V$, 13mA to 130mA load transient
response; V_{ISO} ripple voltage (pick to pick): 68mV

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 Figure 8-19. $V_{DD} = 5V$, $V_{ISO} = 3.3V$, $I_{ISO} = 130mA$; V_{ISO} ripple voltage @ 130mA load current: 51mV

 Figure 8-20. $V_{DD} = 5V$, $V_{ISO} = 3.3V$, 13mA to 130mA load transient response; V_{ISO} ripple voltage (pick to pick): 58mV

 Figure 8-21. $V_{DD} = 3.3V$, $V_{ISO} = 3.3V$, $I_{ISO} = 130mA$
 V_{ISO} ripple voltage @ 75mA load current: 40mV

 Figure 8-22. $V_{DD} = 3.3V$, $V_{ISO} = 3.3V$, 7.5mA to 75mA load transient response; V_{ISO} ripple voltage (pick to pick): 42mV

 Figure 8-23. Efficiency vs. load current (I_{ISO}) at different ambient temperature, $V_{DD} = 5V$, $V_{ISO} = 5V$

 Figure 8-24. Efficiency vs. load current (I_{ISO}) at different ambient temperature, $V_{DD} = 5V$, $V_{ISO} = 3.3V$

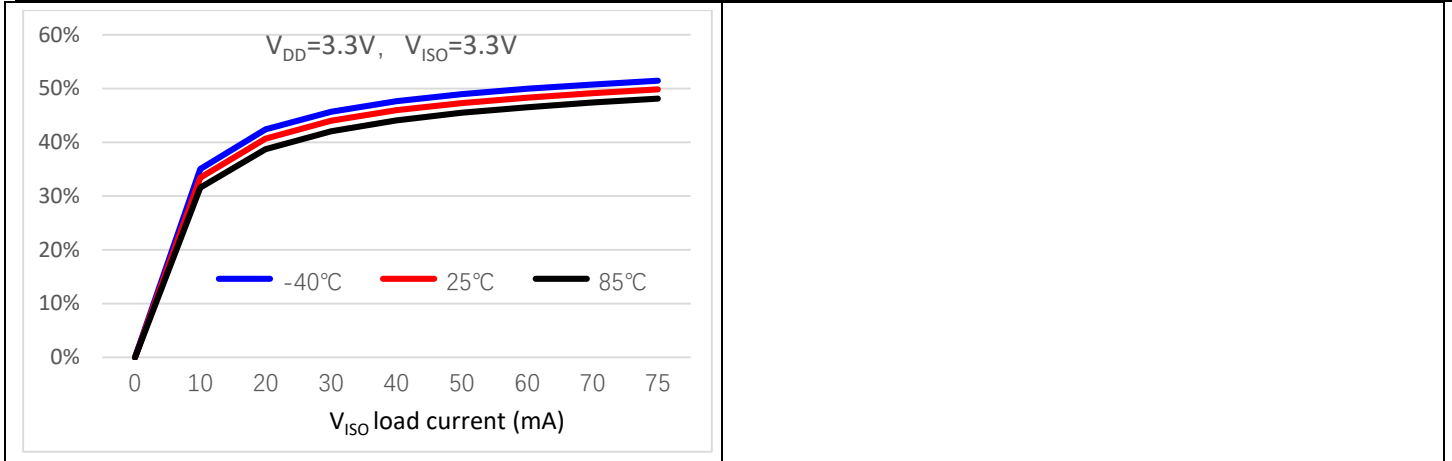
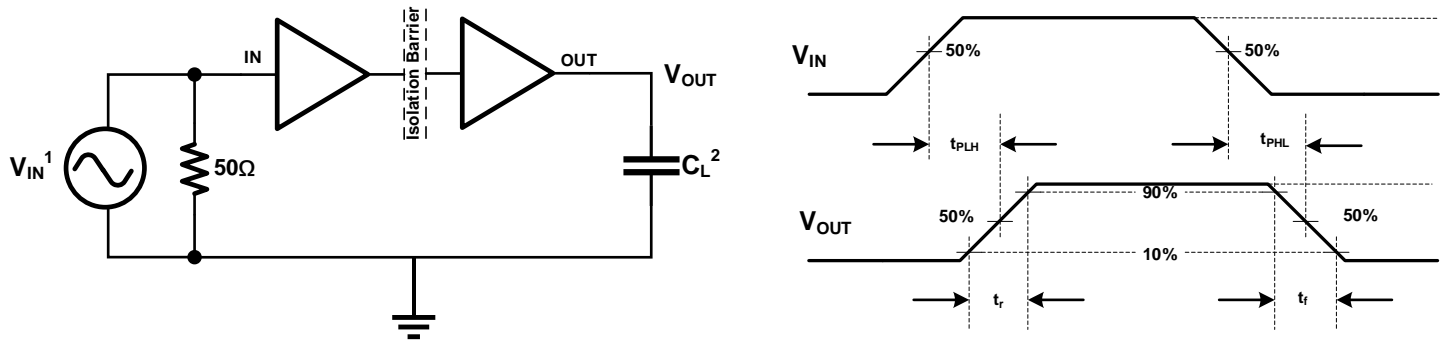


Figure 8-25. Efficiency vs. load current (I_{ISO}) at different ambient temperature, $V_{DD} = 3.3V$, $V_{ISO} = 3.3V$

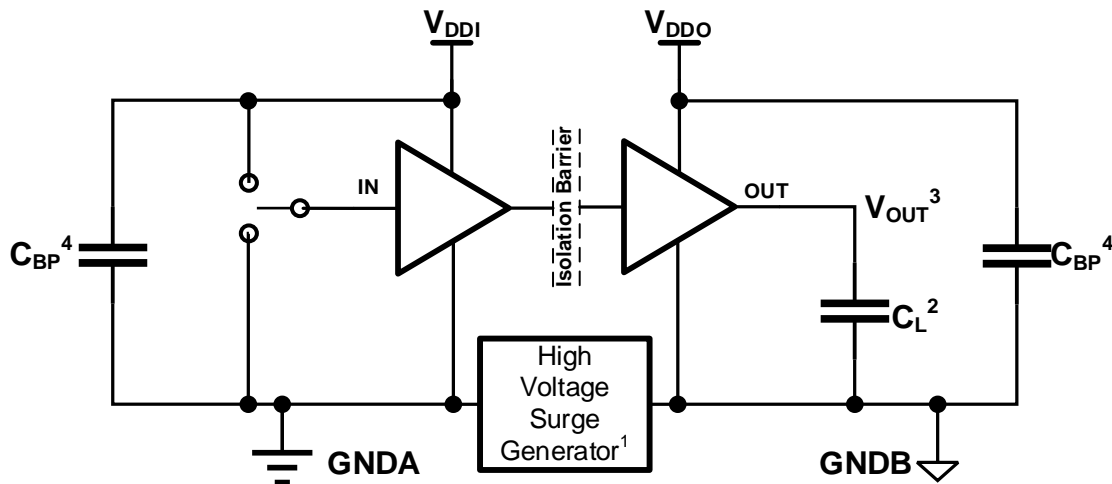
9 Parameter Measurement Information



Notes:

1. A square wave generator provide V_{IN} input signal with characteristics of frequency $\leq 100\text{kHz}$, 50% duty cycle, $t_r \leq 3\text{ns}$, $t_f \leq 3\text{ns}$, $Z_{out} = 50\Omega$. At the input, 50Ω resistor is required to terminate input generator signal. It is not needed in actual application.
2. $C_L = 15\text{pF}$, includes external circuit (instrumentation and fixture etc.) capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

Figure 9-1. Timing Characteristics Test Circuit and Voltage Waveforms



Notes:

1. The High Voltage Surge Generator generates repetitive high voltage surges with $> 1.5\text{kV}$ amplitude, rise time $< 10\text{ns}$ and fall time $< 10\text{ns}$, to reach common-mode transient noise with $> 150\text{kV}/\mu\text{s}$ slew rate.
2. $C_L = 15\text{pF}$ and includes external circuit (instrumentation and fixture etc.) capacitance.
3. Pass-fail criteria: the output must remain stable.
4. C_{BP} ($0.1 \sim 1\mu\text{F}$) is bypass capacitance.

Figure 9-2. Common-Mode Transient Immunity Test Circuit

10 Detailed Description

10.1 Overview

The CA-IS36xx family of devices integrates most of the components needed for digital isolation application, a high-efficiency, low-emissions isolated DC-DC converter with internal transformer and high-speed isolated data channels, into a single, compact SOIC package. This results an efficient and compact fully integrated solution that complies with EMI requirements and makes system level design as easy as possible.

The CA-IS36xx family of devices offers dual-channel and four-channel digital galvanic isolators using Chipanalog's full differential capacitive isolation technology. These devices have an ON-OFF keying (OOK) modulation scheme to transfer digital signals across the SiO₂ based isolation barrier between circuits with different power domains. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the another digital state. The receiver demodulates the signal and recovery input signal at output through a buffer stage. With this OOK architecture, CA-IS36xx family of devices build a robust data transmission path between different power domains, without any special start-up initialization requirements. These devices also incorporate advanced full differential techniques to maximize the CMTI performance and minimize the radiated emissions due to the high frequency carrier and I/O buffer switching.

The internal DC-DC converter uses switched mode operation and proprietary PWM feedback circuit techniques to provide high efficiency and low radiated emissions. Undervoltage lockout (UVLO) with hysteresis is integrated on the V_{DD} supply which ensures robust system performance under noisy conditions. An integrated soft-start mechanism ensures controlled inrush current and avoids any overshoot on the output during power up.

10.2 Functional Block Diagram

The functional block diagram of CA-IS36xx devices is shown in Figure 10-1. The simplified functional block diagram of a typical signal isolation channel and a conceptual OOK operation waveform are shown in Figure 10-2 and Figure 10-3. Each channel of the CA-IS36xx is unidirectional, only passes data in one direction as indicated in the functional diagram and operates independently with guaranteed data rates from DC up to 150Mbps.

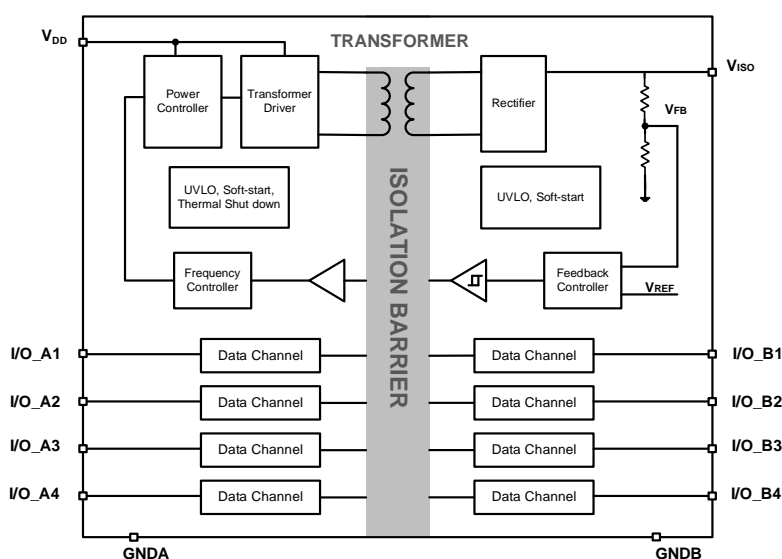


Figure 10-1. Functional Block Diagram of CA-IS36xx Devices

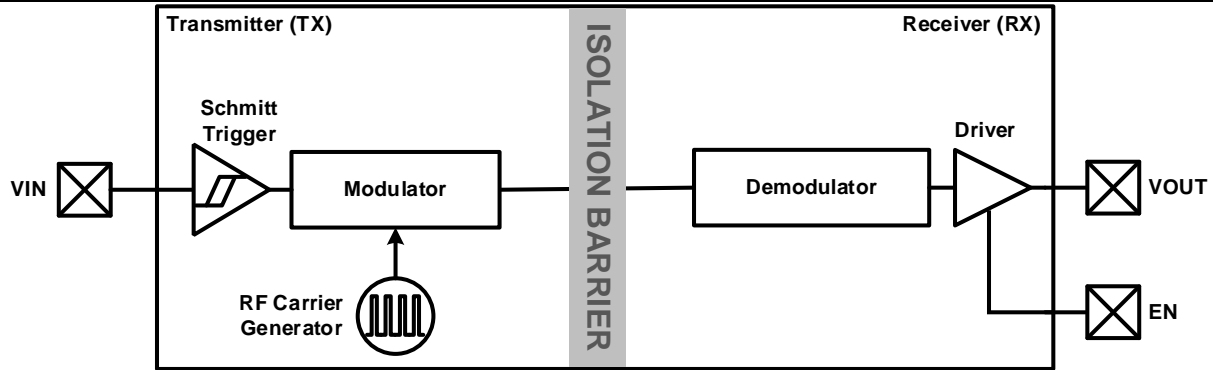


Figure 10-2. Functional Block Diagram of a Single Channel

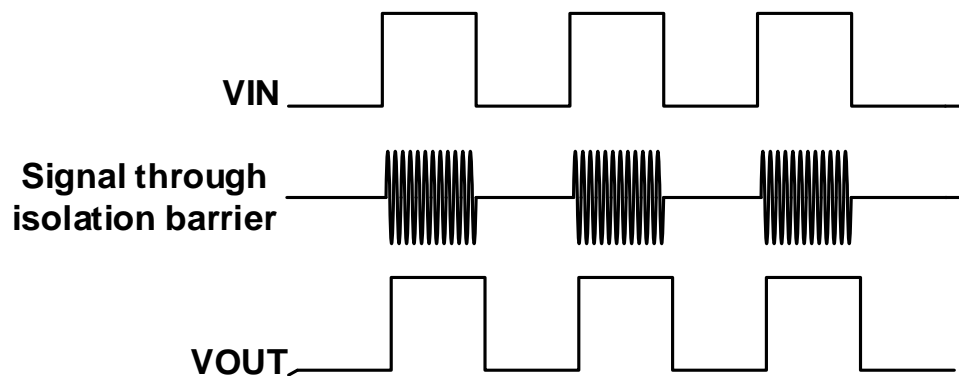


Figure 10-3. Operation Waveforms of a Single Channel

10.3 Undervoltage Protection

Below two tables show CA-IS36xxW and CA-IS36xxVW channel output in different supply configuration.

Table 10-1. CA-IS36xxW Channel Output in Different Supply Configuration

| V_{DD} (V) | A side OUTPUT | B side OUTPUT |
|--------------|---------------|---------------|
| PD | High-Z | High-Z |
| PU | Normal | Normal |

Table 10-2. CA-IS36xxVW Channel Output in Different Supply Configuration

| V_{DD} (V) | V_{DDL} (V) | A side OUTPUT | B side OUTPUT |
|--------------|---------------|---------------|---------------|
| PD | PD | High-Z | High-Z |
| PD | PU | High-Z | High-Z |
| PU | PD | High-Z | Normal |
| PU | PU | Normal | Normal |

Note: PU = Power up ($V_{DD/L} \geq V_{DD}(UVLO+)$); PD = Power down ($V_{DD/L} \leq V_{DD}(UVLO-)$)

10.4 Isolated Supply Output

The integrated isolated DC-DC converter based on PWM control structure provides up to 650mW of isolated power and different output voltage configurations. The V_{DD} supply is provided to the primary of power controller that switches the power stage connected to the integrated high-Q transformer. The output voltage V_{ISO} is monitored and a PWM signal based on feedback information is conveyed to the supply primary side through a dedicated isolation channel, the PWM duty cycle of the

primary switching stage is adjusted accordingly. Power is transferred to the secondary side of transformer, internal rectified and regulated to either 3.3 V or 5 V, depending on the SEL pin status, see Table 10-3 for the supply configurations of CA-IS36xx devices. The maximum output current from V_{ISO} is shown as Table 10-4. Note that the I_{ISO} value in Table 10-4 is the maximum output current at +25°C. With the increase of temperature, especially when the temperature exceeds +85°C, the maximum load current will be decreased, see more details from Figure 8-11. to Figure 8-16.

Table 10-3. Supply Configuration

| SEL INPUT | V_{DD} | V_{ISO} |
|-----------------------------|--------------------|-------------------|
| Shorted to V_{ISO} | 5 V | 5V |
| Shorted to GNDB or floating | 5 V | 3.3V |
| Shorted to GNDB or floating | 3.3 V ¹ | 3.3V ² |

Notes:

- $V_{DD} = 3.3$ V, SEL shorted to V_{ISO} (essentially $V_{ISO} = 5$ V) is not recommended.
- The SEL pin has a weak pull-down internally. However, for $V_{ISO} = 3.3$ V, the SEL pin should be connected to the GNDB externally, especially in the noisy system.

Table 10-4. Maximum Output Current of V_{ISO} @ $T_A = 25^\circ\text{C}$

| Supply Voltage V_{DD} (V) | V_{ISO} (V) | Part Number | Data Rate (bps) | I_{ISO} (mA) |
|-----------------------------|---------------|---|-----------------|----------------|
| 4.5~5.5 | 5V or 3.3V | CA-IS36xx | <1M | 130 |
| 3.15~3.6 | 3.3V | | | 75 |
| 4.5~5.5 | 5V or 3.3V | CA-IS3644LW/CA-IS3644LVW/CA-IS3644HW/CA-IS3644HVW | 100M | 120 |
| 3.15~3.6 | 3.3V | | | 65 |
| 4.5~5.5 | 5V or 3.3V | CA-IS3621LW/CA-IS3643LW/CA-IS3643LVW/CA-IS3643HW/CA-IS3643HVW | 100M | 110 |
| 3.15~3.6 | 3.3V | | | 60 |
| 4.5~5.5 | 5V or 3.3V | CA-IS3620LW/CA-IS3642LW/CA-IS3642LVW/CA-IS3642HW/CA-IS3642HVW | 100M | 100 |
| 3.15~3.6 | 3.3V | | | 55 |
| 4.5~5.5 | 5V or 3.3V | CA-IS3641LW/CA-IS3641LVW/ CA-IS3641HW/CA-IS3641HVW | 100M | 90 |
| 3.15~3.6 | 3.3V | | | 50 |
| 4.5~5.5 | 5V or 3.3V | CA-IS3640LW/CA-IS3640LVW/CA-IS3640HW/CA-IS3640HVW | 100M | 80 |
| 3.15~3.6 | 3.3V | | | 45 |

10.5 Operation Modes

Table 10-5 lists the operation modes for the CA-IS36xx devices.

Table 10-5. Operation Mode¹

| V_{DD}^1 | INPUT(V_{IX}) | OUTPUT (V_{OX}) | OPERATION |
|------------|-------------------|---------------------------|--|
| PU | H | H | Normal operation mode: A channel output follows the logic state of its input. |
| | L | L | |
| | Open | Default | Default output mode: When input V_{IX} is open, the corresponding channel output goes to its default logic state. Default is <i>High</i> for CA-IS36xxH and Low for CA-IS36xxL. |
| PD | X | Undetermined ² | If the V_{DD} is unpowered, a channel output is undetermined. |

Notes:

- V_{DD} = Input-side power supply; PU = Powered up ($V_{DD} \geq 3.15$ V); PD = Powered down ($V_{DD} \leq 2.0$ V); X = Don't care; H = High level; L = Low level.
- The outputs are in undetermined state when $V_{DD} < 2.0$ V.

11 Application and Implementation

11.1 Typical Application

The CA-IS36xx isolation ICs provide complete galvanic isolation between two power domains, protecting circuits from high common-mode transients and faults, eliminating ground loops. In many applications, digital isolators are replacing optocouplers because they can reduce the power requirements and take up less board space while offering the same isolation capability. Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the CA-IS36xx devices integrated both signal and power isolation, only require few external bypass capacitors to operate, and save an external isolated power supply on side-B, help designers to simplify system-level design and reduces board area. These devices are ideal for applications that have limited board space and desire more integration. Figure 11-1 shows typical operating circuit of the CA-IS3642; Figure 11-2 is the typical schematic of CA-IS3641 in SPI isolation application.

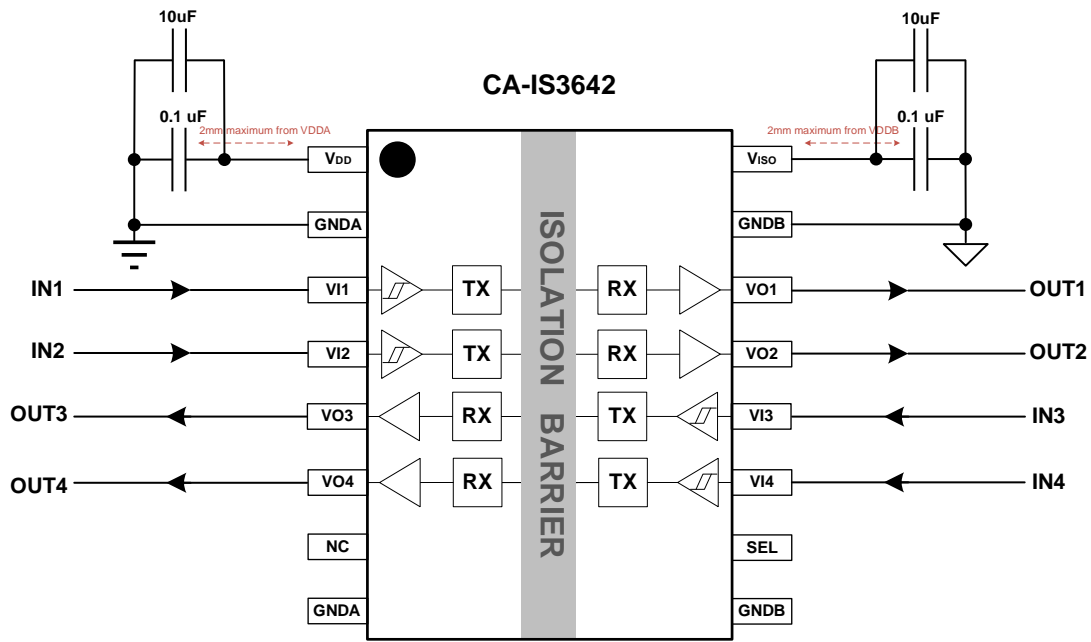


Figure 11-1. Typical Application Circuit of CA-IS3642

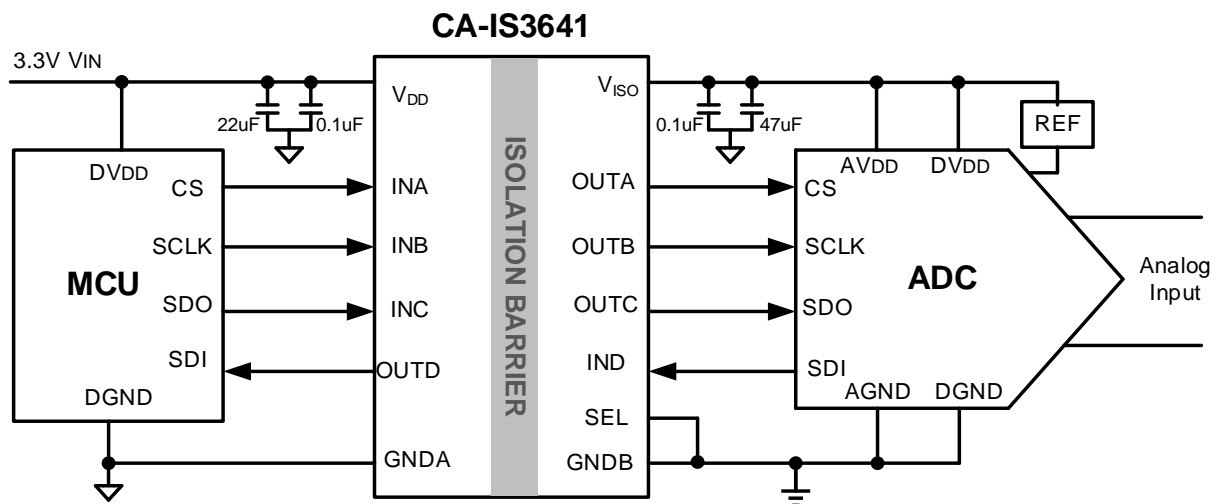


Figure 11-2. CA-IS3641 provides SPI isolation and isolated power for ADC

The CA-IS36xx family devices do not require special power supply sequencing. The logic levels are set independently on either side by V_{DD}/V_{DDL} (side-A) and V_{ISO} (side-B). When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, MCU or FPGA), and a data converter or a line transceivers etc., regardless of the interface type or standard. The PCB designer should follow some critical recommendations in order to get the best performance from the design, especially for the high-speed operating digital circuit boards, see PCB Layout Guidelines section.

11.2 PCB Layout Guidelines

High switching frequencies and large peak currents make PCB layout very important for the digital isolators with internal DC-DC converter. Good PCB design minimizes excessive electromagnetic interference (EMI) and voltage gradients in the ground plane to avoid instability and regulation errors. Even with the high level of integration design, users may fail to achieve specified operation with a poor layout. So careful PCB layout is critical to achieve clean and stable operation.

In the typical application circuit, the input capacitors (0.1 μ F and a bulk capacitor with at least 10 μ F capacitance) between V_{DD} and GNDA are required to reduce the peak current drawn from input power source and reduce the switching noise, increase internal DC-DC efficiency. For the supply input capacitors, choose the ceramic capacitor because they have the lowest equivalent series resistance (ESR), smallest size, and lowest cost. For most applications, we recommend to use at least 0.1 μ F and a 10 μ F ceramic capacitors with X5R or X7R temperature characteristic. When operating at a V_{DD} voltage close to the UVLO threshold, more input capacitance may be required to keep the input voltage ripple from tripping the UVLO protection. Also, these low-ESR ceramic bypass capacitors must be placed as close to the chip pads as possible. For the logic supply input, we recommend to use a 1 μ F ceramic capacitors with X5R or X7R between V_{DDL} pin and GNDA. On side-B, the supply output capacitors between V_{ISO} and GNDB are required as well to keep the output voltage ripple small and to ensure loop stability. These bypass capacitors must have low impedance at the switching frequency. Ceramic capacitors are recommended due to their small size and low ESR. Make sure the capacitor does not degrade its capacitance significantly over temperature and DC bias. Although a 10 μ F capacitor is adequate, higher decoupling capacitors (such as 47 μ F) on both V_{DD} and V_{ISO} pins to the respective grounds are strongly recommended to provide better noise and ripple performance, because of very-high current flowing through the V_{DD} and V_{ISO} supplies.

Place the supply input capacitors, supply output capacitors, and the CA-IS36xx IC on the same PCB layer. The paths must be wide and short to minimize inductance, also any via holes must be avoided on these paths. See Figure 11-3 recommended components placement for the PCB layout.

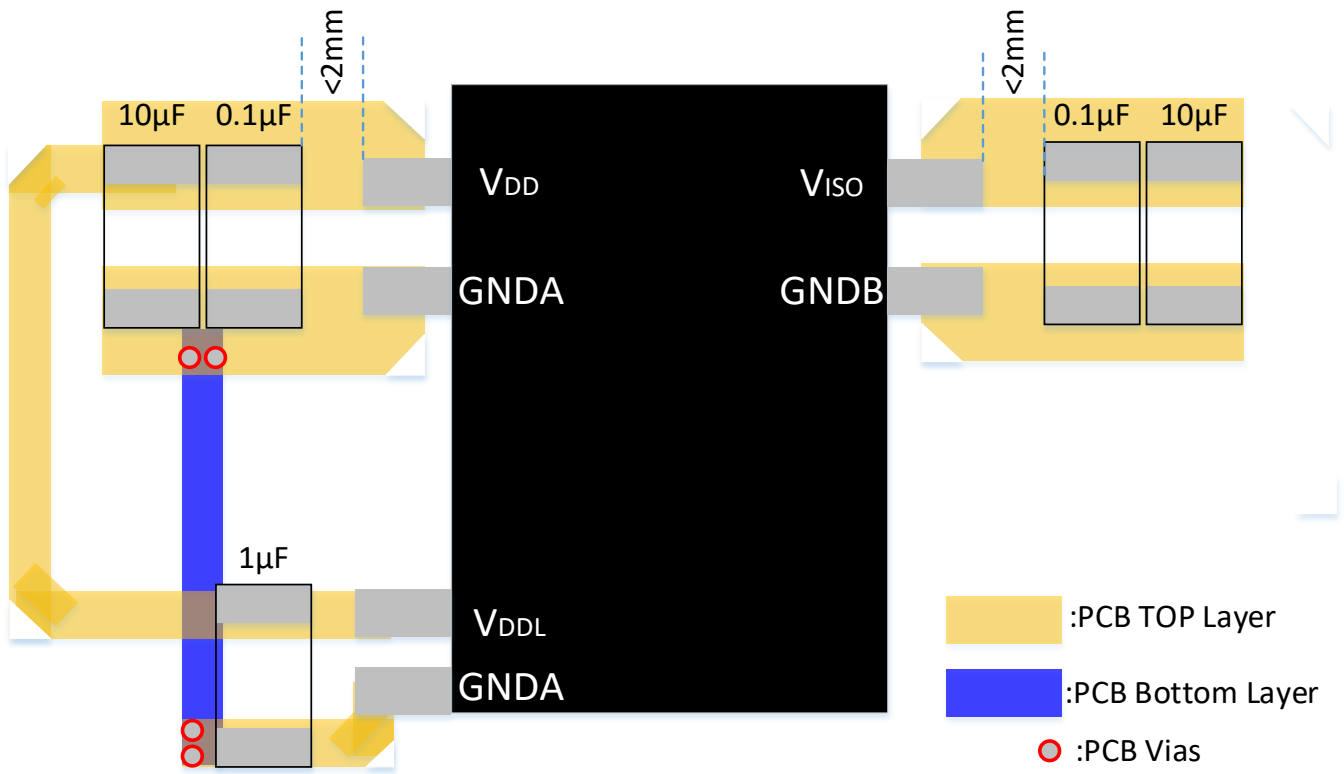
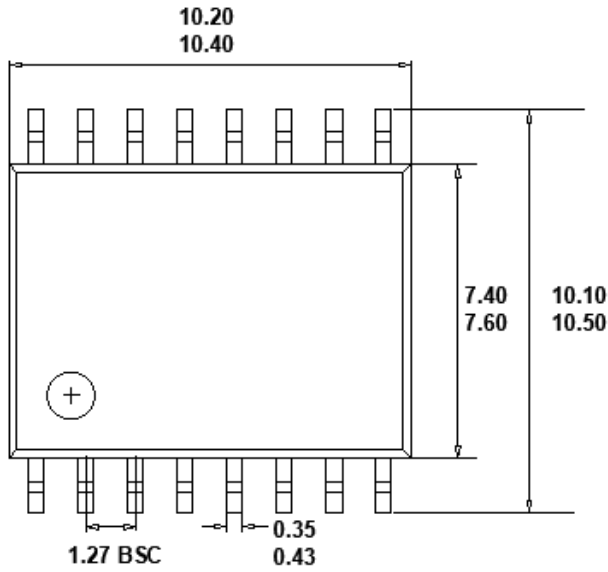


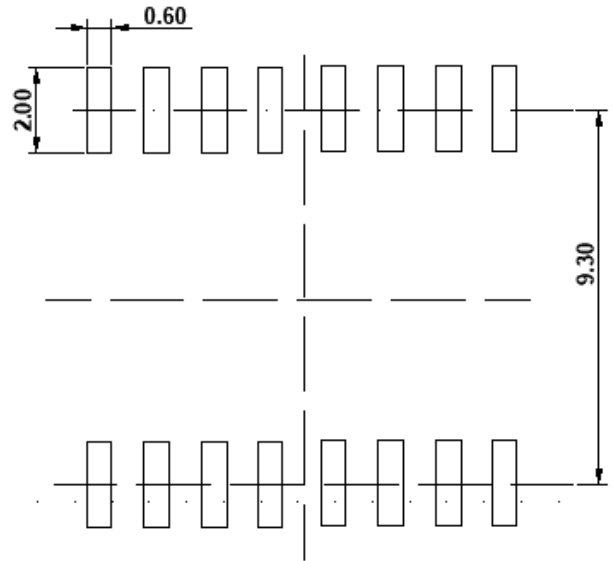
Figure 11-3. Recommended PCB layout for CA-IS36xxVW with $V_{DDL} = V_{DD}$

12 Package Information

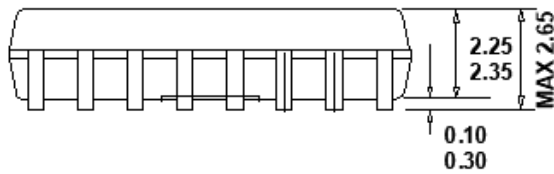
16-Pin Wide Body SOIC Package Outline



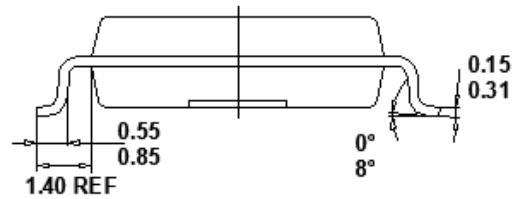
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



LEFT SIDE VIEW

Note:

1. All dimensions are in millimeters, angles are in degrees.

13 Soldering Temperature (reflow) Profile

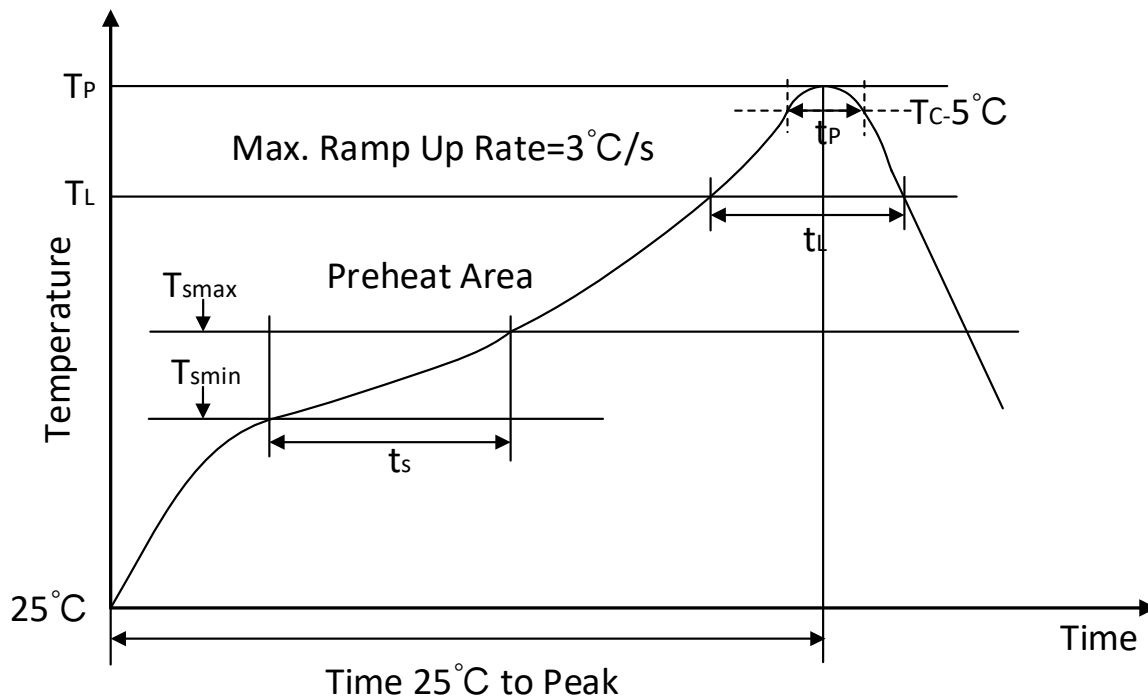


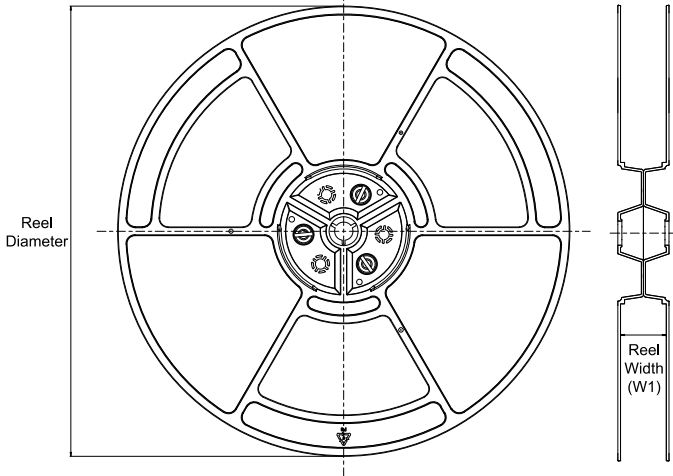
Figure 13-1. Soldering Temperature (reflow) Profile

Table 13-1. Soldering Temperature Parameter

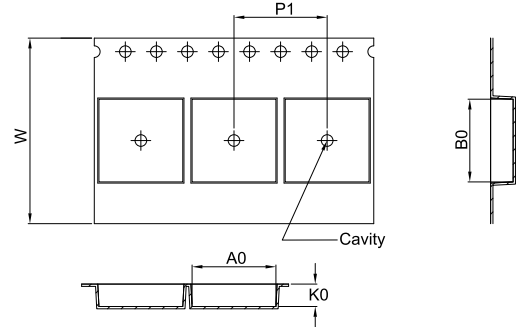
| Profile Feature | Pb-Free Assembly |
|---|-------------------|
| Average ramp-up rate(217 °C to Peak) | 3°C /second max |
| Time of Preheat temp(from 150 °C to 200 °C) | 60-120 second |
| Time to be maintained above 217 °C | 60-150 second |
| Peak temperature | 260 +5/-0 °C |
| Time within 5 °C of actual peak temp | 30 second |
| Ramp-down rate | 6 °C /second max. |
| Time from 25°C to peak temp | 8 minutes max |

14 Tape and Reel Information

REEL DIMENSIONS

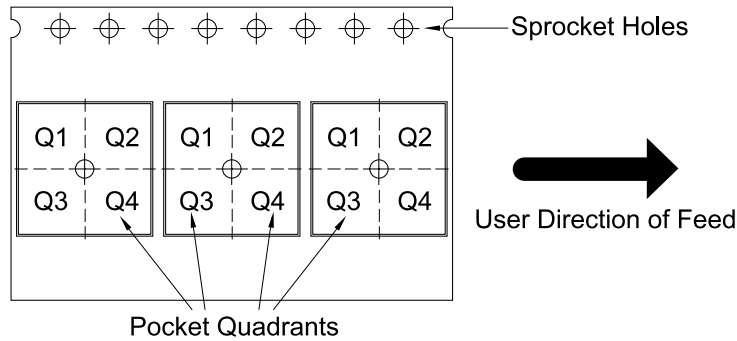


TAPE DIMENSIONS



| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



| evic | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CA-IS3620LW | SOIC | W | 16 | 1000 | 330 | 16.4 | 10.9 | 10.7 | 3.2 | 12.0 | 16.0 | Q1 |
| CA-IS3621LW | SOIC | W | 16 | 1000 | 330 | 16.4 | 10.9 | 10.7 | 3.2 | 12.0 | 16.0 | Q1 |
| CA-IS3640LW | SOIC | W | 16 | 1000 | 330 | 16.4 | 10.9 | 10.7 | 3.2 | 12.0 | 16.0 | Q1 |
| CA-IS3640HW | SOIC | W | 16 | 1000 | 330 | 16.4 | 10.9 | 10.7 | 3.2 | 12.0 | 16.0 | Q1 |
| CA-IS3641LW | SOIC | W | 16 | 1000 | 330 | 16.4 | 10.9 | 10.7 | 3.2 | 12.0 | 16.0 | Q1 |
| CA-IS3640HW | SOIC | W | 16 | 1000 | 330 | 16.4 | 10.9 | 10.7 | 3.2 | 12.0 | 16.0 | Q1 |
| CA-IS3642LW | SOIC | W | 16 | 1000 | 330 | 16.4 | 10.9 | 10.7 | 3.2 | 12.0 | 16.0 | Q1 |
| CA-IS3642HW | SOIC | W | 16 | 1000 | 330 | 16.4 | 10.9 | 10.7 | 3.2 | 12.0 | 16.0 | Q1 |
| CA-IS3643LW | SOIC | W | 16 | 1000 | 330 | 16.4 | 10.9 | 10.7 | 3.2 | 12.0 | 16.0 | Q1 |
| CA-IS3643HW | SOIC | W | 16 | 1000 | 330 | 16.4 | 10.9 | 10.7 | 3.2 | 12.0 | 16.0 | Q1 |
| CA-IS3644LW | SOIC | W | 16 | 1000 | 330 | 16.4 | 10.9 | 10.7 | 3.2 | 12.0 | 16.0 | Q1 |
| CA-IS3644HW | SOIC | W | 16 | 1000 | 330 | 16.4 | 10.9 | 10.7 | 3.2 | 12.0 | 16.0 | Q1 |
| CA-IS3640LVW | SOIC | W | 16 | 1000 | 330 | 16.4 | 10.9 | 10.7 | 3.2 | 12.0 | 16.0 | Q1 |
| CA-IS3640HVW | SOIC | W | 16 | 1000 | 330 | 16.4 | 10.9 | 10.7 | 3.2 | 12.0 | 16.0 | Q1 |
| CA-IS3641LVW | SOIC | W | 16 | 1000 | 330 | 16.4 | 10.9 | 10.7 | 3.2 | 12.0 | 16.0 | Q1 |
| CA-IS3640HVW | SOIC | W | 16 | 1000 | 330 | 16.4 | 10.9 | 10.7 | 3.2 | 12.0 | 16.0 | Q1 |
| CA-IS3642LVW | SOIC | W | 16 | 1000 | 330 | 16.4 | 10.9 | 10.7 | 3.2 | 12.0 | 16.0 | Q1 |
| CA-IS3642HVW | SOIC | W | 16 | 1000 | 330 | 16.4 | 10.9 | 10.7 | 3.2 | 12.0 | 16.0 | Q1 |
| CA-IS3643LVW | SOIC | W | 16 | 1000 | 330 | 16.4 | 10.9 | 10.7 | 3.2 | 12.0 | 16.0 | Q1 |
| CA-IS3643HVW | SOIC | W | 16 | 1000 | 330 | 16.4 | 10.9 | 10.7 | 3.2 | 12.0 | 16.0 | Q1 |
| CA-IS3644LVW | SOIC | W | 16 | 1000 | 330 | 16.4 | 10.9 | 10.7 | 3.2 | 12.0 | 16.0 | Q1 |
| CA-IS3644HVW | SOIC | W | 16 | 1000 | 330 | 16.4 | 10.9 | 10.7 | 3.2 | 12.0 | 16.0 | Q1 |

15 IMPORTANT NOTICE

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