1 Overview

STC8H series of microcontrollers do not require an external crystal oscillator and external reset circuit. They are 8051 microcontrollers with the properties of strong anti-interference/ultra low price/high speed/low power consumption. Under the same operating frequency, STC8H series of microcontrollers are about 12 times faster (11.2 ~ 13.2 times) than traditional 8051. To execute all 111 instructions in sequence, the STC8H series microcontroller only needs 147 clocks, while the traditional 8051 requires 1944 clocks. STC8H series of microcontrollers are single clock/machine cycle (1T) microcontrollers produced by STC. They are new generation 8051 microcontrollers with wide voltage/high speed / high reliability / low power consumption / strong antistatic / strong anti-interference, and is super encrypted. The instruction codes are fully compatible with traditional 8051.

High precision of ±0.3% @+25℃ RC clock is integrated in MCU with −1.38% to +1.42% temperature drift under the temperature range of -40℃ to +85℃, and 0.88% to +1.05% temperature drift under temperature range from -20℃ to +65℃. The frequency of RC clock can be set from 4MHz to 35MHz when programming a MCU using ISP. Note: The maximum frequency must be controlled below 35MHz when the temperature range is -40℃ to + 85℃. Moreover, high reliable reset circuit is integrated in MCU with 4 levels optional reset threshold voltages, which can be selected when user programming using ISP. So, external expensive crystal and the external reset circuit can be eliminated completely.

There are three optional clock sources inside the MCU, internal high precision IRC which can be adjusted appropriately, internal 32KHz low speed IRC, external 4MHz~33MHz oscillator or external clock signal. The clock source can be freely chosen in user codes. After the clock source is selected, it may be 8-bit divided and then be supplied to the CPU and the peripherals, such as timers, UARTs, SPI, and so on.

Two low power modes are provided in MCU, the IDLE mode and the STOP mode. In IDLE mode, MCU stops clocking CPU, CPU stops executing instructions without clock, while all peripherals are still working. At this moment, the power consumption is about 1.0mA at 6MHz working frequency. The STOP mode is the power off or power-down mode. At this momont, the main clock stops, CPU and all peripherals stop working, and the power consumption can be reduced to about 0.6uA when VCC is 5.0V, 0.4uA when VCC is 3.3V.

The Power-down mode can be woke-up by one of the following interrupts: INT0(P3.2), INT1(P3.3), INT2(P3.6), INT3(P3.7), INT4(P3.0), T0(P3.4), T1(P3.5), T2(P1.2), T3(P0.4), T4(P0.6), RXD(P3.0/P3.6/P1.6/P4.3), RXD2(P1.0/P4.6), RXD3(P0.0/P5.0), RXD4(P0.2/P5.2), I2C_SDA(P1.4/P2.4/P3.3), Comparator, LVD, Power-down wake-up timer.

Rich digital peripherals and analog peripherals are provided in MCU, including UARTs, timers, enhanced PWMs and I2C, SPI, USB, ultra-high speed ADC and comparator, which can meet the requirements of users when designing a product.

The enhanced dual data pointers are integrated in the STC8H series of microcontrollers. Using user codes, the function of automatic increasing or decreasing of data pointer and automatic switching of two sets of data pointers can be realized.

Products Line	I/O	UART	Timers	ADC	Enhanced PWM	CMP	SPI	I2C	USB	MDU16	LED DRV	Touch Key	RTC	I/O Int.	Color LCM	LCD DRV	DMA
STC8H1K08 family	17	2	3	$9_{CH}*10_{B}$	●	●	●	●									
STC8H1K28 family	29	2	5	$12_{CH}*10_{B}$	●	●	●	●									
STC8H3K64S4 family	45	4	5	$12_{CH}*12_{B}$	●	●	●	●		●				●			
STC8H3K64S2 family	45	2	5	$12_{CH}*12_{B}$	●	●	●	●		●				●			
STC8H8K64U family Version A	60	4	5	$15_{CH}*12_{B}$	●	●	●	●	●	●							
STC8H8K64U familyVersion B	60	4	5	$15_{CH}*12_{B}$	●	●	●	●	●	●			●	●	●		●
STC8H2K64T family	44	4	5	$15_{CH}*12_{B}$	●	●	●	●		●	●	●	●	●			
STC8H4K64TLR family	44	4	5	$15_{CH}*12_{B}$	●	●	●	●		●	●	●	●	●	●		●
STC8H4K64TLCD family	60	4	5	$15_{CH}*12_{B}$	●	●	●	●		●		●	●	●	●	●	●
STC8H4K64LCD family	61	4	5	$15_{CH}*12_{B}$	●	●	●	●		●			●	●	●	●	●
STC8H1K08TR family	16	2	3	$15_{CH}*12_{B}$	●	●	●	●		●		●	●	●	●		●

2 Features

2.1 STC8H1K28-36I-LQFP32/QFN32 family

2.1.1 Features

- **Selection and price (No external crystal and external reset required)**

MCU	Operating voltage（V)	Flash Code Memory (100 thousand times) (Byte)	Idata, Internal DATA RAM(Byte)	Xdata, Internal extended SRAM (Byte)	Enhanced Dual DPTR increasing or decreasing	EEPROM 100 thousand times) (Byte)	Maximum I/O Lines	Traditional I/O interrupt(INT0/INT1/INT2/INT3/INT4) (can wake-up CPU)	UARTs which can wake-up CPU	SPI	I²C which can wake-up CPU	Timers/Counters (T0-T4 Pin Can wake-up CPU)	16-bit advanced PWM timer with Complementary symmetrical dead-time	Power-down Wake-up timer	12-channels high speed ADC (8 PWM can be used as 8 DACs)	Comparator (May be used as ADC to detect external power-down)	Internal LVD interrupt (can wake-up CPU)	Watch-dog Timer	Internal high reliable reset circuit with 4 level optional reset threshold voltage	Internal high precision Clock (adjustbal under 35MHz)	Clock output and Reset	Program encrypted transmission (Anti-blocking)	Password can be set for next update	Support RS485 download	Support software USB download directly	Online debugging	Price & Package		Main product supply information
																											LQFP32<9mm*9mm>	QFN32<4mm*4mm>	
STC8H1K16	1.9-5.5	16K	256	1K	2	12K	29	Y	2	Y	Y	5	8	Y	10bit	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y			Available
STC8H1K24	1.9-5.5	24K	256	1K	2	4K	29	Y	2	Y	Y	5	8	Y	10bit	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y			
STC8H1K28	1.9-5.5	28K	256	1K	2	IAP	29	Y	2	Y	Y	5	8	Y	10bit	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y			
STC8H1K33	1.9-5.5	33K	256	1K	2	IAP	29	Y	2	Y	Y	5	8	Y	10bit	Y	Y	Y	Y	Y	Y	Y	Y	Y	-	-	√	√	

- **Core**
  - ✓ Ultra-high speed 8051 Core with single clock per machine cycle, which is called 1T and the speed is about 12 times faster than traditional 8051
  - ✓ Fully compatible instruction set with traditional 8051
  - ✓ 19 interrupt sources and 4 interrupt priority levels
  - ✓ Online debugging is supported
- **Operating voltage**
  - ✓ 1.9V～5.5V
- **Operating temperature**
  - ✓ -40℃~85℃(The chip is -40℃～125℃ process. Please refer to the description of the electrical characteristics chapter for applications beyond the temperature range)
- **Flash memory**
  - ✓ Up to 33Kbytes of Flash memory to be used for storing user code
  - ✓ Configurable size EEPROM, 512bytes single page for being erased, which can be repeatedly erased more than 100 thousand times.

- ✓ In-System-Programming, ISP in short, can be used to update the application code. No dedicated programmer is needed.
- ✓ Online debugging with single chip is supported, and no dedicated emulator is needed. The number of breakpoints is unlimited theoratically.

➢ **SRAM**

- ✓ 128 bytes internal direct access RAM (DATA, use keyword *data* to declare in C language program)
- ✓ 128 bytes internal indirect access RAM(IDATA, use keyword *idata* to declare in C language program)
- ✓ 1024 bytes internal extended RAM (internal XDATA, use keyword *xdata* to declare in C language program)

➢ **Clock**

- ✓ Internal high precise RC clock (IRC for short, ranges from 4MHz to 38MHz), adjustable while ISP and can be divided to lower frequency by user software, 100KHz for instance.
  - ✓ Error:±0.3% (at the temperature 25℃)
  - ✓ -1.35%～+1.30% temperature drift (at the temperature range of -40℃ to +85℃)
  - ✓ -0.76%～+0.98% temperature drift (at the temperature range of -20℃ to 65℃)
- ✓ Internal 32KHz low speed IRC with large error
- ✓ External 4MHz~33MHz oscillator or external clock
  The three clock sources above can be selected freely by user code.

➢ **Reset**

- ✓ Hardware reset
  - ✓ Power-on reset. (**Effective when the chip does not enable the low voltage reset function**)
  - ✓ Reset by reset pin. The default function of P5.4 is the I/O port. P5.4 pin can be set as the reset pin while ISP download. (**Note: When the P5.4 pin is set as the reset pin, the reset level is low**.)
  - ✓ Watch dog timer reset
  - ✓ Low voltage detection reset. 4 low voltage detection levels are provided, 2.0V, 2.4V, 2.7V, 3.0V.
- ✓ Software reset
  - ✓ Writing the reset trigger register using software

➢ **Interrupts**

- ✓ 19 interrupt sources: INT0(Supports rising edge and falling edge interrupt), INT1(Supports rising edge and falling edge interrupt), INT2(Supports falling edge interrupt only), INT3(Supports falling edge interrupt only), INT4(Supports falling edge interrupt only), timer0, timer1, timer2, timer3, timer4, UART1, UART2, ADC, LVD, SPI, I^2C, Comparator, PWMA,PWMB
- ✓ 4 interrupt priority levels
- ✓ Interrupts that can wake up the CPU in clock stop mode: INT0(P3.2), INT1(P3.3), INT2(P3.6), INT3(P3.7), INT4(P3.0), T0(P3.4), T1(P3.5), T2(P1.2), T3(P0.4), T4(P0.6), RXD(P3.0/P3.6/P1.6), RXD2(P1.0), I2C_SDA(P1.4/P2.4/P3.3), Comparator, LVD, Power-down wake-up timer.

➢ **Digital peripherals**

- ✓ 5 16-bit timers: timer0, timer1, timer2, timer3, timer4, where the mode 3 of timer 0 has the Non-Maskable Interrupt (NMI in short) function. Mode 0 of timer 0 and timer 1 is 16-bit Auto-reload mode.
- ✓ 2 high speed UARTs: UART1, UART2, whose maximum baudrate may be FOSC/4.
- ✓ 8 channels/2 groups of enhanced PWMs, which can realize control signals with dead time, and support external fault detection function. In addition, it also supports 16-bit timers, 8 external interrupts, 8 external captures and pulse width measurement functions.
- ✓ SPI: Master mode, slave mode or master/slave automatic switch mode are supported.
- ✓ I^2C: Master mode or slave mode are supported.

➢ **Analog peripherals**

- ✓ 12 channels (channel 0 to channel 11) ultra high speed ADC which supports 10-bit precision. The maximum speed can be 500K(Half a million ADC conversions per second)
- ✓ Channel 15 of ADC is used to test the internal reference voltage. (The default internal reference voltage is 1.19V when the chip is shipped)
- ✓ A set of comparator (the CMP+ port and all ADC input ports can be selected as the positive terminal of the comparator, so the comparator can be used as a multi-channel comparator for time division multiplexing)
- ✓ DAC: 8 channels advanced PWM timer can be used as 8 channels DAC

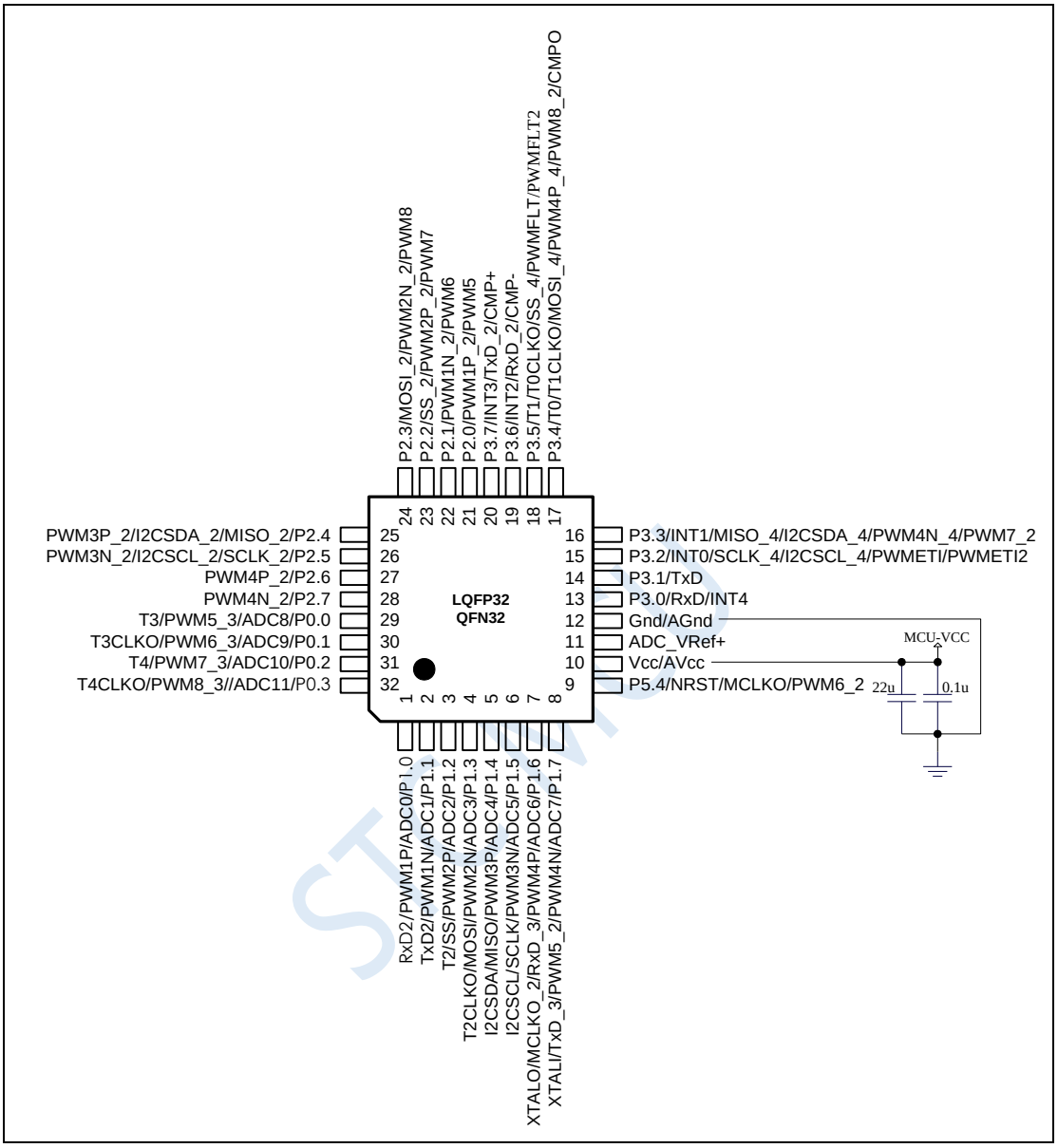
➢ **GPIO**

- ✓ Up to 29 GPIOs: P0.0~P0.3, P1.0~P1.7, P2.0~P2.7, P3.0~P3.7, P5.4
- ✓ 4 modes for all GPIOs: quasi_bidirectional mode, push-pull outputmode, open drain mode, high-impedance input mode
- ✓ Except for P3.0 and P3.1, all other I/O ports are in a high-impedance state after power-on. User must configure the I/O ports mode before using them. In addition, the internal 4K pull-up resistor of every I/O can be enabled independently.

➢ **Package**

- ✓ LQFP32 <9mm*9mm>, QFN32 <4mm*4mm>

2.1.2 Pinouts



Note:
1. ADC's external reference power supply pin ADC_VRef+ must not be floating. It must be connected to an external reference power supply or directly connected to Vcc.
2. If USB download is not required, P3.0/P3.1/P3.2 cannot be at low level at the same time when the chip is reset.

The download steps using ISP and notes are the same as the circumstances in 2.1.2.

Note:

1. **Except for P3.0 and P3.1, all other I/O ports are in high-impedance input state after power-on. User must set the I/O port mode firstly when using I/O.**
2. **All I/O ports can be set to quasi-bidirectional port mode, strong push-pull output mode, open-drain output mode or high-impedance input mode. In addition, each I/O can independently enable the internal 4K pull-up resistor.**
3. **When P5.4 is enabled as the reset pin, the reset level is low.**

2.1.3 Pin descriptions

Pin number		name	type	description
LQFP32/QFN32				
1		P1.0	I/O	Standard IO port
		RxD2	I	Serial input of UART2
		ADC0	I	ADC analog input 0
		PWM1P	I/O	Capture of external signal/Positive of PWMA pulse output
2		P1.1	I/O	Standard IO port
		TxD2	O	Serial Transmit pin of UART 2
		ADC1	I	ADC analog input 1
		PWM1N	I/O	Capture of external signal/Negative of PWMA pulse output
3		P1.2	I/O	Standard IO port
		ADC2	I	ADC analog input 2
		SS	I/O	Slave selection of SPI
		T2	I	Timer2 external input
		PWM2P	I/O	Capture of external signal/ Positive of PWMB pulse output
4		P1.3	I/O	Standard IO port
		ADC3	I	ADC analog input 3
		MOSI	I/O	Master Output/Slave Input of SPI
		T2CLKO	O	Clock out of timer 2
		PWM2N	I/O	Capture of external signal/ Negative of PWMB pulse output
5		P1.4	I/O	Standard IO port
		ADC4	I	ADC analog input 4
		MISO	I/O	Serial Clock line of I2C
		SDA	I/O	Serial data line of I2C
		PWM3P	I/O	Capture of external signal/ Positive of PWM3 pulse output
6		P1.5	I/O	Standard IO port
		ADC5	I	ADC analog input 5
		SCLK	I/O	Serial Clock of SPI
		SCL	I/O	Serial Clock line of I2C
		PWM3N	I/O	Capture of external signal/ Negative of PWM3 pulse output
7		P1.6	I/O	Standard IO port
		ADC6	I	ADC analog input 6
		RxD_3	I	Serial input of UART1
		PWM4P	I/O	Capture of external signal/ Positive of PWM4 pulse output
		MCLKO_2	O	Main clock output
		XTALO	O	Output pin of external crystal oscillator
8		P1.7	I/O	Standard IO port
		ADC7	I	ADC analog input 7
		TxD_3	O	Serial Transmit pin of UART 1
		PWM4N	I/O	Capture of external signal/Negative of PWM4 pulse output
		PWM5_2	I/O	Capture of external signal/ Positive of PWM5 pulse output
		XTALI	I	External crystal/external clock input pin

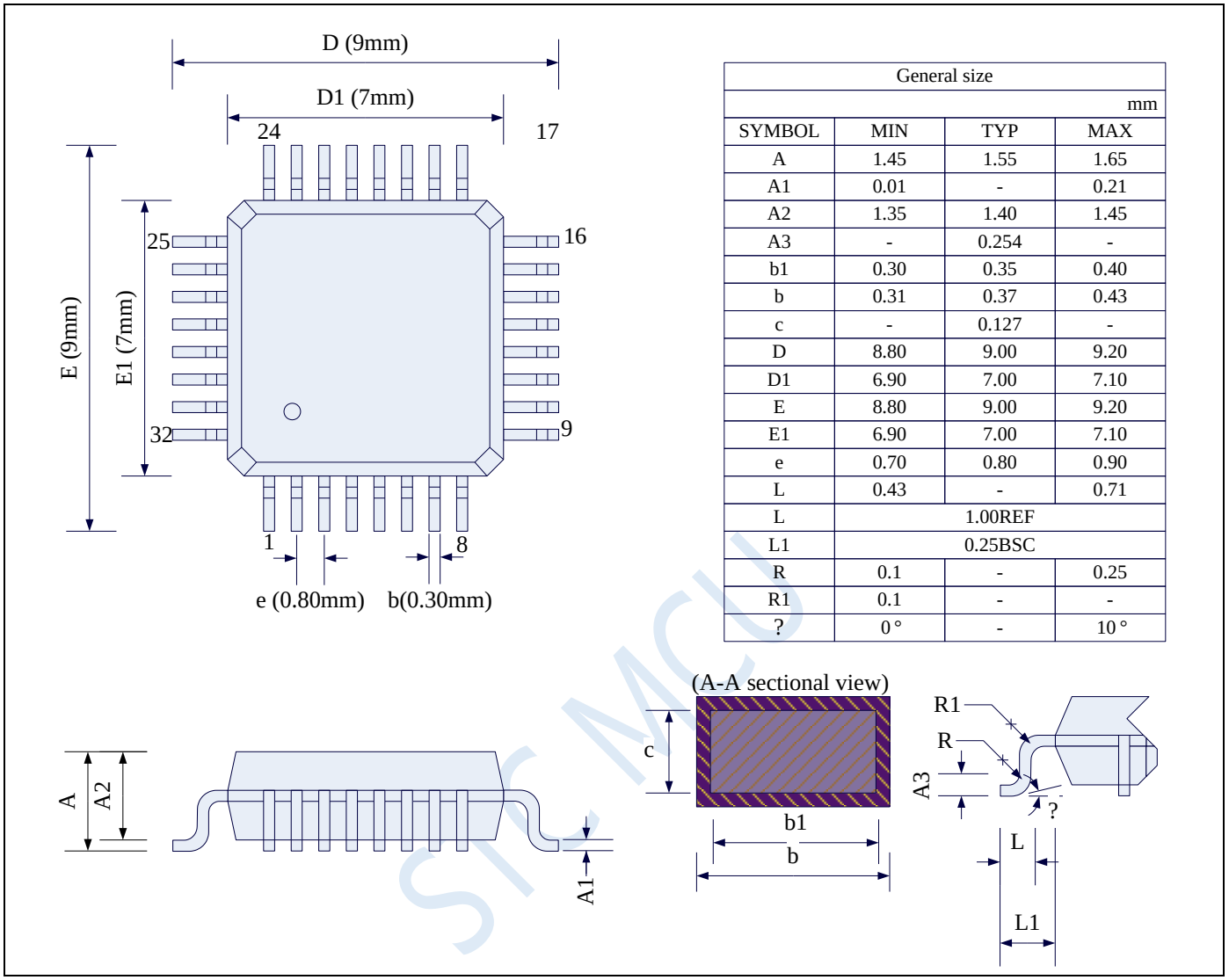
Pin number LQFP32/QFN32		name	type	description
9		P5.4	I/O	Standard IO port
		RST	I	Reset pin
		MCLKO	O	Main clock output
		PWM6_2	I/O	Capture of external signal/ Positive of PWM6 pulse output
10		Vcc	Vcc	Power Supply
		AVcc	Vcc	Power Supply for ADC
11		ADC_VREF+	I	Reference voltage pin of ADC.It can be directly connected to the VCC of the MCU if the requirement is not high
12		Gnd	Gnd	Ground
		AGnd	Gnd	ADC Ground
13		P3.0	I/O	Standard IO port
		RxD	I	Serial input of UART1
		INT4	I	External interrupt 4
14		P3.1	I/O	Standard IO port
		TxD	O	Serial Transmit pin of UART 1
15		P3.2	I/O	Standard IO port
		INT0	I	External interrupt 0
		SCLK_4	I/O	Serial Clock of SPI
		SCL_4	I/O	Serial Clock line of I2C
		PWMETI	I	PWM external trigger input pin
		PWMETI2	I	PWM external trigger input pin 2
16		P3.3	I/O	Standard IO port
		INT1	I	External interrupt 1
		MISO_4	I/O	Serial Clock line of I2C
		SDA_4	I/O	Serial data line of I2C
		PWM4N_4	I/O	Capture of external signal/ Negative of PWM4 pulse output
		PWM7_2	I/O	Capture of external signal/ Positive of PWM7 pulse output
17		P3.4	I/O	Standard IO port
		T0	I	Timer0 external input
		T1CLKO	O	Clock out of timer 1
		MOSI_4	I/O	Master Output/Slave Input of SPI
		PWM4P_4	I/O	Capture of external signal/ Positive of PWM4 pulse output
		PWM8_2	I/O	Capture of external signal/ Positive of PWM8 pulse output
		CMPO	O	Comparator output
18		P3.5	I/O	Standard IO port
		T1	I	Timer1 external input
		T0CLKO	O	Clock out of timer 0
		SS_4	I/O	Slave selection of SPI
		PWMFLT	I	PWMA external anomaly detection pin
		PWMFLT2	I	PWMB external anomaly detection pin
19		P3.6	I/O	Standard IO port
		INT2	I	External interrupt 2
		RxD_2	I	Serial input of UART1
		CMP-	I	Comparator negative input
20		P3.7	I/O	Standard IO port
		INT3	I	External interrupt 3
		TxD_2	O	Serial Transmit pin of UART 1
		CMP+	I	Comparator positive input

Pin number		name	type	description
LQFP32/QFN32				
21		P2.0	I/O	Standard IO port
		PWM1P_2	I/O	Capture of external signal/ Positive of PWMA pulse output
		PWM5	I/O	Capture of external signal/ Positive of PWM5 pulse output
22		P2.1	I/O	Standard IO port
		PWM1N_2	I/O	Capture of external signal/ Negative of PWMA pulse output
		PWM6	I/O	Capture of external signal/ Positive of PWM6 pulse output
23		P2.2	I/O	Standard IO port
		PWM2P_2	I/O	Capture of external signal/ Positive of PWMB pulse output
		PWM7	I/O	Capture of external signal/ Positive of PWM7 pulse output
		SS_2	I/O	Slave selection of SPI
24		P2.3	I/O	Standard IO port
		PWM2N_2	I/O	Capture of external signal/ Negative of PWMB pulse output
		PWM8	I/O	Capture of external signal/ Positive of PWM8 pulse output
		MOSI_2	I/O	Master Output/Slave Input of SPI
25		P2.4	I/O	Standard IO port
		PWM3P_2	I/O	Capture of external signal/ Positive of PWM3 pulse output
		MISO_2	I/O	Serial Clock line of I2C
		SDA_2	I/O	Serial data line of I2C
26		P2.5	I/O	Standard IO port
		PWM3N_2	I/O	Capture of external signal/ Negative of PWM3 pulse output
		SCLK_2	I/O	Serial Clock of SPI
		SCL_2	I/O	Serial Clock line of I2C
27		P2.6	I/O	Standard IO port
		PWM4P_2	I/O	Capture of external signal/ Positive of PWM4 pulse output
28		P2.7	I/O	Standard IO port
		PWM4N_2	I/O	Capture of external signal/ Negative of PWM4 pulse output
29		P0.0	I/O	Standard IO port
		ADC8	I	ADC analog input 8
		RxD3	I	Serial input of UART3
		T3	I	Timer3 external input
		PWM5_3	I/O	Capture of external signal/ Positive of PWM5 pulse output
30		P0.1	I/O	Standard IO port
		ADC9	I	ADC analog input 9
		TxD3	O	Serial Transmit pin of UART 3
		T3CLKO	O	Clock out of timer 3
		PWM6_3	I/O	Capture of external signal/ Positive of PWM6 pulse output

Pin number		name	type	description
LQFP32/QFN32				
31		P0.2	I/O	Standard IO port
		ADC10	I	ADC analog input 10
		RxD4	I	Serial input of UART4
		T4	I	Timer4 external input
		PWM7_3	I/O	Capture of external signal/ Positive of PWM7 pulse output
32		P0.3	I/O	Standard IO port
		ADC11	I	ADC analog input 11
		TxD4	O	Serial Transmit pin of UART 4
		T4CLKO	O	Clock out of timer 4
		PWM8_3	I/O	Capture of external signal/ Positive of PWM8 pulse output

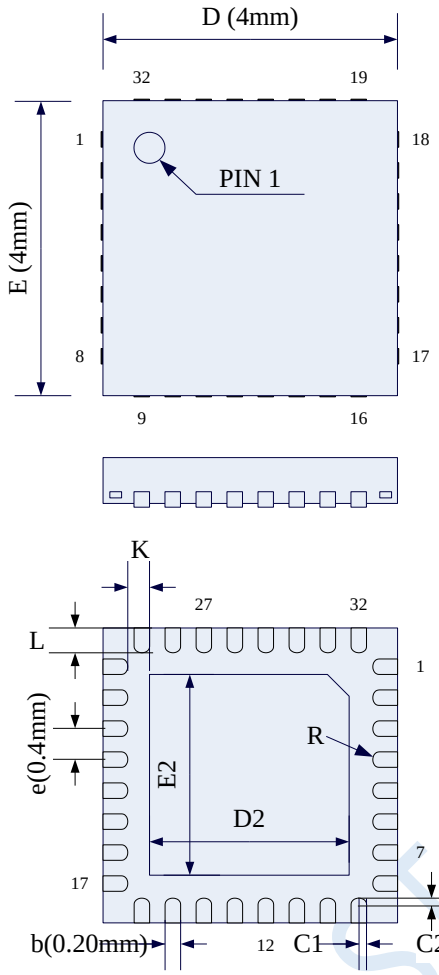
3 Package Dimensions

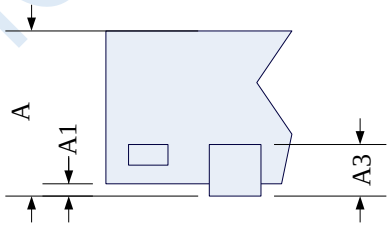
3.1 LQFP32 Package mechanical data（9mm*9mm）



General size			
			mm
SYMBOL	MIN	TYP	MAX
A	1.45	1.55	1.65
A1	0.01	-	0.21
A2	1.35	1.40	1.45
A3	-	0.254	-
b1	0.30	0.35	0.40
b	0.31	0.37	0.43
c	-	0.127	-
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.70	0.80	0.90
L	0.43	-	0.71
L	1.00REF		
L1	0.25BSC		
R	0.1	-	0.25
R1	0.1	-	-
?	0 °	-	10 °

3.2 QFN32 Package mechanical data（4mm*4mm）





General size			
			mm
SYMBOL	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2	0.50	0.55	0.60
A3	-	0.20REF	-
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
e	0.30	0.40	0.50
L	0.35	0.40	0.45
K	0.25REF		
R	0.09	-	-
C1	-	0.16	-
C2	-	0.16	-

The back metal sheet (substrate) of STC's existing DFN8 packaged chip is not grounded inside the chip. It can be grounded or ungrounded on the user's PCB board, which will not affect the performance of the chip.

3.3 Naming rules of STC8 family