Data Sheet

BIT3105

High Efficiency ZVS CCFL Controller

Version : 1.01

Notice

All information contained in this document is subject to change without notice.

Features:

- **4.5V ~ 13.2V Operation Voltage**
- **Full Bridge Fixed Frequency ZVS Control**
- **High Efficiency**
- **Built-in PWM Dimming**
- **Programmable Soft Start**
- **Programmable Striking Voltage**
- **Open Lamp Latched Protection**
- **ON/OFF Control with 0 Standby Current**
- **High Voltage Rail-to-Rail Totem Pole Output**
- **Low Power CMOS Process**

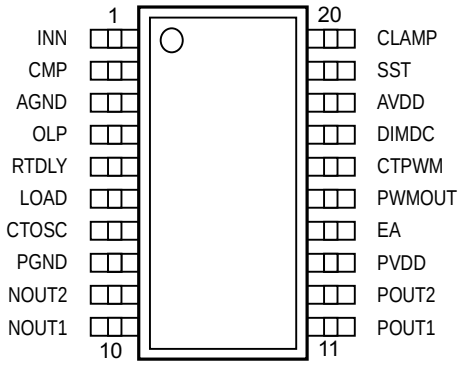
Applications:

- **Cold Cathode Fluorescent Lamps system**
- **Notebook Computer**
- **LCD Monitor**
- **LCD PC**
- **LCD TV**
- **Personal Digital Assistants**
- **Video Phone/ Door Phone**
- **Navigation Devices (GPS Equipment)**
- **ATM/ Financial Terminal**
- **POS Terminal**

Recommended Operating Condition:

Supply Voltage……4.5 ~ 13.2 V
Operating Ambient Temperature……...0 ~ 70 ℃
Operating Frequency……30K ~ 250K Hz

Pin Layout:

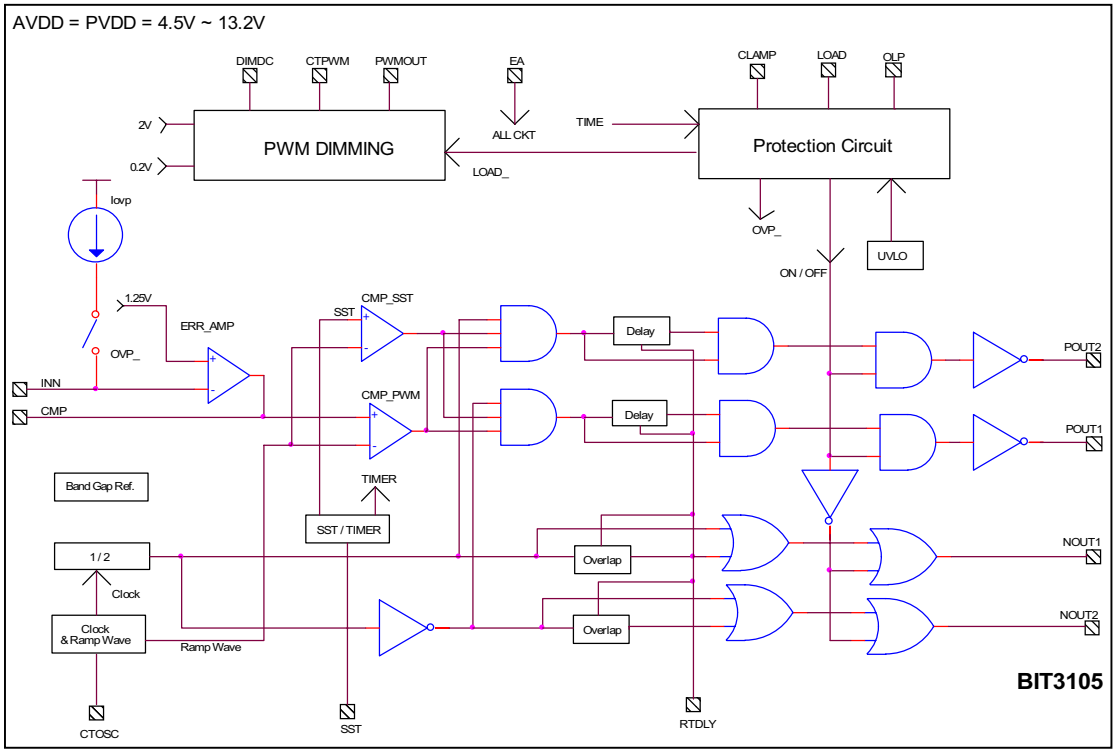


General Description:

BIT3105 integrated circuit provides the essential features for controlling CCFL in a small 20-pin package. New developed full bridge ZVS configuration provides a symmetry AC output and more than 85% efficiency to make it especially suitable for LCD backlight application. BIT3105 senses the lamp current directly to enable the built-in PWM dimming circuit. If no current flow into the lamp, BIT3105 provides a continuous AC output to ensure the successful ignition. PWM dimming is started immediately while the lamp is ignited. The up to 13.2V high voltage CMOS process is used to design the output drivers to drive PMOS switches directly without any boost circuitry. BIT3105 includes a clamped striking voltage control loop to protect the transformer while ignition and the lamp current monitor provides the most reliable latched open lamp protection.

Patent pending.

Functional Block Diagram:



Functional Description:

UVLO: The under-voltage-look-out circuit turns the output driver off when supply voltage drops too low. System is shut down with all outputs turned to logic high level.

Band Gap Reference: An internal trimmed band-gap reference provides a high accuracy, supply and temperature insensitive voltage reference. By amplifying or dividing this voltage can generate the other required reference voltages.

Over Voltage Clamping: while a > 2.0V is sensed by CLAMP pin, an internal ~ 100uA current will flow into the INN pin, the inverting input of the error amplifier, to clamp the output.

On/Off Function: The EA pin provides the function to turn on and off the output without shut down the supply voltage. An internal 80K ohm pull-low resistor is connected here. All the output are forced to logic high when the chip is turned off.

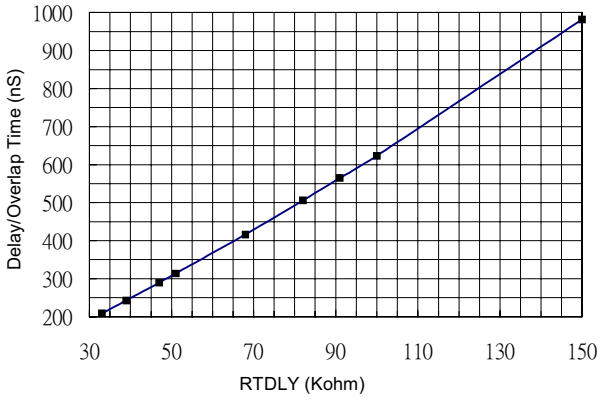
Set the Delay/Overlap Time for ZVS Operation: The period made by internal delay generation circuitry is dependent on the resistance of R_{RTDLY}. The CCFL control needs timing circuitry, the required period of ignition, lamp operation frequency, PWM dimming PWM frequency and the delay/overlap for ZVS switching. The resistor R_{RTDLY} connected to pin

$$I_{REF} = \frac{1.25V}{R_{RTDLY}} \text{.....(1)}$$

RTDLY and the internal 1.25V determines a reference current I_{REF} with

The Delay/Overlap time T_{Delay} and $T_{Overlap}$, in typical case 5V 25°C, can be found as bellow:

RTDLY vs. Delay/Overlap Time



Set the Lamp Operation Frequency: The lamp operating frequency can be calculated as equation (2)

$$F_{LAMP} = \frac{1.3}{R_{RTDLY} \times C_{TOSC}} \text{.....(2)}$$

For a 45KHz operation CCFL, if an 82K ohm resistor is used as the delay resistor, a 350pF capacitor can be connected to the pin CTOSC.

The Soft Start and Open Lamp Protection: A current mirror provides current of ~ 0.02 x I_{REF} to charge the SST pin. The slope of Soft Start $\Delta V/\Delta T$ can be determined by

$$\frac{\Delta V}{\Delta T} = \frac{0.025}{R_{RTDLY} \times C_{SST}} \text{.....(3)}$$

The required time of ignition is set as equation (4)

$$T_{STRIKE} = 50 \times R_{RTDLY} \times C_{SST} \text{.....(4)}$$

In the case of R_{RTDLY}= 82K ohm, a 0.47 uF capacitor connected on the SST pin can set a ~ 2 seconds period for striking the lamp. If the voltage of OLP pin is less than 300mV after this period, the latched protection function will latch the output drivers to PVDD high level. The latched situation can be released while the system is re-started.

PWM Dimming: To compare the input of DIMDC pin with the 0.2V ~ 2.0V ramp wave makes the PWM pulses for PWM dimming. The internal ramp wave generator generates a ramp wave with peak=2V and valley=0.2V. Its frequency can be set as equation (5)

$$F_{PWM} = \frac{0.347}{R_{RTDLY} \times C_{CTDIM}} \text{.....(5)}$$

The output of PWMOUT pin is pulled to VDD to make the dark portion of the CCFL output burst and the floating state to make the bright portion. A less than 0.2V input on DIMDC pin will make the PWMOUT be floating to obtain 100% brightness. BIT3105 provides the continuous high voltage to strike the lamp. It sends the PWM pulses while the voltage of OLP pin > 300mV.

Open Lamp Indicator: The LOAD pin is an open drain transistor, which is controlled by OLP pin input. If the input of OLP pin is less than 300mV. A pulled to GND output is generated through LOAD pin. LOAD pin is floating during normal operation.

Pin Description:

Pin	Names	I/O	Description
1	INN	I	The inverting input of error amplifier.
2	CMP	O	Output of error amplifier.
3	AGND	I/O	The ground pin of analog control circuitry.
4	OLP	I	Lamp current detection pin, the open lamp situation is detected if a less than 300mV input is sensed.
5	RTDLY	I/O	An external resistor connected here to make a reference current which determines the delay and overlap time of the output drivers. With this reference current and different capacitors the period of soft start, the frequency of PWM dimming and the operation frequency of the lamp can be set.
6	LOAD	I/O	This node becomes floating if the OLP pin has detected the lamp current. A ~ 200ohm pull to GND switch is connected here while the input of OLP is less than 300mV.
7	CTOSC	I/O	With the RTDLY pin made reference current and an external capacitor connected here can set the lamp operation frequency.
8	PGND	I/O	The ground pin of output drivers.
9	NOUT2	O	The number 2 output driver that driving the NMOSFET switch.
10	NOUT1	O	The number 1 output driver that driving the NMOSFET switch.
11	POUT1	O	The number 1 output driver that driving the PMOSFET switch.
12	POUT2	O	The number 2 output driver that driving the PMOSFET switch.
13	PVDD	I	The power supply of 4.0V ~ 13.2V high voltage output drivers.
14	EA	I	ON/OFF control pin, 1.4V threshold with an internal 80K ± 15% ohm pull-low resistor.
15	PWMOUT	O	The output of PWM dimming. An ~ 200ohm pull to AVDD switch can be used to turn off the lamp with low frequency.
16	CTPWM	I/O	Open lamp protection. A < 300 mV input will latch off the whole system. OLP senses a < 300mV input will cause the whole system latched off.
17	DIMDC	I	PWM dimming control input. A PWM output comes out by comparing this DC input and the triangle wave that is generated by CTPWM.
18	AVDD	I	The power supply of analog voltage control circuitry.
19	SST	O	With the RTDLY pin made reference current and an external capacitor connected here can set the required period of ignition and the slop of soft start. The open lamp protection function will be enabled after this node is charged to > 2.5V.
20	CLAMP	I	Over voltage clamping. If a > 2 V voltage is detected, a ~ 180uA current will flow into the INN pin to reduce the output of the error amplifier CMP to clamp the output voltage.

Absolute Ratings: *(if Ta=25℃)*

Parameter	Symbol	Ratings	Unit	Remarks
Control Supply Voltage	AVDD	-0.3~+ 15	V	Ta=25°C
Analog Ground	AGND	±0.3	V	
Driver Supply Voltage	PVDD	-0.3~+ 15	V	
Driver Ground	PGND	±0.3	V	
Input Voltage		-0.3~ VDD+0.3	V	
Power Dissipation		800	mW	
Operating Ambient Temperature	Ta	0~ +70	° C	
Operating Junction Temperature		+150	° C	
Storage Temperature		-55~+150	° C	

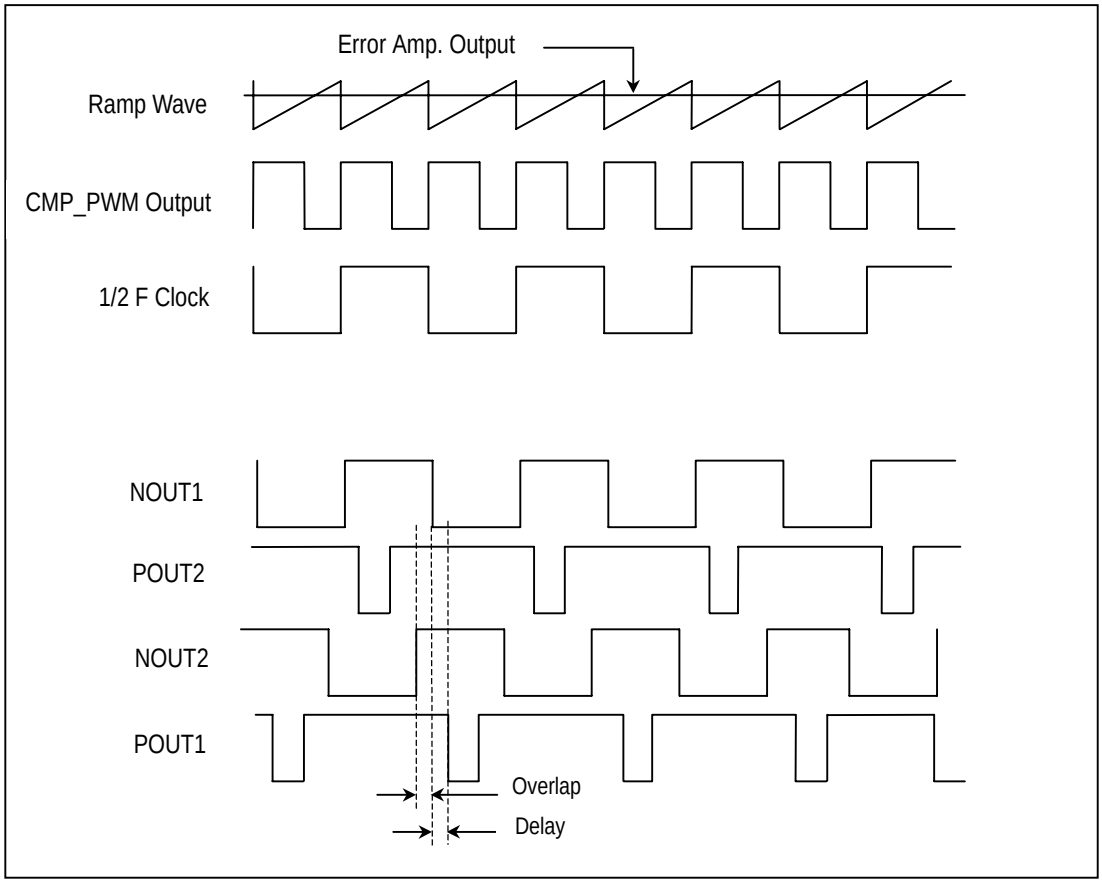
DC/AC Characteristics:

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Supply Voltages					
AVDD (note1)		4.0		13.2	V
PVDD (note1)		4.0		13.2	V
Chip Consumed Current	12V Supply Voltage Ta=25°C		2		mA
Reference Voltage					
Output voltage	Measure INN	1.2125	1.25	1.2875	V
Line regulation	VDD=4.5 ~13.2 V		2	20	mV
Under Voltage Look Out					
Positive Going Threshold	Ta=25°C Note4	3.8	4	4.2	V
Hysteresis		0.1	0.2	0.3	V
Ramp Wave Generator and Lamp Frequency					
Operating Frequency	Note2	50		250	KHz
Output peak			2.25		V
Output valley			0.45		V
Error Amplifier					
Input voltage	Note3	0.1		3	V
Open loop gain		60	80		dB
Unit gain band width		1	1.5		MHz
SST Soft Start and Open Lamp Enable					
Output current	VDD=12V, Ta=25°C		$25/R_{RTDLY}$		mA
Open Lamp Detection Enable			2.5		V
Open Lamp Protection					
OLP pin Open lamp detection lower threshold	VDD=12V, Ta=25°C Note 4		300		mV
Hysterisis			20		mV
Over Voltage Clamping					
CLAMP pin detection lower threshold	VDD=12V, Ta=25°C		2.0		V
Hysterisis			20		mV
INN pin driving current			100		uA
On/Off Function					
The threshold of EA pin	VDD=12V, Ta=25°C		1.4		V
Internal pulled low resistance			80K		Ω
PWM Dimming PWM Generator					
Ramp Wave Peak	VDD=12V, Ta=25°C		2.0		V
Ramp Wave Valley			0.2		V
PWM Frequency		10		100K	Hz
100 % Brightness Dimming Voltage on pin DIMDC				0.2	V
0 % Brightness Dimming Voltage on pin DIMDC		2			V
Pulled high resistance of Pin PWMOUT output for making the dark burst			200		Ω
Pin PWMOUT output for making the bright burst		Floating			
Output					
CMOS output impedance	(Note3, Note4)		50		Ω
Rising Time	VDD=5V, 1000pF(Note3, Note4)		110		ns
Falling Time			100		ns

Note 1. AVDD and PVDD must be set to an equal supply voltage VDD in typical application.
Note 2. The lamp operation frequency is the half of the ramp wave frequency.
Note 3. Only verified by simulation. Not 100% tested.
Note 4. The voltages of the output drivers are VDD in each off states.

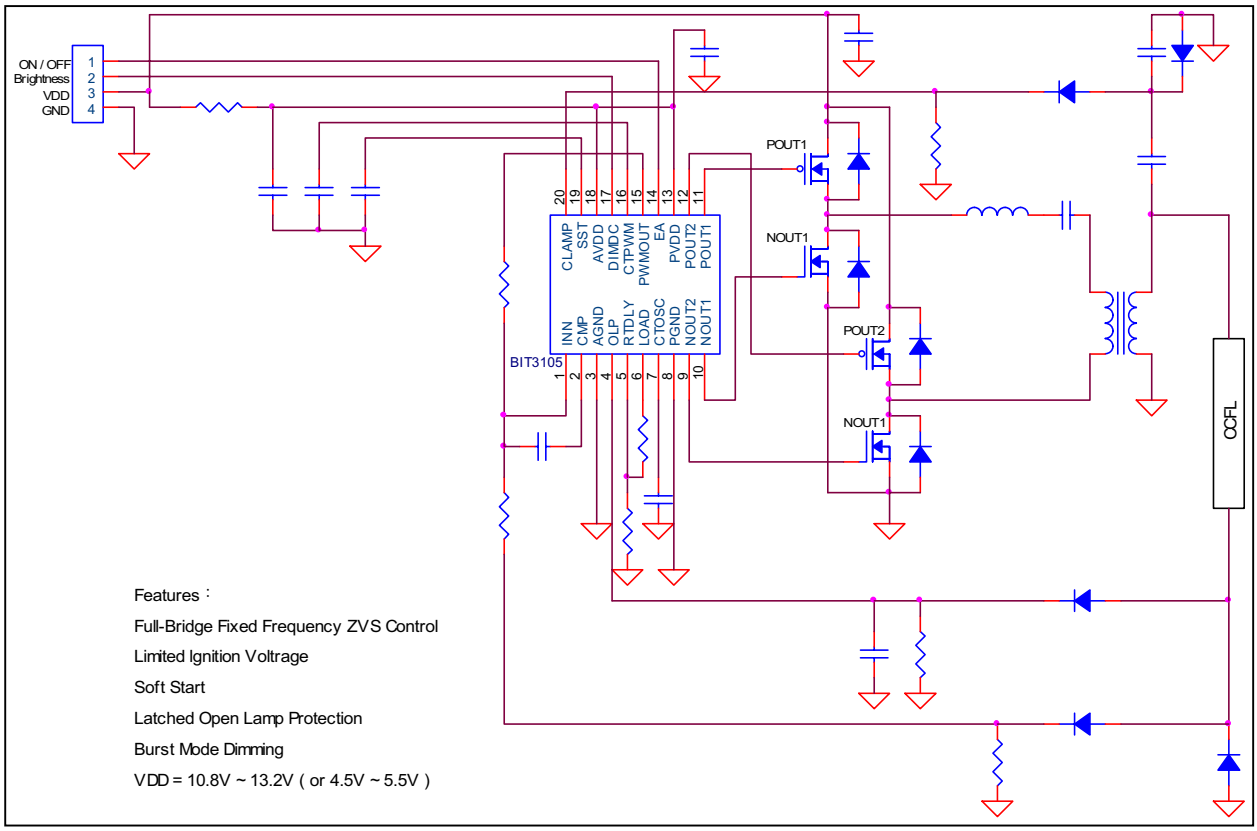
Timing Diagram

BIT3105 uses new developed fixed frequency full bridge driving methodology to drive CCFL. The low side switches; NMOSFETs are driven by fixed frequency and fixed; > 50% duty cycle signals. The high side switches; PMOSFETs are driven by fixed frequency PWM controlled signals. The detail timing relationship is shown as bellow:



If the lamp operation frequency is set to higher than resonant frequency of the LC tank, symmetry ZVS switching operation can be performed. A well-controlled delay and overlap timing relationship play the key role of this control scheme. It can be set through using proper resistor connected on RTDLY pin. (Patent pending)

Application Information:



A Typical application of BIT3105

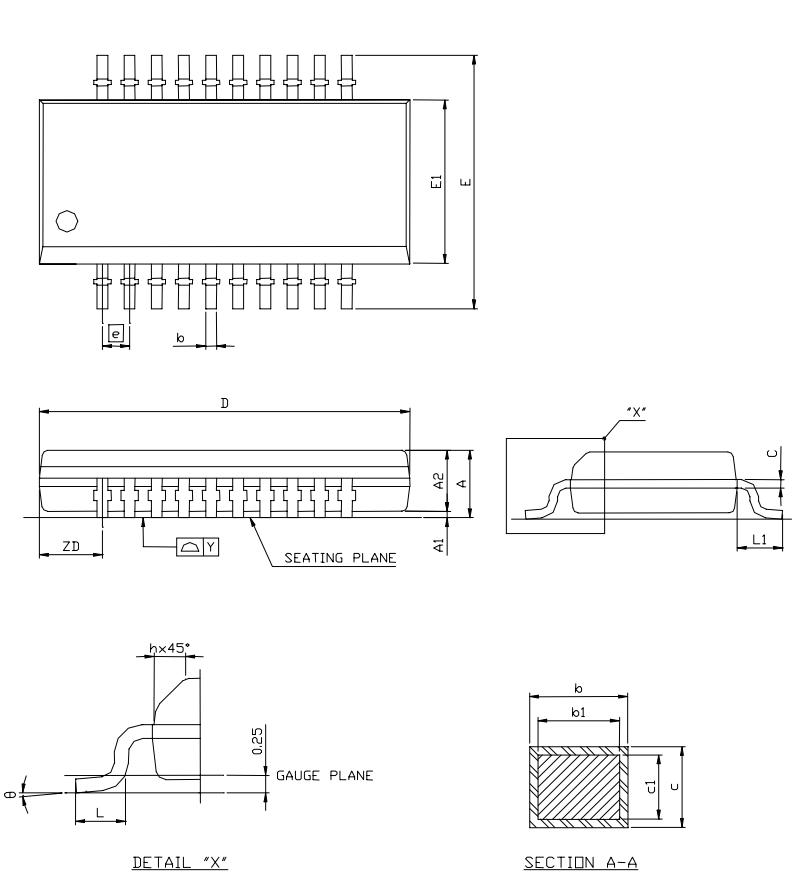
Order Information:

BIT3105-SSO

- **SSOP** type packing
- Part number
- Beyond Innovation Technology Co., Ltd.

Package Information :

SSOP type :



DETAIL "X"

SECTION A-A

SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	1.60	1.75	53	63	69
A1	0.10	0.15	0.25	4	6	10
A2			1.50			59
b	0.20	0.254	0.30	8	10	12
b1	0.20	0.254	0.28	8	10	11
c	0.18	0.203	0.25	7	8	10
c1	0.18	0.203	0.23	7	8	9
D	8.56	8.66	8.74	337	341	344
E	5.80	6.00	6.20	228	236	244
E1	3.80	3.90	4.00	150	154	157
e	0.635 BSC			25 BSC		
h	0.25	0.42	0.50	10	17	20
L	0.40	0.635	1.27	16	25	50
L1	1.00	1.05	1.10	39	41	43
ZD	1.50 REF			58 REF		
Y			0.10			4
θ	0°		8°	0°		8°

NOTE:
1. REFER TO JEDEC STD MO-137 AD
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm (6 MIL) PER SIDE. PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm (6 MIL) PER SIDE.
3. DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE.
4. CONTROLLING DIMENSION: MILLIMENTER