AMC1100 Fully-Differential Isolation Amplifier

1 Features

- ±250-mV Input Voltage Range Optimized for Shunt Resistors
- Very Low Nonlinearity: 0.075% max at 5 V
- Low Offset Error: 1.5 mV max
- Low Noise: 3.1 mV_{RMS} typ
- Low High-Side Supply Current: 8 mA max at 5 V
- Input Bandwidth: 60 kHz min
- Fixed Gain: 8 (0.5% Accuracy)
- High Common-Mode Rejection Ratio: 108 dB
- Low-Side Operation: 3.3 V
- Certified Galvanic Isolation:
  - UL1577 and IEC60747-5-2 Approved
  - Isolation Voltage: 4250 V_{PEAK}
  - Working Voltage: 1200 V_{PEAK}
  - Transient Immunity: 2.5 kV/µs min
- Typical 10-Year Life Span at Rated Working Voltage (see Application Report SLLA197)
- Fully Specified Over the Extended Industrial Temperature Range

2 Applications

- Shunt Resistor Based Current Sensing in:
  - Energy Meters
  - Green Energy
  - Power Measurement Applications

3 Description

The AMC1100 is a precision isolation amplifier with an output separated from the input circuitry by a silicon dioxide (SiO_2) barrier that is highly resistant to magnetic interference. This barrier is certified to provide galvanic isolation of up to 4250 V_{PEAK}, according to UL1577 and IEC60747-5-2. Used in conjunction with isolated power supplies, this device prevents noise currents on a high common-mode voltage line from entering the local ground and interfering with or damaging sensitive circuitry.

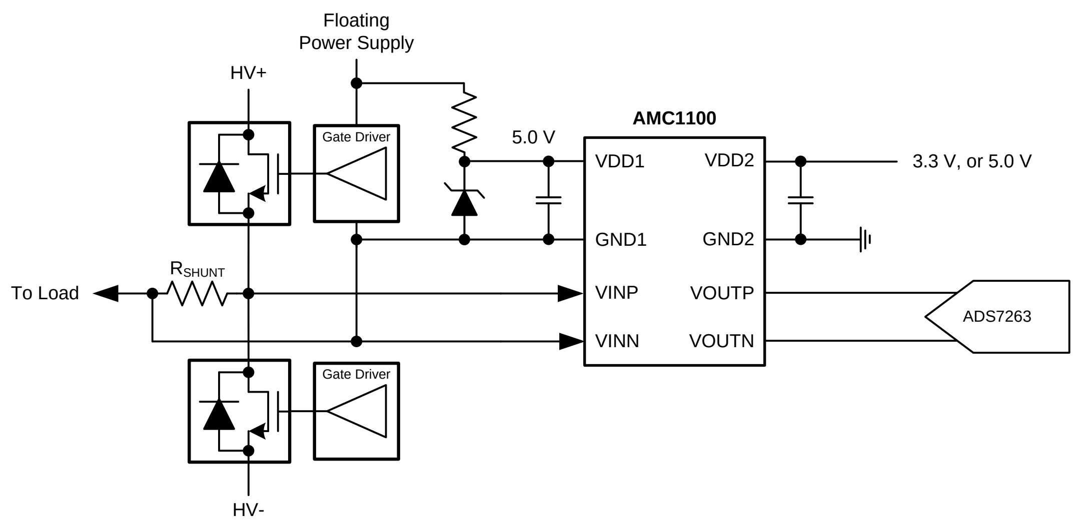
The AMC1100 input is optimized for direct connection to shunt resistors or other low voltage level signal sources. The excellent performance of the device enables accurate current and voltage measurement in energy-metering applications. The output signal common-mode voltage is automatically adjusted to either the 3-V or 5-V low-side supply.

The AMC1100 is fully specified over the extended industrial temperature range of –40°C to +105°C and is available in the SMD-type, wide-body SOIC-8 (DWV) and gullwing-8 (DUB) packages.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AMC1100	SOP (8)	9.50 mm × 6.57 mm
	SOIC (8)	5.85 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



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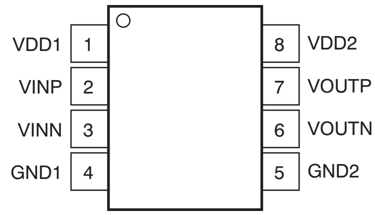
4 Revision History

Changes from Original (April 2012) to Revision A **Page**

- Changed format to meet latest data sheet standards 1
- Added *ESD Rating* table and *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections 1
- Added DWV package to document 1
- Deleted *Package and Ordering Information* section 3

5 Pin Configuration and Functions

DUB and DWV Packages
SOP-8 and SOIC-8
(Top View)



Pin Descriptions

PIN		FUNCTION	DESCRIPTION
NAME	NO.		
GND1	4	Power	High-side analog ground
GND2	5	Power	Low-side analog ground
VDD1	1	Power	High-side power supply
VDD2	8	Power	Low-side power supply
VINN	3	Analog input	Inverting analog input
VINP	2	Analog input	Noninverting analog input
VOUTN	6	Analog output	Inverting analog output
VOUTP	7	Analog output	Noninverting analog output

6 Specifications

6.1 Absolute Maximum Ratings

over the operating ambient temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage, VDD1 to GND1 or VDD2 to GND2	–0.5	6	V
Analog input voltage at VINP, VINN	GND1 – 0.5	VDD1 + 0.5	V
Input current to any pin except supply pins		±10	mA
Maximum junction temperature, T_J Max		150	°C
Storage temperature range, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_A	Operating ambient temperature range	–40		105	°C
VDD1	High-side power supply	4.5	5.0	5.5	V
VDD2	Low-side power supply	2.7	5.0	5.5	V

6.4 Thermal Information

THERMAL METRIC(1)		AMC1100		UNIT
		DUB (SOP)	DWV (SOIC)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	75.1	102.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.6	49.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	39.8	56.6	
ψ_{JT}	Junction-to-top characterization parameter	27.2	16.0	
ψ_{JB}	Junction-to-board characterization parameter	39.4	55.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Regulatory Information

VDE AND IEC	UL	CSA
Certified according to IEC 60747-5-2	Recognized under 1577 component recognition program	Recognized under CSA component acceptance NO 5 program
File number: 40016131	File number: E181974	File number: pending

6.6 IEC 60747-5-2 Insulation Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
V_{IORM}	Maximum working insulation voltage		1200	V_{PEAK}
V_{PR}	Input-to-output test voltage	Qualification test: after input/output safety test subgroup 2/3 $V_{PR} = V_{IORM} \times 1.2$, t = 10 s, partial discharge < 5 pC	1140	V_{PEAK}
		Qualification test: method A, after environmental tests subgroup 1, $V_{PR} = V_{IORM} \times 1.6$, t = 10 s, partial discharge < 5 pC	1920	V_{PEAK}
		100% production test: method B1, $V_{PR} = V_{IORM} \times 1.875$, t = 1 s, partial discharge < 5 pC	2250	V_{PEAK}
V_{IOTM}	Transient overvoltage	Qualification test: t = 60 s	4250	V_{PEAK}
V_{ISO}	Insulation voltage per UL	Qualification test: $V_{TEST} = V_{ISO}$, t = 60 s	4250	V_{PEAK}
		100% production test: $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s	5100	V_{PEAK}
R_S	Insulation resistance	V_{IO} = 500 V	$> 10^9$	Ω
PD	Pollution degree		2	°

6.7 IEC Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output (I/O) circuitry. I/O circuitry failure can allow low resistance to either ground or supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, thus potentially leading to secondary system failures.

The safety-limiting constraint is the operating virtual junction temperature range specified in the *Absolute Maximum Ratings* table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determine the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed in the JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface-Mount Packages* and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	θ_{JA} = 246°C/W, V_{IN} = 5.5 V, T_J = +150°C, T_A = +25°C			10	mA
T_C	Maximum-case temperature				+150	°C

6.8 IEC 61000-4-5 Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
V_{IOSM}	Surge immunity	1.2-µs or 50-µs voltage surge and 8-µs or 20-µs current surge	±6000	V

6.9 IEC 60664-1 Ratings

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	II
Installation classification	Rated mains voltage ≤ 150 V_{RMS}	I-IV
	Rated mains voltage ≤ 300 V_{RMS}	I-IV
	Rated mains voltage ≤ 400 V_{RMS}	I-III
	Rated mains voltage < 600 V_{RMS}	I-III

6.10 Package Characteristics(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (clearance)	Shortest terminal-to-terminal distance through air	7			mm
L(I02)	Minimum external tracking (creepage)	Shortest terminal-to-terminal distance across package surface	7			mm
CTI	Tracking resistance (comparative tracking index)	DIN IEC 60112 and VDE 0303 part 1	> 400			V
	Minimum internal gap (internal clearance)	Distance through insulation	0.014			mm
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500 V, all pins on each side of the barrier tied together to create a two-terminal device, T_A < +85°C		> 10^{12}		Ω
		Input to output, V_{IO} = 500 V, +85°C ≤ T_A < T_A max		> 10^{11}		Ω
C_{IO}	Barrier capacitance input to output	V_I = 0.5 V_{PP} at 1 MHz		1.2		pF
C_I	Input capacitance to ground	V_I = 0.5 V_{PP} at 1 MHz		3		pF

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of a specific application. Care should be taken to maintain the creepage and clearance distance of the board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal according to the measurement techniques shown in the *Isolation Glossary* section. Techniques such as inserting grooves or ribs on the PCB are used to help increase these specifications.

6.11 Electrical Characteristics

All minimum and maximum specifications are at T_A = –40°C to +105°C and are within the specified voltage range, unless otherwise noted. Typical values are at T_A = +25°C, VDD1 = 5 V, and VDD2 = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
	Maximum input voltage before clipping	VINP – VINN		±320		mV
	Differential input voltage	VINP – VINN	–250		250	mV
V_{CM}	Common-mode operating range		–0.16		VDD1	V
V_{OS}	Input offset voltage		–1.5	±0.2	1.5	mV
TCV_{OS}	Input offset thermal drift		–10	±1.5	10	µV/K
CMRR	Common-mode rejection ratio	V_{IN} from 0 V to 5 V at 0 Hz		108		dB
		V_{IN} from 0 V to 5 V at 50 kHz		95		dB
C_{IN}	Input capacitance to GND1	VINP or VINN		3		pF
C_{IND}	Differential input capacitance			3.6		pF
R_{IN}	Differential input resistance			28		kΩ
	Small-signal bandwidth		60	100		kHz
OUTPUT						
	Nominal gain			8		
G_{ERR}	Gain error	Initial, at T_A = +25°C	–0.5%	±0.05%	0.5%	
			–1%	±0.05%	1%	
TCG_{ERR}	Gain error thermal drift			±56		ppm/K
	Nonlinearity	4.5 V ≤ VDD2 ≤ 5.5 V	–0.075%	±0.015%	0.075%	
		2.7 V ≤ VDD2 ≤ 3.6 V	–0.1%	±0.023%	0.1%	
	Nonlinearity thermal drift			2.4		ppm/K
	Output noise	VINP = VINN = 0 V		3.1		mV_{RMS}
PSRR	Power-supply rejection ratio	vs VDD1, 10-kHz ripple		80		dB
		vs VDD2, 10-kHz ripple		61		dB
	Rise-and-fall time	0.5-V step, 10% to 90%		3.66	6.6	µs
	V_{IN} to V_{OUT} signal delay	0.5-V step, 50% to 10%, unfiltered output		1.6	3.3	µs
		0.5-V step, 50% to 50%, unfiltered output		3.15	5.6	µs
		0.5-V step, 50% to 90%, unfiltered output		5.26	9.9	µs
CMTI	Common-mode transient immunity	V_{CM} = 1 kV	2.5	3.75		kV/µs
	Output common-mode voltage	2.7 V ≤ VDD2 ≤ 3.6 V	1.15	1.29	1.45	V
		4.5 V ≤ VDD2 ≤ 5.5 V	2.4	2.55	2.7	V
	Short-circuit current			20		mA
R_{OUT}	Output resistance			2.5		Ω
POWER SUPPLY						
VDD1	High-side supply voltage		4.5	5.0	5.5	V
VDD2	Low-side supply voltage		2.7	5.0	5.5	V
I_{DD1}	High-side supply current			5.4	8	mA
I_{DD2}	Low-side supply current	2.7 V < VDD2 < 3.6 V		3.8	6	mA
		4.5 V < VDD2 < 5.5 V		4.4	7	mA
P_{DD1}	High-side power dissipation			27.0	44.0	mW
P_{DD2}	Low-side power dissipation	2.7 V < VDD2 < 3.6 V		11.4	21.6	mW
		4.5 V < VDD2 < 5.5 V		22.0	38.5	mW

6.12 Typical Characteristics

At VDD1 = VDD2 = 5 V, VINP = –250 mV to +250 mV, and VINN = 0 V, unless otherwise noted.

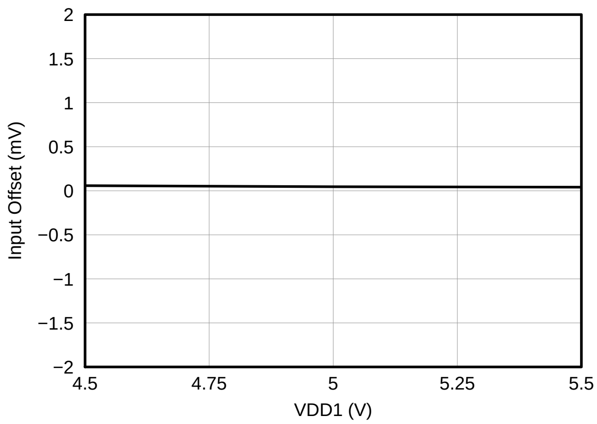


Figure 1. Input Offset vs High-Side Supply Voltage

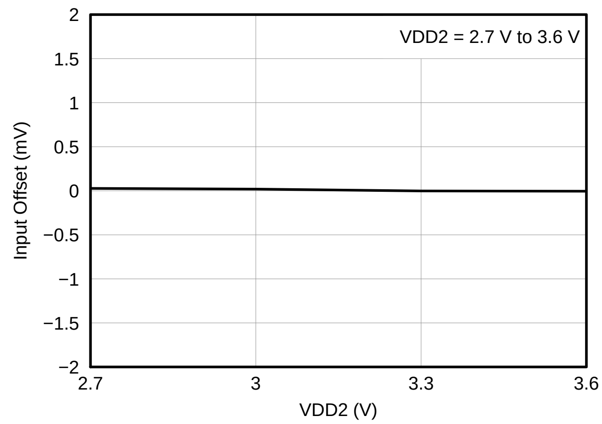


Figure 2. Input Offset vs Low-Side Supply Voltage

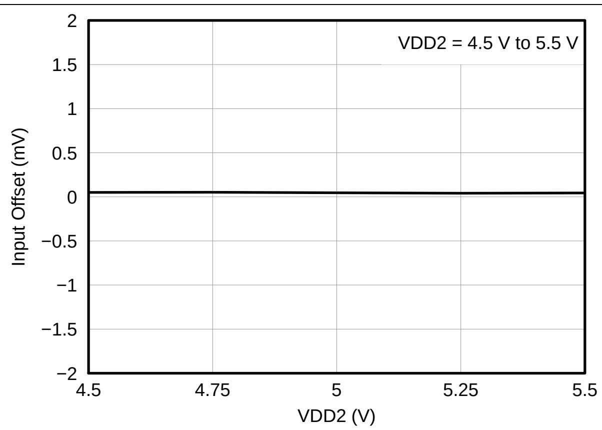


Figure 3. Input Offset vs Low-Side Supply Voltage

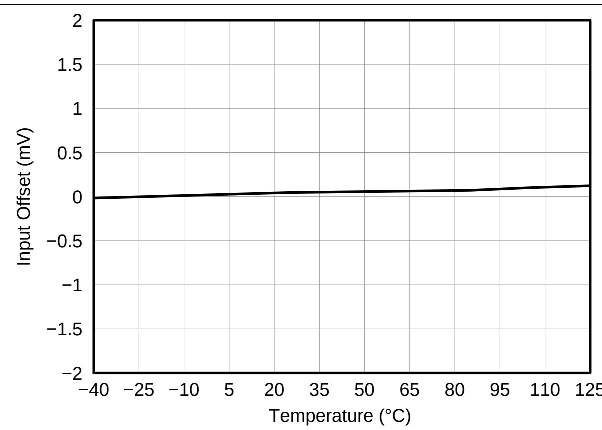


Figure 4. Input Offset vs Temperature

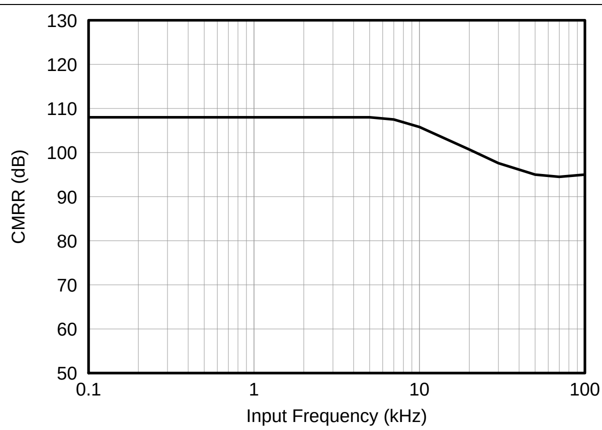


Figure 5. Common-Mode Rejection Ratio vs Input Frequency

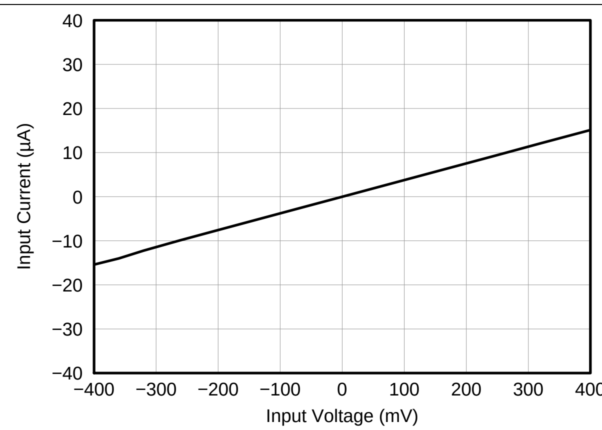


Figure 6. Input Current vs Input Voltage

Typical Characteristics (continued)

At VDD1 = VDD2 = 5 V, VINP = –250 mV to +250 mV, and VINN = 0 V, unless otherwise noted.

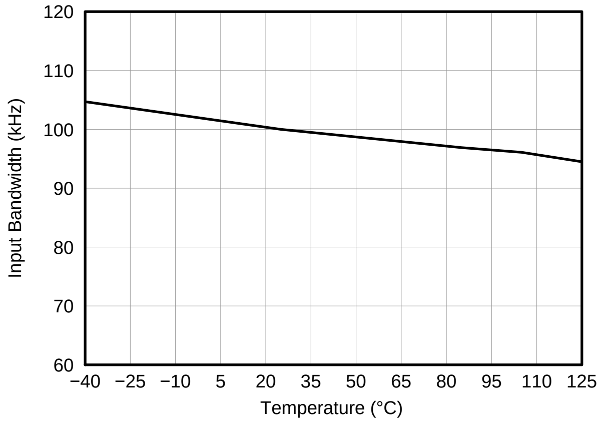


Figure 7. Input Bandwidth vs Temperature

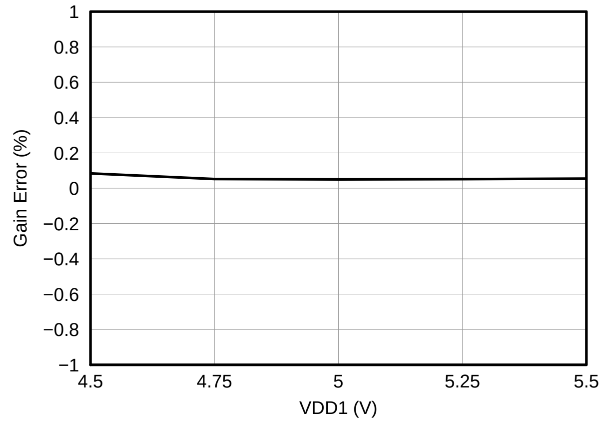


Figure 8. Gain Error vs High-Side Supply Voltage

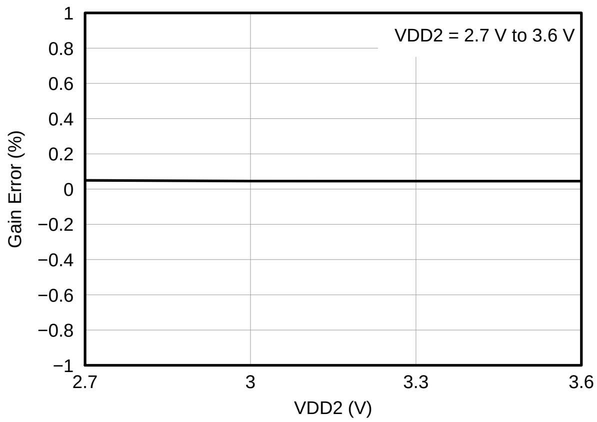


Figure 9. Gain Error vs Low-Side Supply Voltage

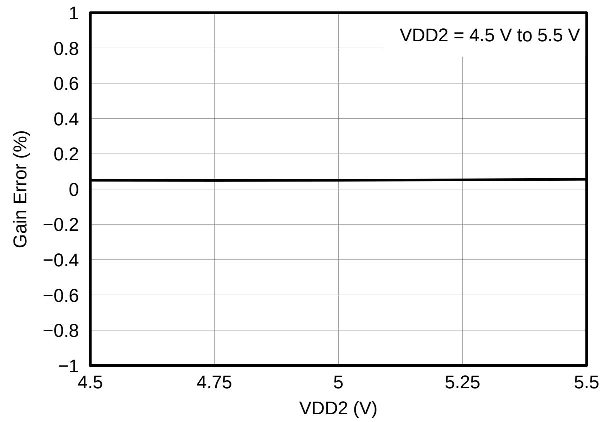


Figure 10. Gain Error vs Low-Side Supply Voltage

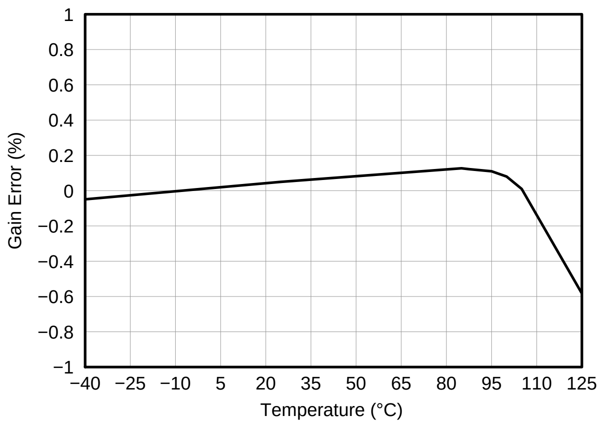


Figure 11. Gain Error vs Temperature

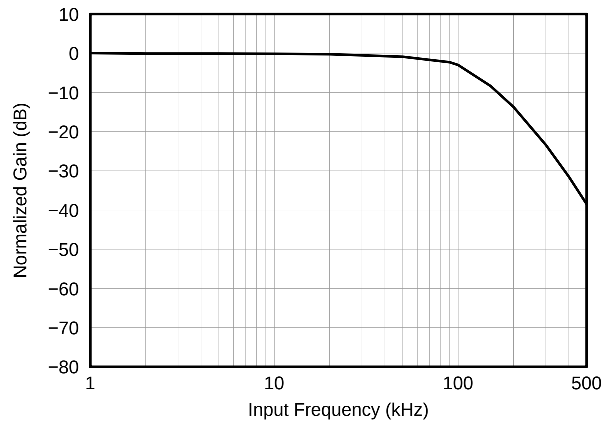


Figure 12. Normalized Gain vs Input Frequency

Typical Characteristics (continued)

At VDD1 = VDD2 = 5 V, VINP = –250 mV to +250 mV, and VINN = 0 V, unless otherwise noted.

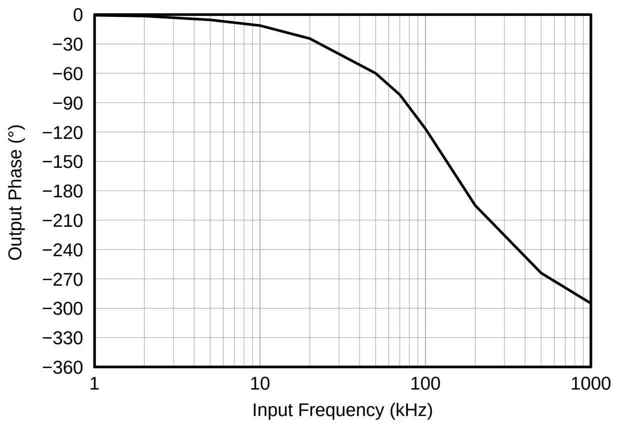


Figure 13. Output Phase vs Input Frequency

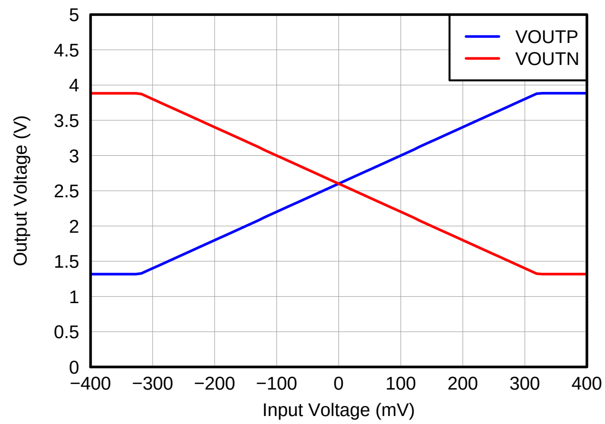


Figure 14. Output Voltage vs Input Voltage

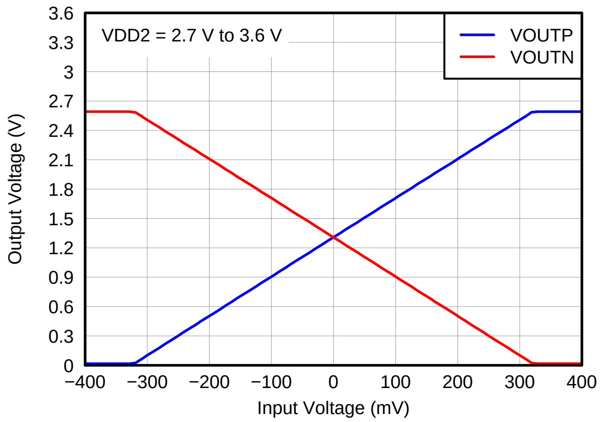


Figure 15. Output Voltage vs Input Voltage

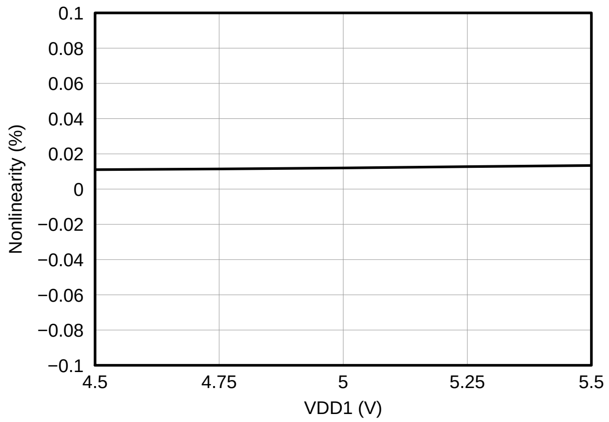


Figure 16. Nonlinearity vs High-Side Supply Voltage

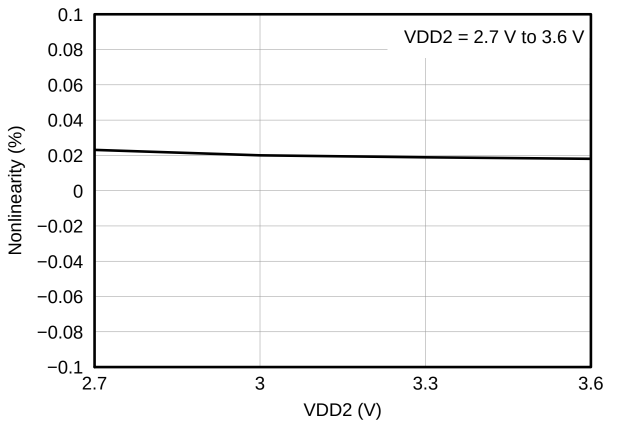


Figure 17. Nonlinearity vs Low-Side Supply Voltage

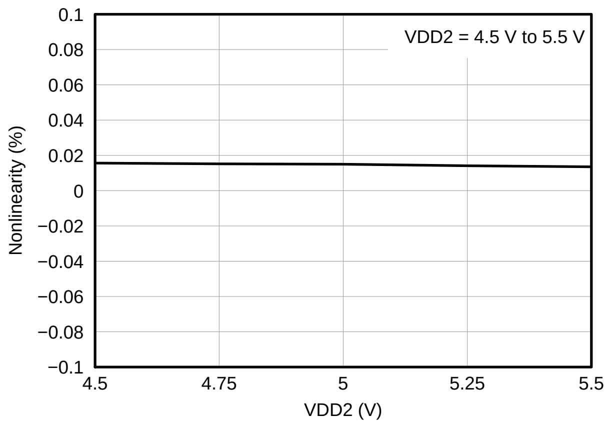


Figure 18. Nonlinearity vs Low-Side Supply Voltage

Typical Characteristics (continued)

At VDD1 = VDD2 = 5 V, VINP = –250 mV to +250 mV, and VINN = 0 V, unless otherwise noted.

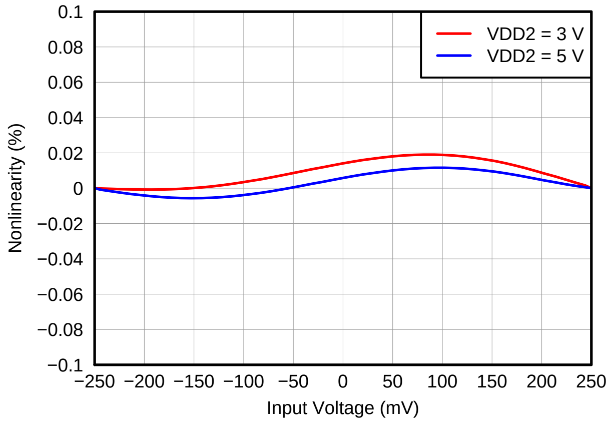


Figure 19. Nonlinearity vs Input Voltage

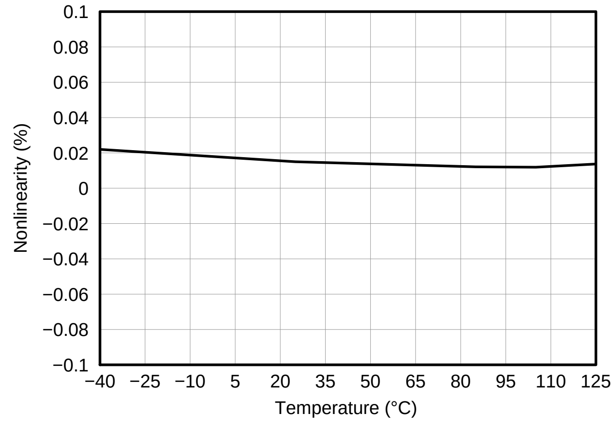


Figure 20. Nonlinearity vs Temperature

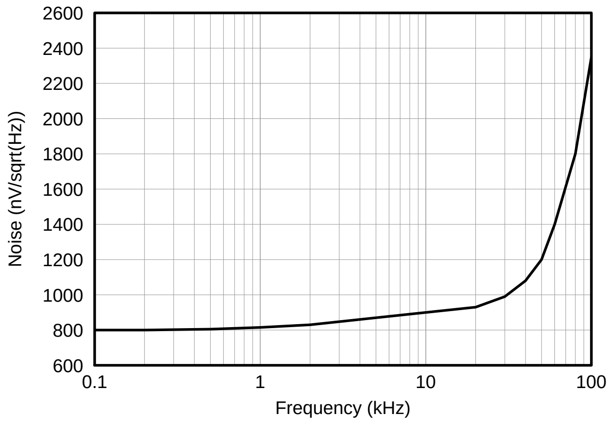


Figure 21. Output Noise Density vs Frequency

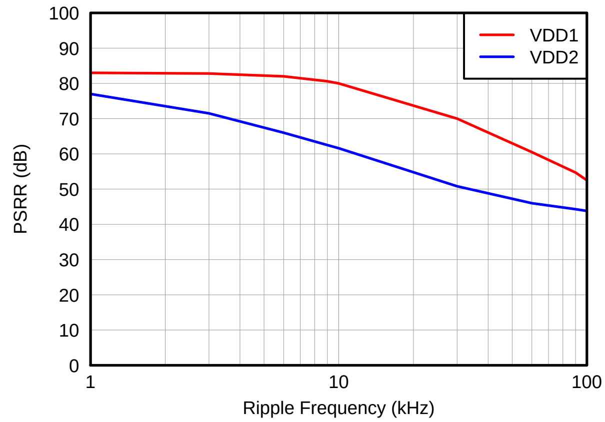


Figure 22. Power-Supply Rejection Ratio vs Ripple Frequency

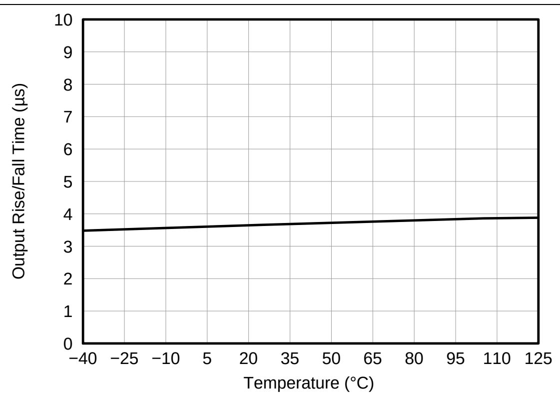


Figure 23. Output Rise and Fall Time vs Temperature

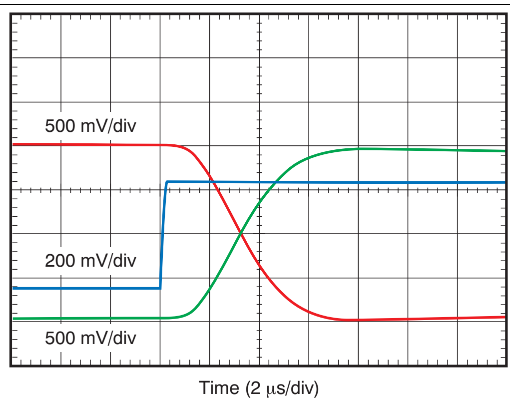


Figure 24. Full-Scale Step Response

Typical Characteristics (continued)

At VDD1 = VDD2 = 5 V, VINP = –250 mV to +250 mV, and VINN = 0 V, unless otherwise noted.

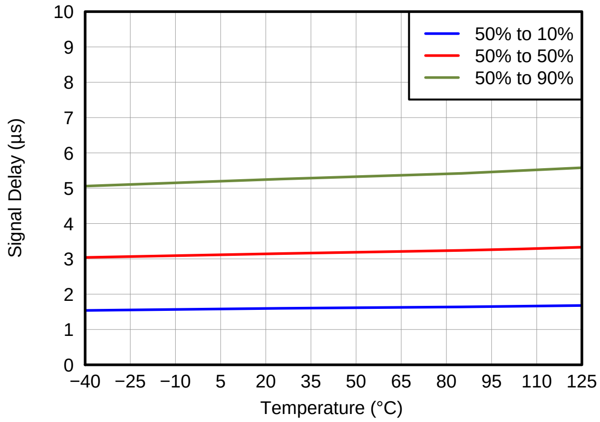


Figure 25. Output Signal Delay Time vs Temperature

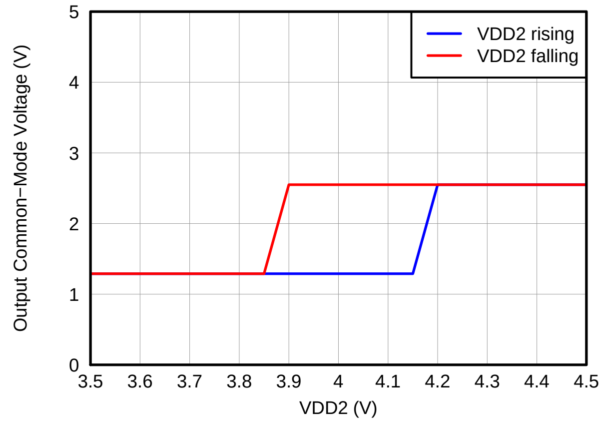


Figure 26. Output Common-Mode Voltage vs Low-Side Supply Voltage

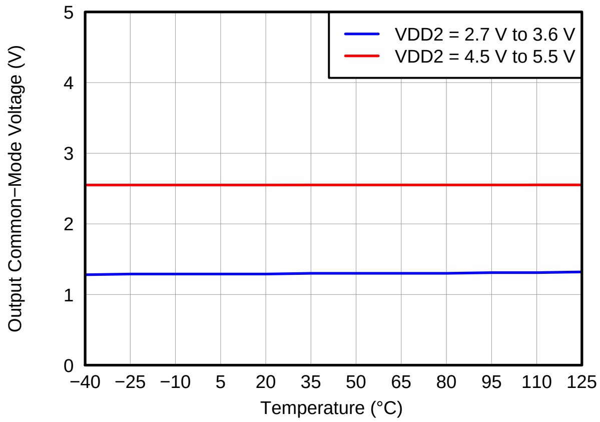


Figure 27. Output Common-Mode Voltage vs Temperature

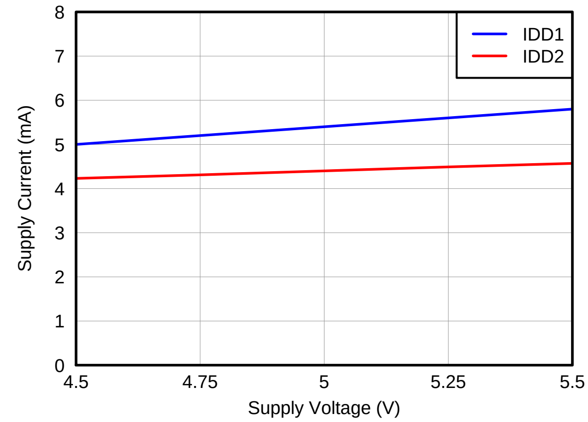


Figure 28. Supply Current vs Supply Voltage

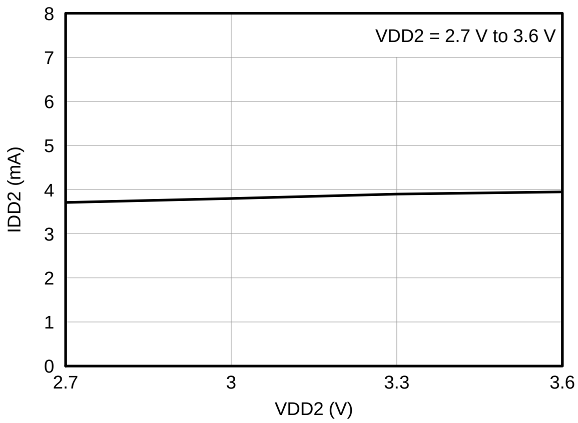


Figure 29. Low-Side Supply Current vs Low-Side Supply Voltage

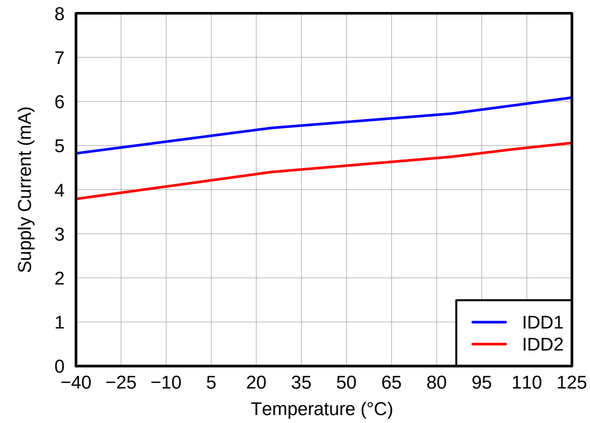


Figure 30. Supply Current vs Temperature

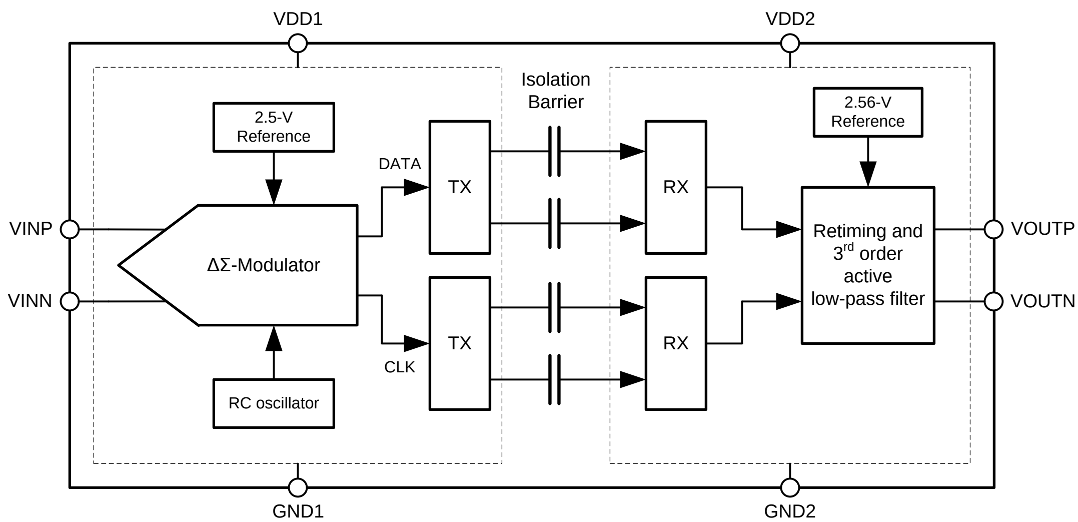
7 Detailed Description

7.1 Overview

The AMC1100 consists of a delta-sigma modulator input stage including an internal reference and clock generator. The output of the modulator and clock signal are differentially transmitted over the integrated capacitive isolation barrier that separates the high- and low-voltage domains. The received bitstream and clock signals are synchronized and processed by a third-order analog filter with a nominal gain of 8 on the low-side and presented as a differential output of the device, as shown in the *Functional Block Diagram* section.

The SiO_2-based capacitive isolation barrier supports a high level of magnetic field immunity, as described in application report SLLA181, *ISO72x Digital Isolator Magnetic-Field Immunity* (available for download at www.ti.com).

7.2 Functional Block Diagram



7.3 Feature Description

The differential analog input of the AMC1100 is a switched-capacitor circuit based on a second-order modulator stage that digitizes the input signal into a 1-bit output stream. The device compares the differential input signal (V_{IN} = VINP – VINN) against the internal reference of 2.5 V using internal capacitors that are continuously charged and discharged with a typical frequency of 10 MHz. With the S1 switches closed, C_{IND} charges to the voltage difference across VINP and VINN. For the discharge phase, both S1 switches open first and then both S2 switches close. C_{IND} discharges to approximately GND1 + 0.8 V during this phase. Figure 31 shows the simplified equivalent input circuitry.

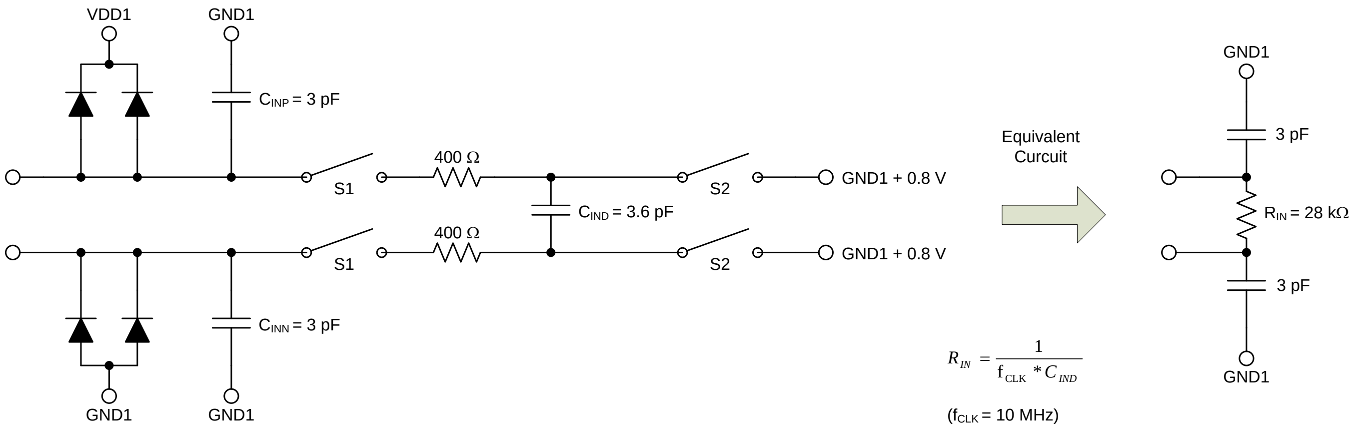


Figure 31. Equivalent Input Circuit

The analog input range is tailored to directly accommodate a voltage drop across a shunt resistor used for current sensing. However, there are two restrictions on the analog input signals, VINP and VINN. If the input voltage exceeds the range GND1 – 0.5 V to VDD1 + 0.5 V, the input current must be limited to 10 mA to protect the implemented input protection diodes from damage. In addition, the device linearity and noise performance are ensured only when the differential analog input voltage remains within ±250 mV.

7.4 Device Functional Modes

The AMC1100 is powered on when the supplies are connected. The device is operated off a 5-V nominal supply on the high-side. The potential of the ground reference GND1 can be floating, which is usually the case in shunt-based current-measurement applications. TI recommends tying one side of the shunt to the GND1 pin of the AMC1100 to maintain the operating common-mode range requirements of the device.

The low-side of the AMC1100 can be powered from a supply source with a nominal voltage of 3.0 V, 3.3 V, or 5.0 V. When operated at 5 V, the common-mode voltage of the output stage is set to 2.55 V nominal; in both other cases, the common-mode voltage is automatically set to 1.29 V.

Although usually applied in shunt-based current-sensing circuits, the AMC1100 can also be used for isolated voltage measurement applications, as shown in a simplified way in Figure 32. In such applications, usually a resistor divider (R_1 and R_2 in Figure 32) is used to match the relatively small input voltage range of the AMC1100. R_2 and the AMC1100 input resistance (R_{IN}) also create a resistance divider that results in additional gain error. With the assumption that R_1 and R_{IN} have a considerably higher value than R_2, the resulting total gain error can be estimated using Equation 1:

$$G_{ERRTOT} = G_{ERR} + \frac{R_2}{R_{IN}} \quad (1)$$

where:

- G_{ERR} = device gain error.

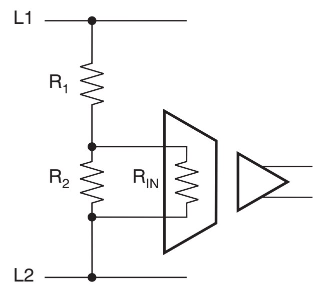


Figure 32. Voltage Measurement Application

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The AMC1100 offers unique linearity, high input common-mode rejection, and low dc errors and drift. These features make the AMC1100 a robust, high-performance isolation amplifier for industrial applications where users and subsystems must be protected from high voltage potentials.

8.2 Typical Applications

8.2.1 The AMC1100 in Frequency Inverters

A typical operation for the AMC1100 is isolated current and voltage measurement in frequency inverter applications (such as industrial motor drives, photovoltaic inverters, or uninterruptible power supplies), as conceptually shown in Figure 33. Depending on the end application, only two or three phase currents are being sensed.

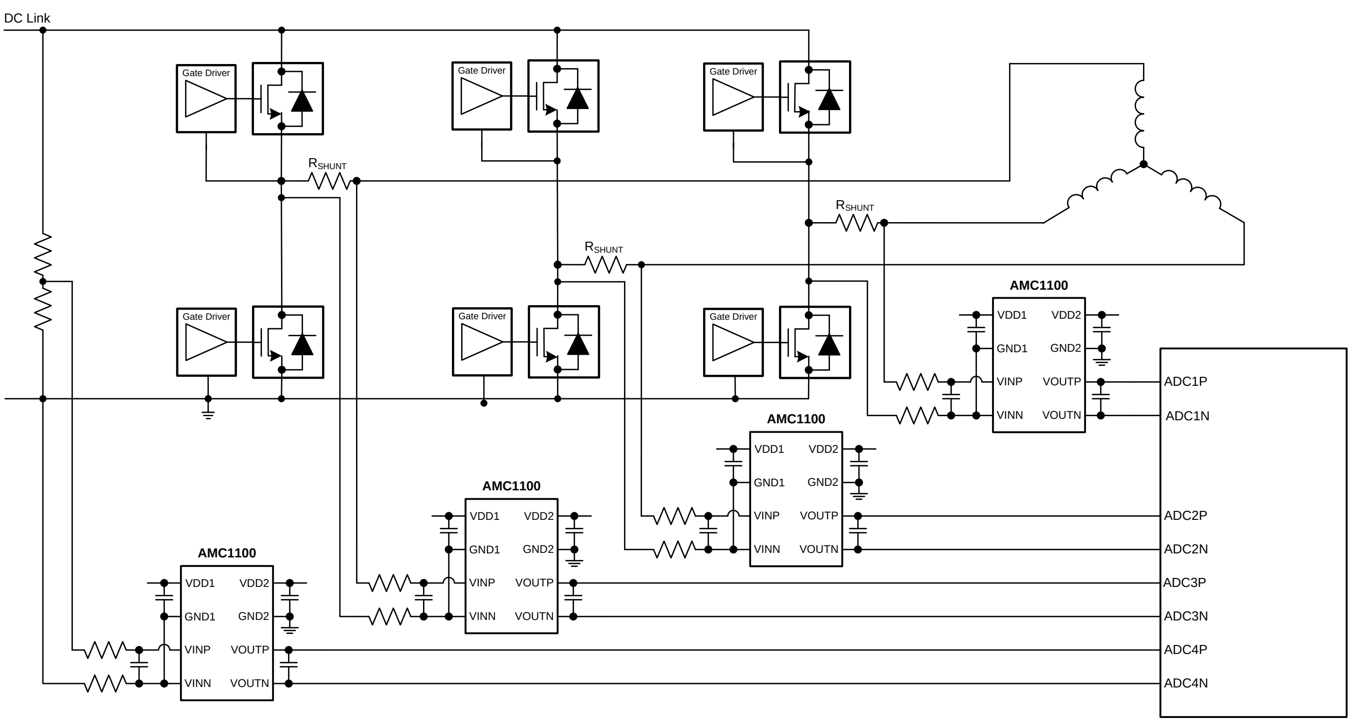


Figure 33. Isolated Current and Voltage Sensing in Frequency Inverters

8.2.1.1 Design Requirements

Current measurement through the phase of a motor power line is done via the shunt resistor R_{SHUNT} (in a two-terminal shunt); see Figure 34. For better performance, the differential signal is filtered using RC filters (components R_2, R_3, and C_2). Optionally, C_3 and C_4 can be used to reduce charge dumping from the inputs. In this case, care must be taken when choosing the quality of these capacitors; mismatch in values of these capacitors leads to a common-mode error at the modulator input. Using NP0 capacitors is recommended, if necessary.

Typical Applications (continued)

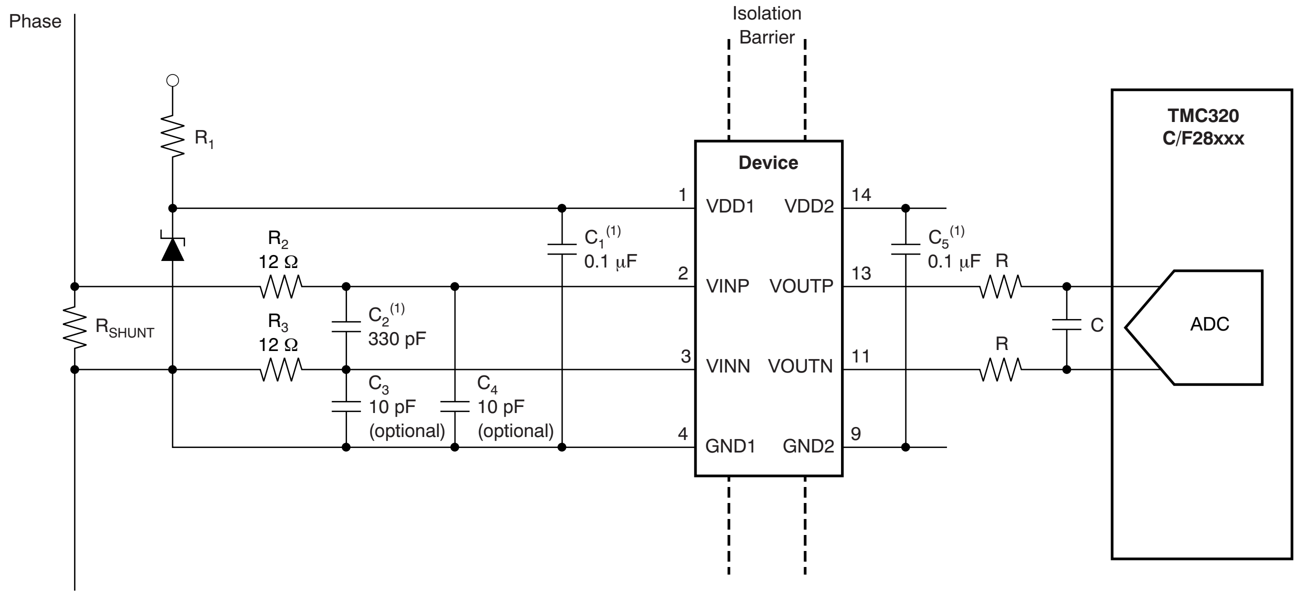


Figure 34. Shunt-Based Current Sensing with the AMC1100

The isolated voltage measurement can be performed as described in the *Device Functional Modes* section.

8.2.1.2 Detailed Design Procedure

The floating ground reference (GND1) is derived from the end of the shunt resistor, which is connected to the negative input of the AMC1100 (VINN). If a four-terminal shunt is used, the inputs of the AMC1100 are connected to the inner leads and GND1 is connected to one of the outer shunt leads. The differential input of the AMC1100 ensures accurate operation even in noisy environments.

The differential output of the AMC1100 can either directly drive an analog-to-digital converter (ADC) input or can be further filtered before being processed by the ADC.

8.2.1.3 Application Curve

In frequency inverter applications the power switches must be protected in case of an overcurrent condition. To allow fast powering off of the system, low delay caused by the isolation amplifier is required. Figure 35 shows the typical full-scale step response of the AMC1100.

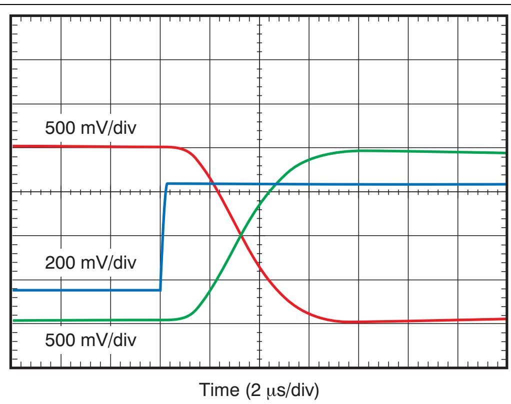


Figure 35. Typical Step Response of the AMC1100

Typical Applications (continued)

8.2.2 The AMC1100 in Energy Metering

Resulting from its immunity to magnetic fields, the AMC1100 can be used for shunt-based current sensing in smart electricity meter (e-meter) designs, as shown in Figure 36. Three AMC1100 devices are used for isolated current sensing. For voltage sensing, resistive dividers are usually used to reduce the common-mode voltage to levels that allow non-isolated measurement.

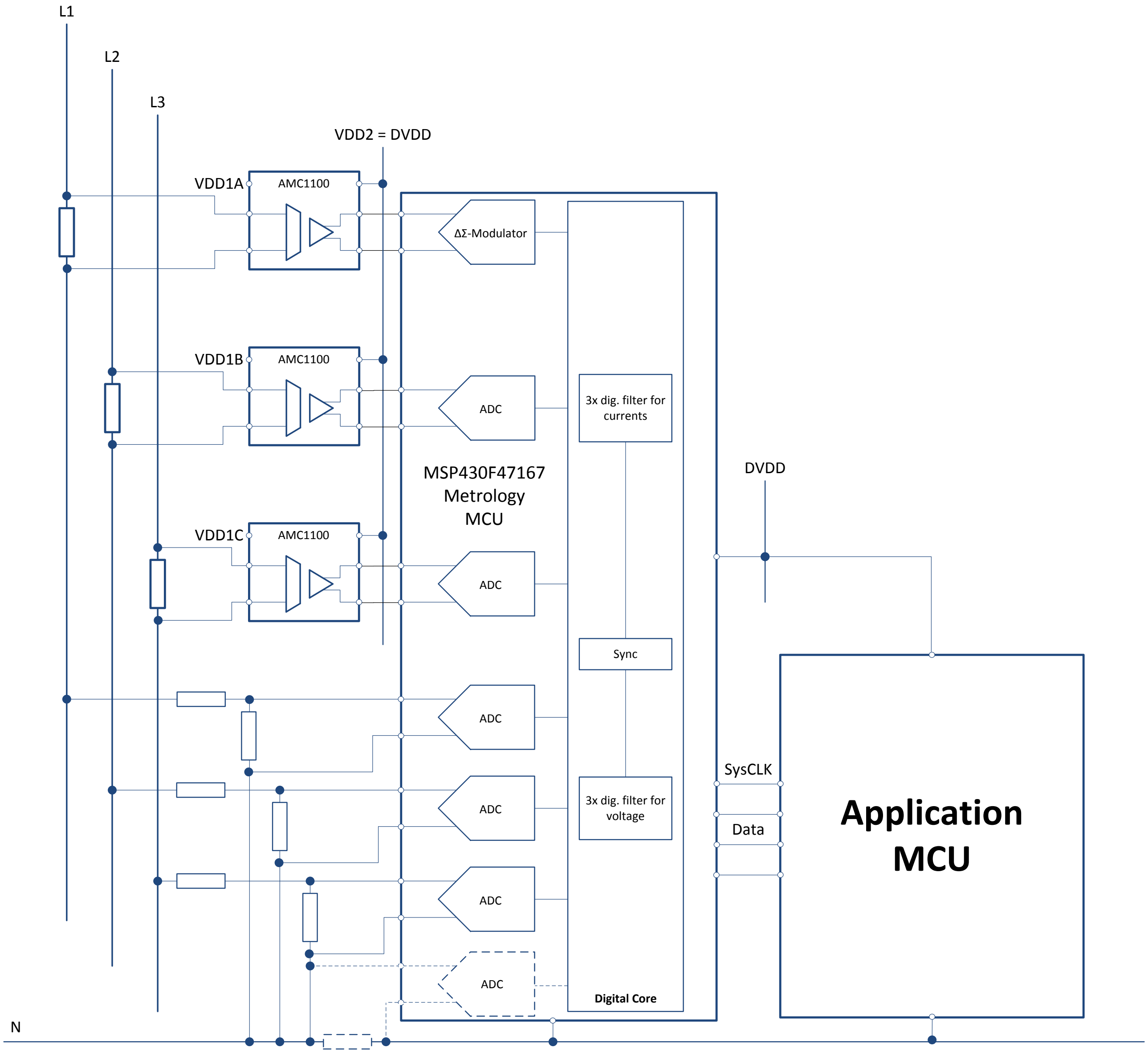


Figure 36. The AMC1100 in an E-Meter Application

8.2.2.1 Design Requirements

For best performance, an RC low-pass filter can be used in front of the AMC1100. Further improvement can be achieved by filtering the output signal of the device. In both cases, the values of the resistors and the capacitors must be tailored to the bandwidth requirements of the system.

Typical Applications (continued)

The analog output of the device is converted to the digital domain using the on-chip analog-to-digital converters (ADCs) of a suitable metrology microcontroller. The architecture of the MSP430F471x7 family of ultra-low power microcontrollers is tailored for this kind of applications. The MSP430F471x7 offers up to seven ADCs for simultaneous sampling: six of which are used for the three phase currents and voltages whereas the seventh channel can be used for additional voltage sensing of the neutral line for applications that require anti-tampering measures.

8.2.2.2 Detailed Design Procedure

The high-side supply for the AMC1100 can be derived from the phase voltage using a capacitive-drop power supply (cap-drop), as shown in Figure 37 and described in the application report SLAA552, *AMC1100: Replacement of Input Main Sensing Transformer in Inverters with Isolate Amplifier*.

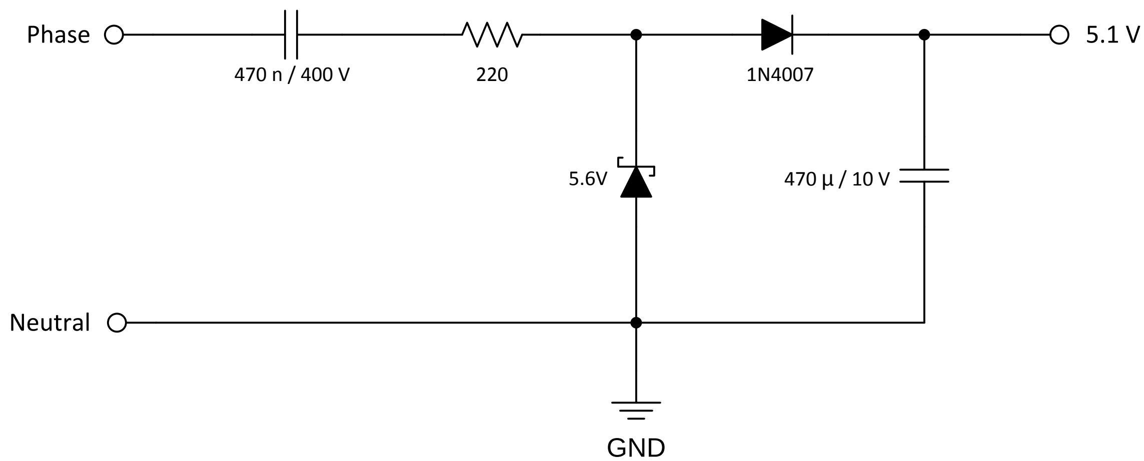


Figure 37. Cap-Drop High-Side Power Supply for the AMC1100

Alternatively, the high-side power supply for each AMC1100 can also be derived from the low-side supply using the SN6501 to drive a transformer, as proven by the TI reference design TIPD121, *Isolated Current Sensing Reference Design Solution, 5A, 2kV*.

8.2.2.3 Application Curve

One of the key parameters of an e-meter is its noise performance, which is mainly influenced by the performance of the ADC and the current sensor. When using a shunt-based approach, the sensor front-end consists of the actual shunt resistor and the isolated amplifier. Figure 38 shows the typical output noise density of the AMC1100 as a basis for overall performance estimations.

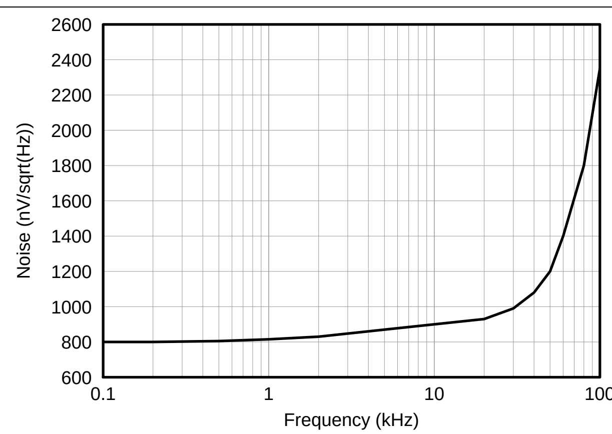


Figure 38. Output Noise Density of the AMC1100

9 Power Supply Recommendations

In a typical frequency inverter application, the high-side power supply for the AMC1100 (VDD1) is derived from the system supply, as shown in Figure 39. For lowest cost, a Zener diode can be used to limit the voltage to 5 V ± 10%. A 0.1-µF decoupling capacitor is recommended for filtering this power-supply path. Place this capacitor (C_1) as close as possible to the VDD1 pin for best performance. If better filtering is required, an additional 1-µF to 10-µF capacitor can be used.

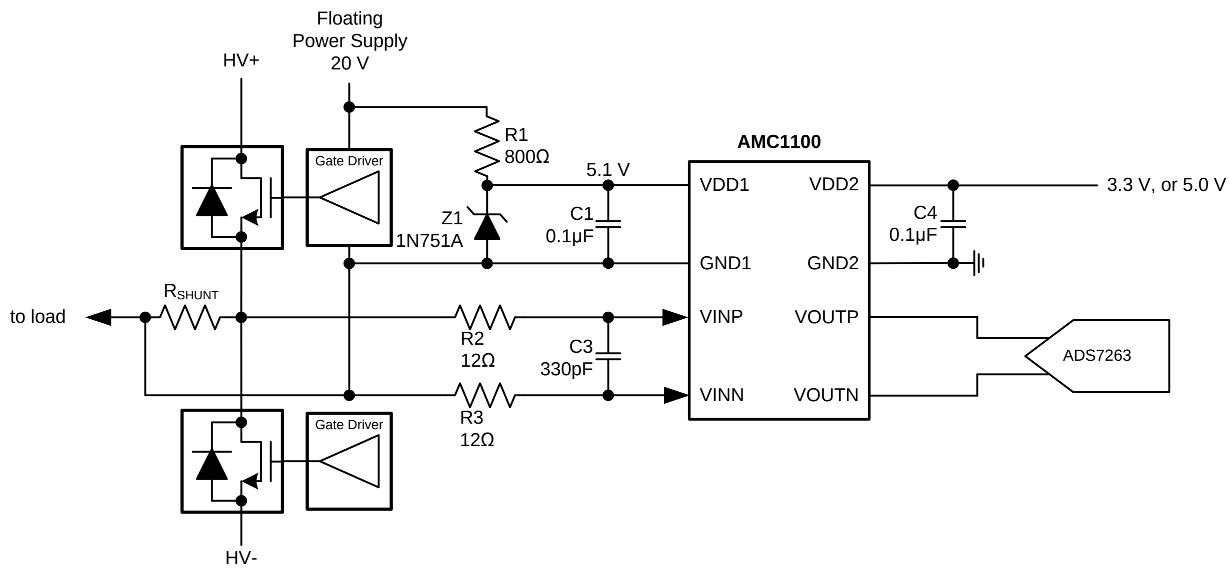


Figure 39. Zener Diode Based High-Side Supply

For higher power efficiency and better performance, a buck converter can be used; an example of such an approach is based on the LM5017. A reference design including performance test results and layout documentation can be downloaded at PMP9480, *Isolated Bias Supplies + Isolated Amplifier Combo for Line Voltage or Current Measurement*.

10 Layout

10.1 Layout Guidelines

A layout recommendation showing the critical placement of the decoupling capacitors that be placed as close as possible to the AMC1100 while maintaining a differential routing of the input signals is shown in Figure 40.

To maintain the isolation barrier and the common-mode transient immunity (CMTI) of the device, keep the distance between the high-side ground (GND1) and the low-side ground (GND2) at a maximum; that is, the entire area underneath the device must be kept free of any conducting materials.

10.2 Layout Example

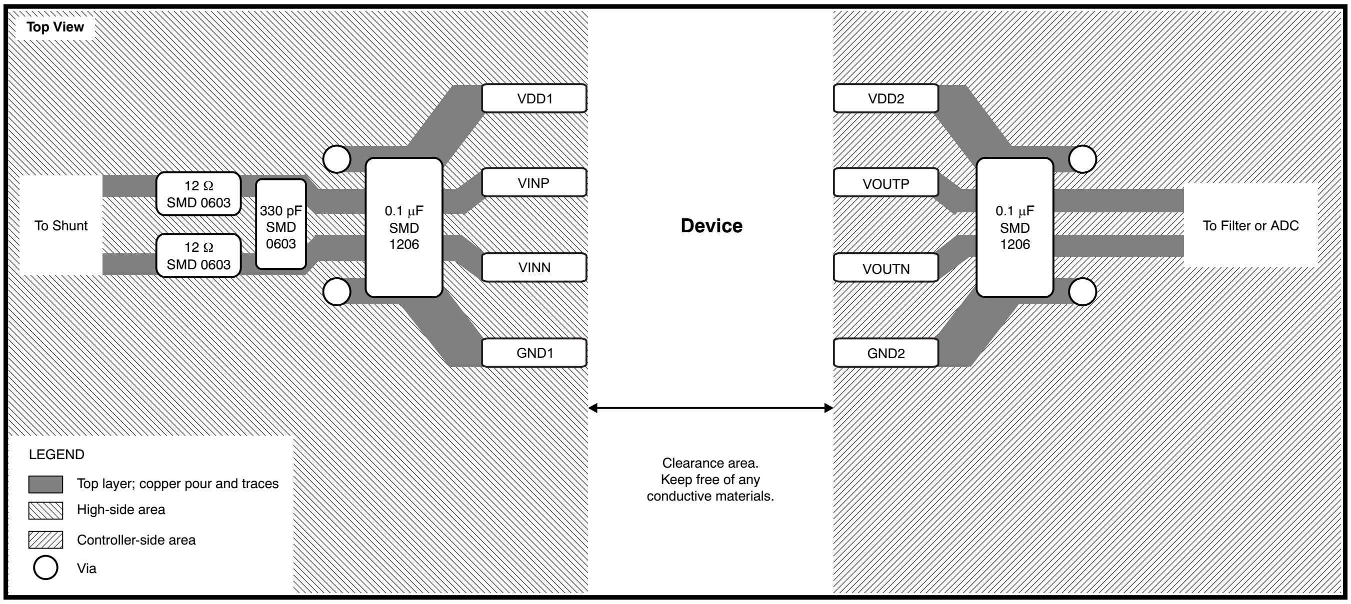


Figure 40. Example Layout

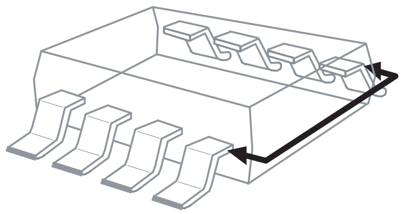
11 Device and Documentation Support

11.1 Device Support

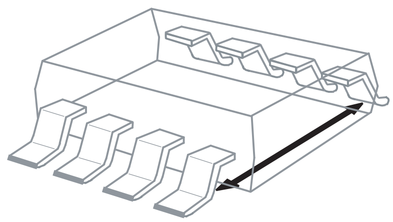
11.1.1 Device Nomenclature

11.1.1.1 Isolation Glossary

Creepage Distance: The shortest path between two conductive input-to-output leads measured along the surface of the insulation. The shortest distance path is found around the end of the package body.



Clearance: The shortest distance between two conductive input-to-output leads measured through air (line of sight).



Input-to-Output Barrier Capacitance: The total capacitance between all input terminals connected together, and all output terminals connected together.

Input-to-Output Barrier Resistance: The total resistance between all input terminals connected together, and all output terminals connected together.

Primary Circuit: An internal circuit directly connected to an external supply mains or other equivalent source that supplies the primary circuit electric power.

Secondary Circuit: A circuit with no direct connection to primary power that derives its power from a separate isolated source.

Comparative Tracking Index (CTI): CTI is an index used for electrical insulating materials. It is defined as the numerical value of the voltage that causes failure by tracking during standard testing. Tracking is the process that produces a partially conducting path of localized deterioration on or through the surface of an insulating material as a result of the action of electric discharges on or close to an insulation surface. The higher CTI value of the insulating material, the smaller the minimum creepage distance.

Generally, insulation breakdown occurs either through the material, over its surface, or both. Surface failure may arise from flashover or from the progressive insulation surface degradation by small localized sparks. Such sparks result from a surface film of a conducting contaminant breaking on the insulation. The resulting break in the leakage current produces an overvoltage at the site of the discontinuity, and an electric spark is generated. These sparks often cause carbonization on insulation material and lead to a carbon track between points of different potential. This process is known as *tracking*.

11.1.1.1.1 Insulation:

Operational insulation—Insulation needed for correct equipment operation.

Basic insulation—Insulation to provide basic protection against electric shock.

Supplementary insulation—Independent insulation applied in addition to basic insulation in order to ensure protection against electric shock in the event of a failure of the basic insulation.

Device Support (continued)

Double insulation—Insulation comprising both basic and supplementary insulation.

Reinforced insulation—A single insulation system that provides a degree of protection against electric shock equivalent to double insulation.

11.1.1.1.2 Pollution Degree:

Pollution Degree 1—No pollution, or only dry, nonconductive pollution occurs. The pollution has no influence on device performance.

Pollution Degree 2—Normally, only nonconductive pollution occurs. However, a temporary conductivity caused by condensation is to be expected.

Pollution Degree 3—Conductive pollution, or dry nonconductive pollution that becomes conductive because of condensation, occurs. Condensation is to be expected.

Pollution Degree 4—Continuous conductivity occurs as a result of conductive dust, rain, or other wet conditions.

11.1.1.1.3 Installation Category:

Overvoltage Category—This section is directed at insulation coordination by identifying the transient overvoltages that may occur, and by assigning four different levels as indicated in IEC 60664.

1. Signal Level: Special equipment or parts of equipment.
2. Local Level: Portable equipment and so forth
3. Distribution Level: Fixed installation.
4. Primary Supply Level: Overhead lines, cable systems.

Each category should be subject to smaller transients than the previous category.

11.2 Documentation Support

11.2.1 Related Documentation

High-Voltage Lifetime of the ISO72x Family of Digital Isolators, SLLA197

ISO72x Digital Isolator Magnetic-Field Immunity, SLLA181

AMC1100: Replacement of Input Main Sensing Transformer in Inverters with Isolate Amplifier, SLAA552

Isolated Current Sensing Reference Design Solution, 5A, 2kV, TIPD121

Isolated Bias Supplies + Isolated Amplifier Combo for Line Voltage or Current Measurement, PMP9480

TPS62120 Data Sheet, SLVSAD5

MSP430F471xx Data Sheet, SLAS626

SN6501 Data Sheet, SLLSEA0

LM5017 Data Sheet, SNVS783

11.3 Trademarks

All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC1100DUB	ACTIVE	SOP	DUB	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	AMC1100	Samples
AMC1100DUBR	ACTIVE	SOP	DUB	8	350	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	AMC1100	Samples
AMC1100DWV	ACTIVE	SOIC	DWV	8	64	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-2-260C-1 YEAR	-40 to 105	AMC1100	Samples
AMC1100DWVR	ACTIVE	SOIC	DWV	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-2-260C-1 YEAR	-40 to 105	AMC1100	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

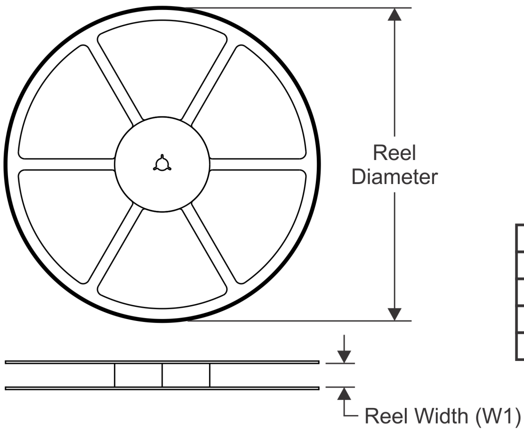
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

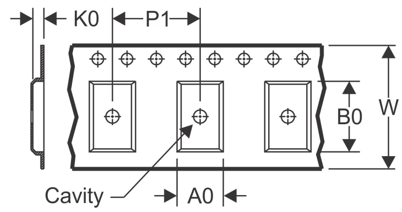
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

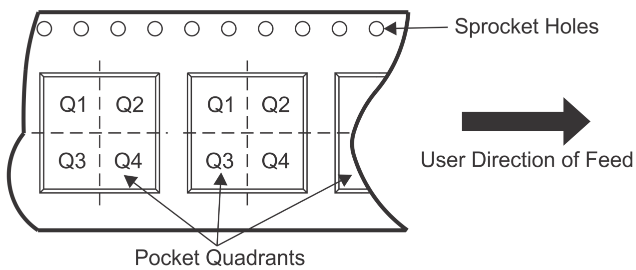


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

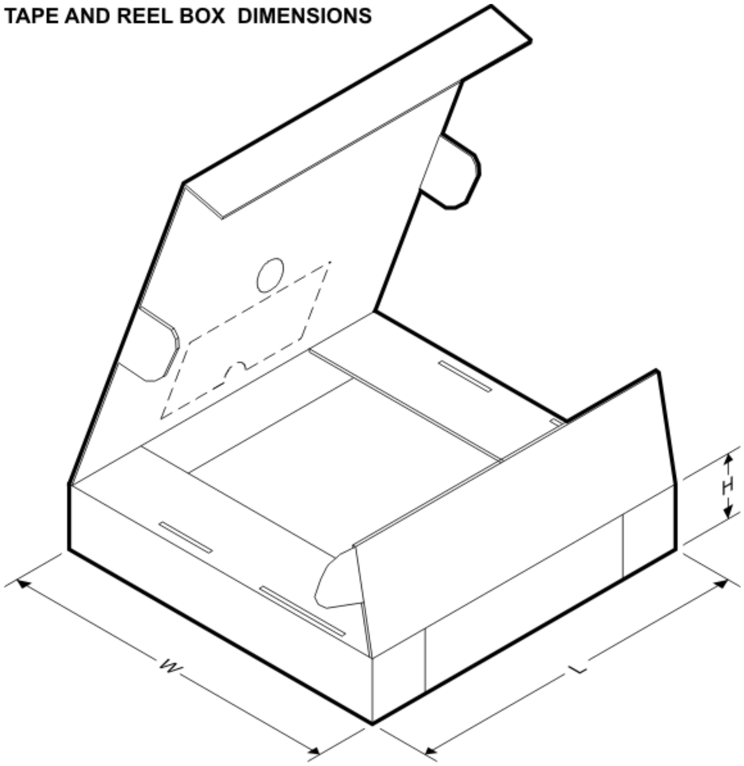
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

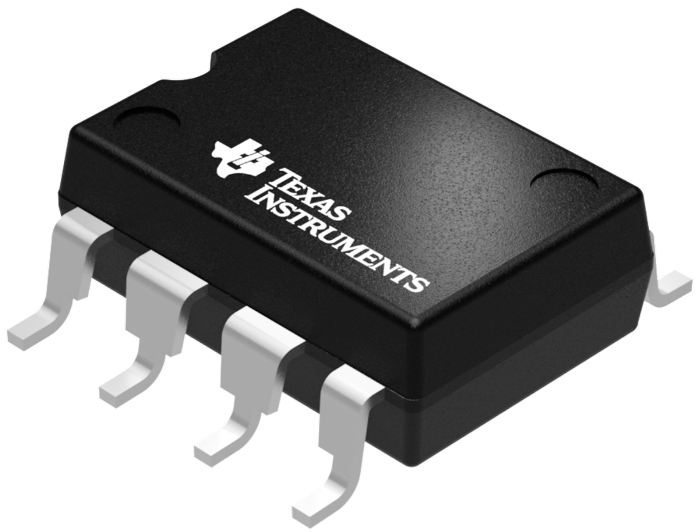
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1100DUBR	SOP	DUB	8	350	330.0	24.4	10.9	10.01	5.85	16.0	24.0	Q1
AMC1100DWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



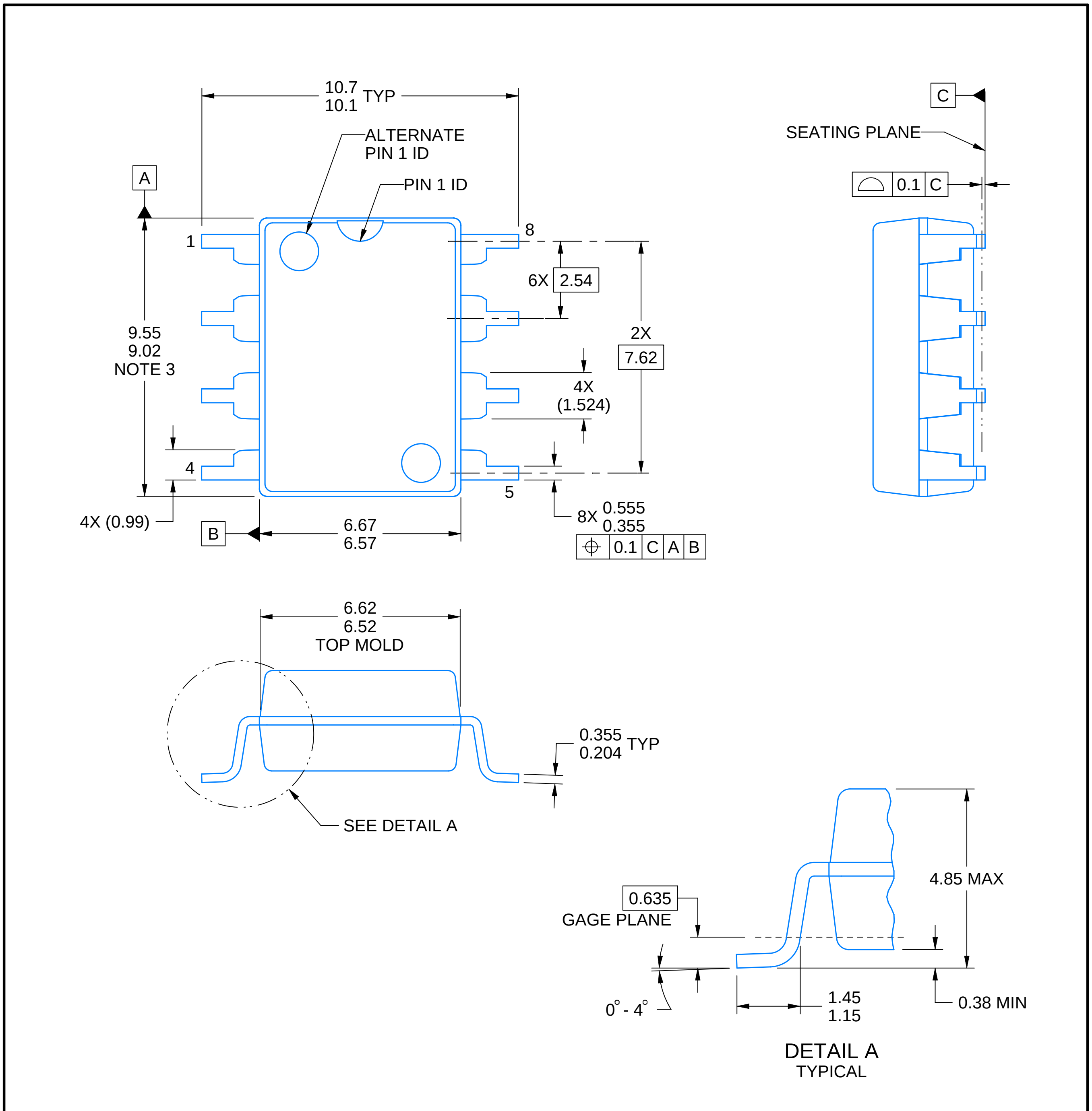
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1100DUBR	SOP	DUB	8	350	346.0	346.0	29.0
AMC1100DWVR	SOIC	DWV	8	1000	367.0	367.0	38.0



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

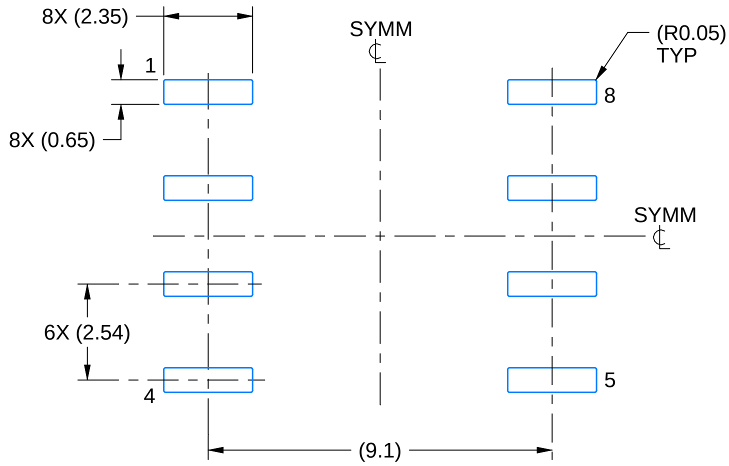
4207614/E



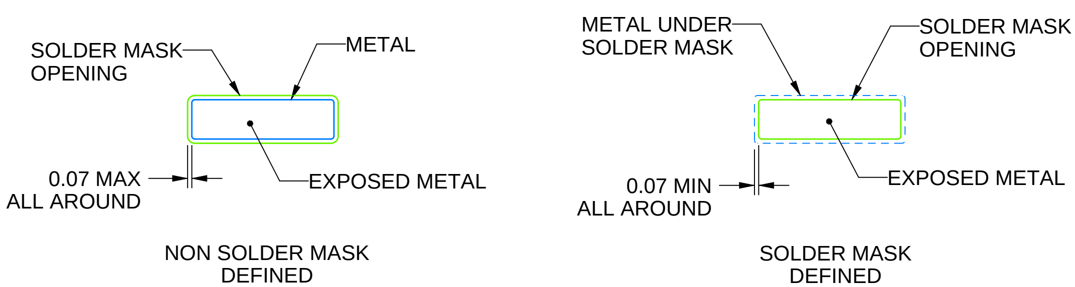
4222355/D 08/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.254 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:5X

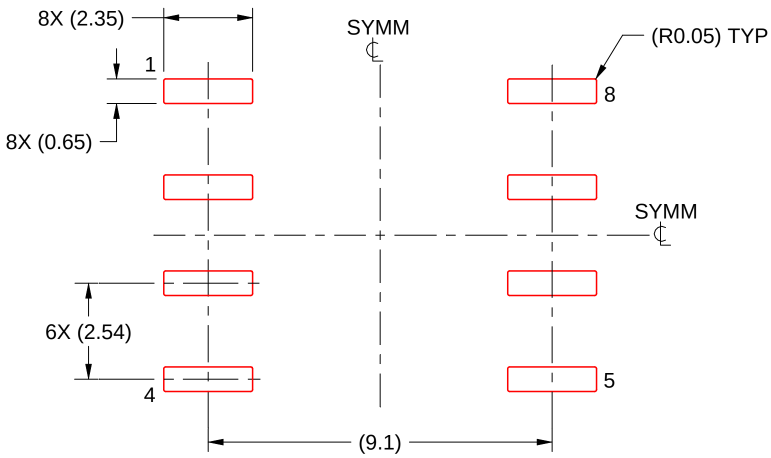


SOLDER MASK DETAILS
NOT TO SCALE

4222355/D 08/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

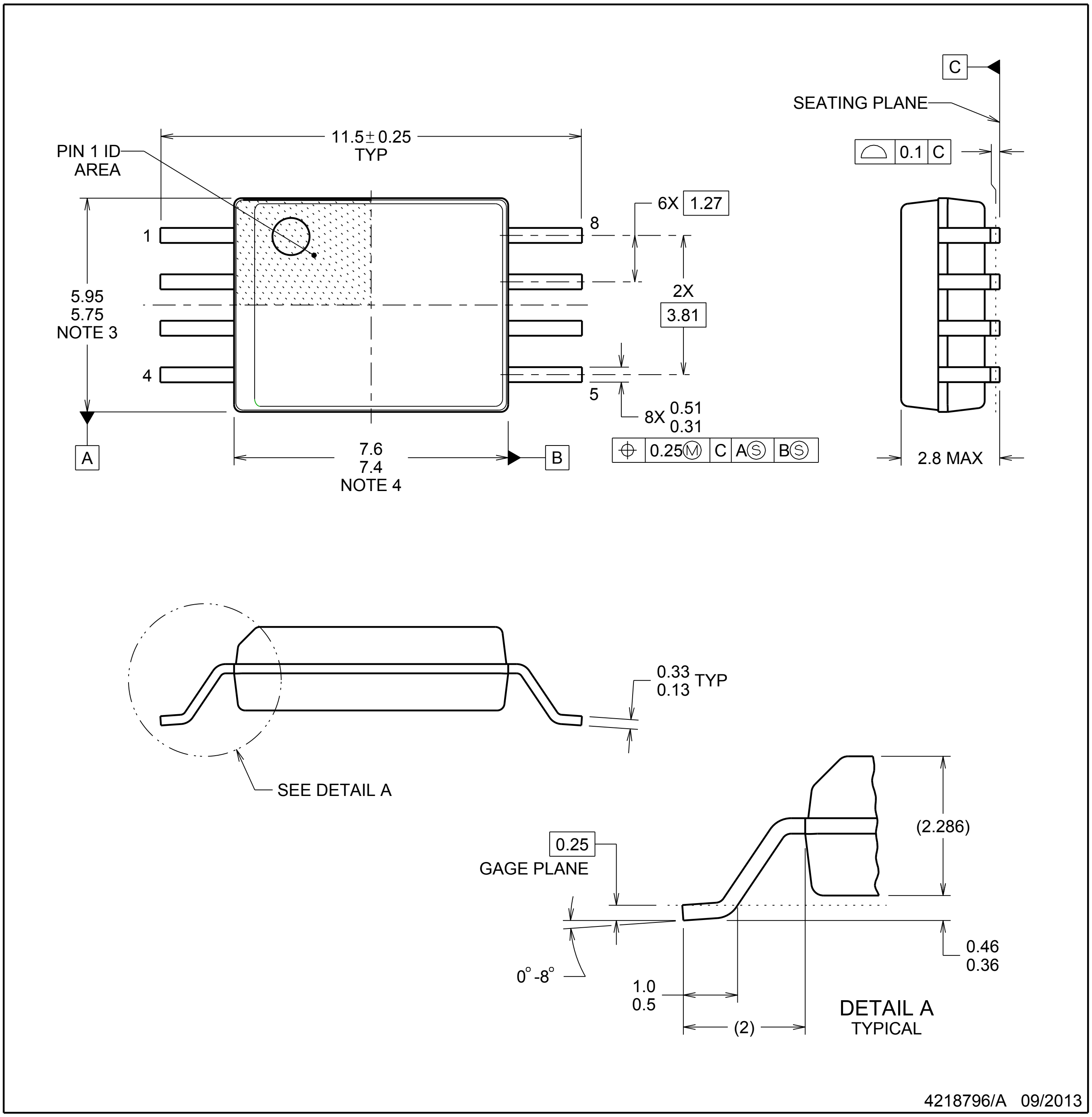


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:5X

4222355/D 08/2017

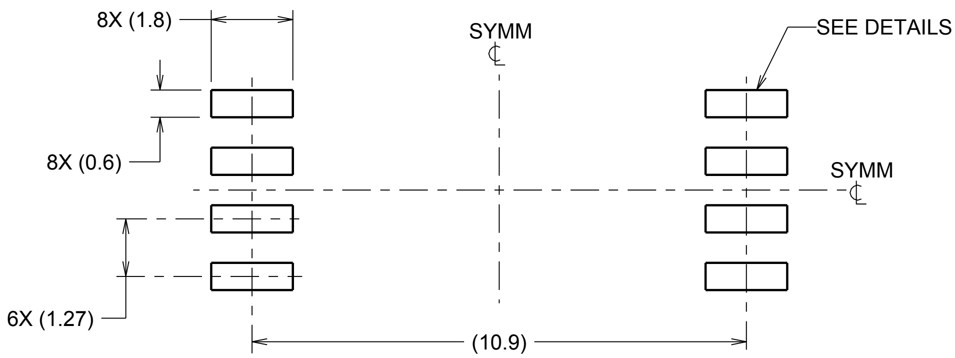
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

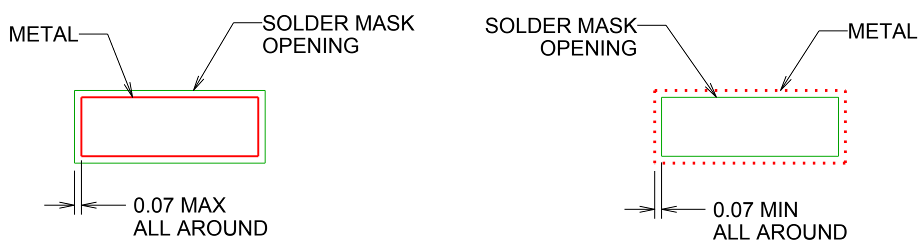


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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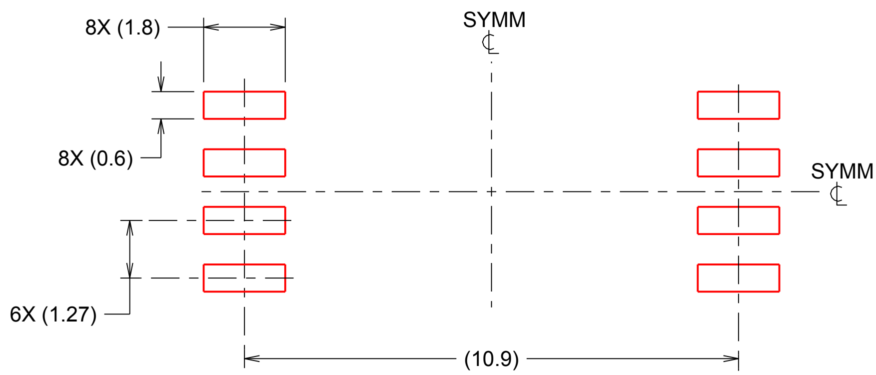
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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