TPS61085 650-kHz,1.2-MHz, 18.5-V Step-Up DC-DC Converter

1 Features

- 2.3 V to 6 V Input Voltage Range
- 18.5-V Boost Converter With 2.0-A Switch Current
- 650-kHz/1.2-MHz Selectable Switching Frequency
- Adjustable Soft-Start
- Thermal Shutdown
- Undervoltage Lockout
- 8-Pin VSSOP Package
- 8-Pin TSSOP Package

2 Applications

- Handheld Devices
- GPS Receivers
- Digital Still Cameras
- Portable Applications
- DSL Modems
- PCMCIA Cards
- TFT LCD Bias Supply

3 Description

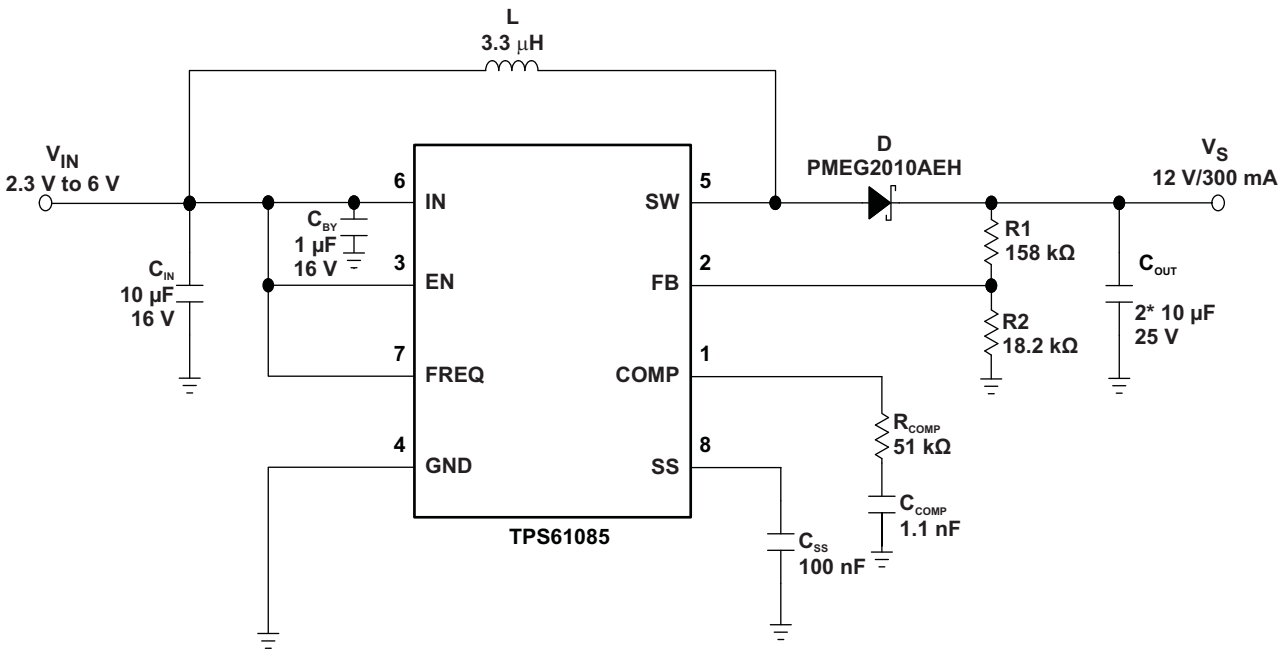
The TPS61085 is a high frequency, high efficiency DC-DC converter with an integrated 2.0-A, 0.13-Ω power switch capable of providing an output voltage up to 18.5 V. The selectable frequency of 650 kHz or 1.2 MHz allows the use of small external inductors and capacitors and provides fast transient response. The external compensation allows optimizing the application for specific conditions. A capacitor connected to the soft-start pin minimizes inrush current at startup.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61085	VSSOP (8)	3.00 mm × 3.00 mm
	TSSOP (8)	3.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



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5 Revision History

Changes from Revision A (April 2012) to Revision B — **Page**

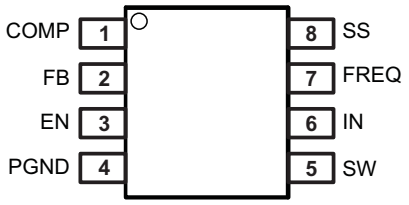
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Original (June 2008) to Revision A — **Page**

- Changed the circuit illustration value of C_{COMP} From: 1.6 nF To: 1.1 nF ... 1
- Deleted Lead Temperature from the Abs Max table ... 3
- Added a conditions statement and two new graphs (Max Load Current vs Input Voltage) to the Typical Characteristics graphs ... 5
- Added three paragraphs of text to the Detailed Description. ... 7
- Changed Figure 8 to Figure 17 ... 9
- Changed the Design Procudures step 3 details following Equation 4 ... 10
- Changed text in the Inductor Selection section "inductor current ripple is below 20%" to " inductor current ripple is below 35%" ... 10
- Changed Equation 8 ... 12
- Added Used I_{OUT} to Table 5 ... 12
- Added Equation 10 ... 13
- Changed the White LED Applications optional Zener connection for Figure 19 to Figure 21 ... 17

6 Pin Configuration and Functions

DGK, PW Packages
8 Pins
Top View



8-PIN 4.9-mm × 3-mm × 1.1-mm VSSOP (DGK)

8-PIN 6.4-mm × 3-mm × 1.2-mm TSSOP (PW)

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
COMP	1	I/O	Compensation pin
EN	3	I	Shutdown control input. Connect this pin to logic high level to enable the device
FB	2	I	Feedback pin
FREQ	7	I	Frequency select pin. The power switch operates at 650 kHz if FREQ is connected to GND and at 1.2 MHz if FREQ is connected to IN
IN	6	I	Input supply pin
PGND	4		Power ground
SS	8	O	Soft-start control pin. Connect a capacitor to this pin if soft-start needed. Open = no soft-start
SW	5	I	Switch pin

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Input voltage range IN	–0.3	7	V
Voltage range on pins EN, FB, SS, FREQ, COMP	–0.3	7	V
Voltage on pin SW	-0.3	20	V
Continuous power dissipation	See *Thermal Information*		
Operating junction temperature	–40	150	°C
Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	
		Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±XXX V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±YYY V may actually have higher performance.

7.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	2.3		6	V
V_S	Boost output voltage range	V_{IN} + 0.5		18.5	V
T_A	Operating free-air temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS61085		UNIT
		DGK	PW	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	189.3	183.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57.1	66.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	109.9	112.0	
ψ_{JT}	Junction-to-top characterization parameter	3.5	8.3	
ψ_{JB}	Junction-to-board characterization parameter	108.3	110.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

V_{IN} = 3.3 V, EN = V_{IN}, V_S = 12 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		2.3		6	V
I_Q	Operating quiescent current into IN	Device not switching, V_{FB} = 1.3 V		70	100	µA
I_{SDVIN}	Shutdown current into IN	EN = GND			1	µA
UVLO	Undervoltage lockout threshold	V_{IN} falling			2.2	V
		V_{IN} rising			2.3	V
T_{SD}	Thermal shutdown	Temperature rising		150		°C
$T_{SD(HYS)}$	Thermal shutdown hysteresis			14		°C
LOGIC SIGNALS EN, FREQ						
V_{IH}	High level input voltage	V_{IN} = 2.3 V to 6 V	2			V
V_{IL}	Low level input voltage	V_{IN} = 2.3 V to 6 V			0.5	V
I_{lkg}	Input leakage current	EN = FREQ = GND			0.1	µA
BOOST CONVERTER						
V_S	Boost output voltage		V_{IN} + 0.5		18.5	V
V_{FB}	Feedback regulation voltage		1.230	1.238	1.246	V
gm	Transconductance error amplifier			107		µA/V
I_{FB}	Feedback input bias current	V_{FB} = 1.238 V			0.1	µA
$r_{DS(on)}$	N-channel MOSFET on-resistance	V_{IN} = V_{GS} = 5 V, I_{SW} = current limit		0.13	0.20	Ω
		V_{IN} = V_{GS} = 3.3V, I_{SW} = current limit		0.15	0.24	
I_{lkg}	SW leakage current	EN = GND, V_{SW} = 6V TBD			10	µA
I_{LIM}	N-Channel MOSFET current limit		2.0	2.6	3.2	A
I_{SS}	Soft-start current	V_{SS} = 1.238 V	7	10	13	µA
f_S	Oscillator frequency	FREQ = V_{IN}	0.9	1.2	1.5	MHz
		FREQ = GND	480	650	820	kHz
	Line regulation	V_{IN} = 2.3 V to 6 V, I_{OUT} = 10 mA		0.0002		%/V
	Load regulation	V_{IN} = 3.3 V, I_{OUT} = 1 mA to 400 mA		0.11		%/A

7.6 Typical Characteristics

The typical characteristics are measured with the inductors 7447789003 3.3 µH (high frequency) or B82464G4 6.8 µH (low frequency) from Epcos and the rectifier diode SL22.

Table 1. Table Of Graphs

			FIGURE
$I_{OUT(max)}$	Maximum load current	vs Input voltage at high frequency (1.2 MHz)	Figure 1
		vs Input voltage at low frequency (650 kHz)	Figure 2
η	Efficiency	vs Load current, V_S = 12 V, V_{IN} = 3.3 V	Figure 3
		vs Load current, V_S = 9 V, V_{IN} = 3.3 V	Figure 4
	Supply current	vs Supply voltage	Figure 5
	Frequency	vs Load current	Figure 6
	Frequency	vs Supply voltage	Figure 7

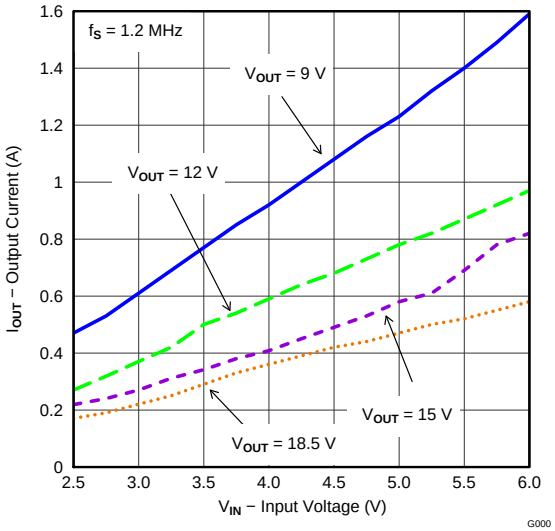


Figure 1. Maximum Load Current vs Input Voltage

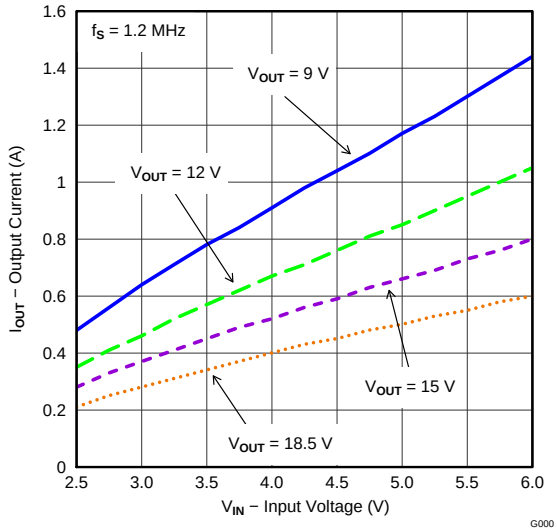


Figure 2. Maximum Load Current vs Input Voltage

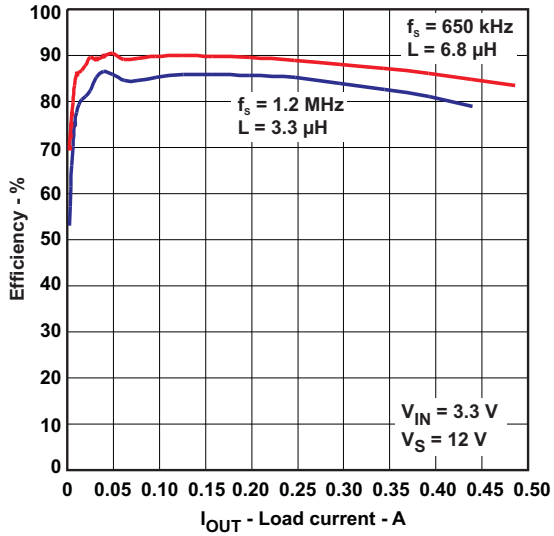


Figure 3. Efficiency vs Load Current

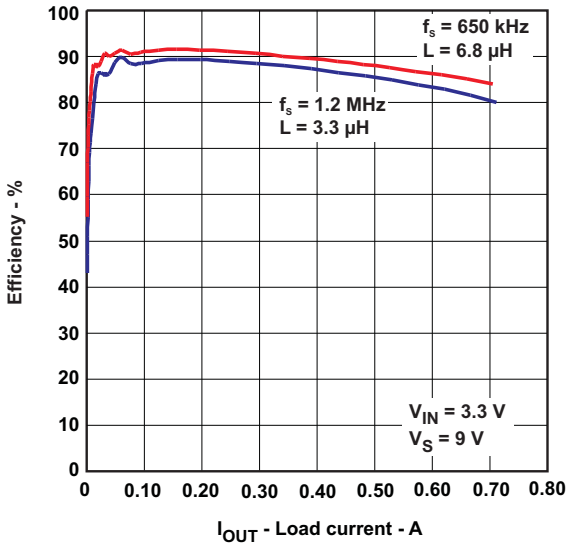


Figure 4. Efficiency vs Load Current

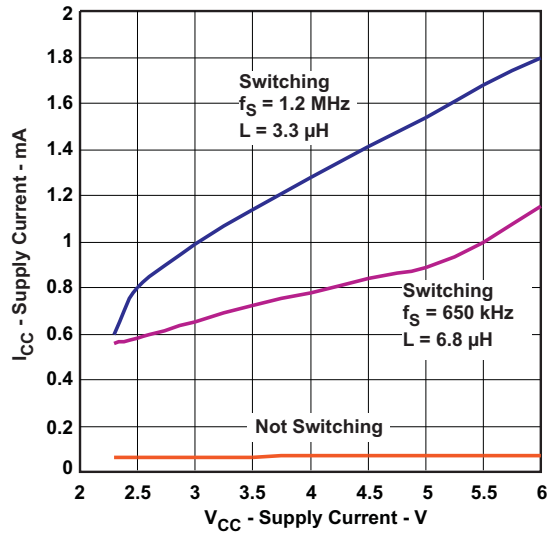


Figure 5. Supply Current vs Supply Voltage

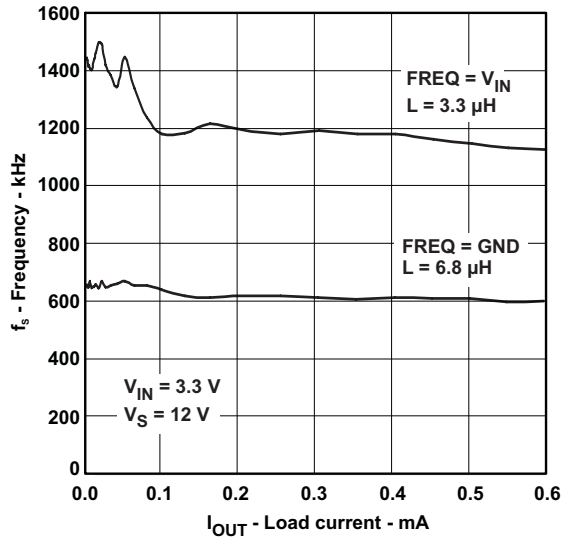


Figure 6. Frequency vs Load Current

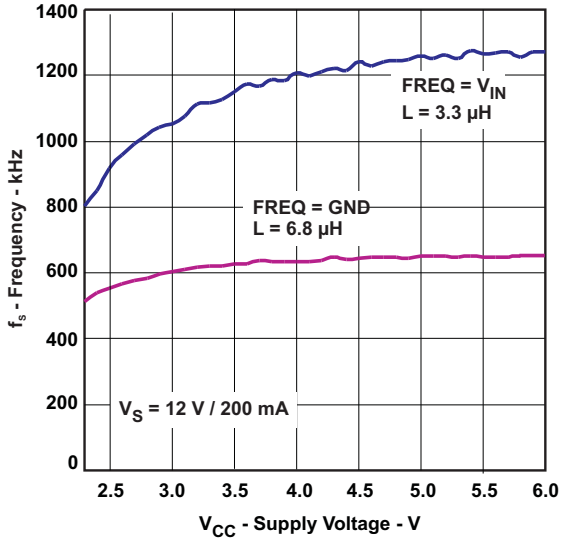


Figure 7. Frequency vs Supply Voltage

8 Detailed Description

8.1 Overview

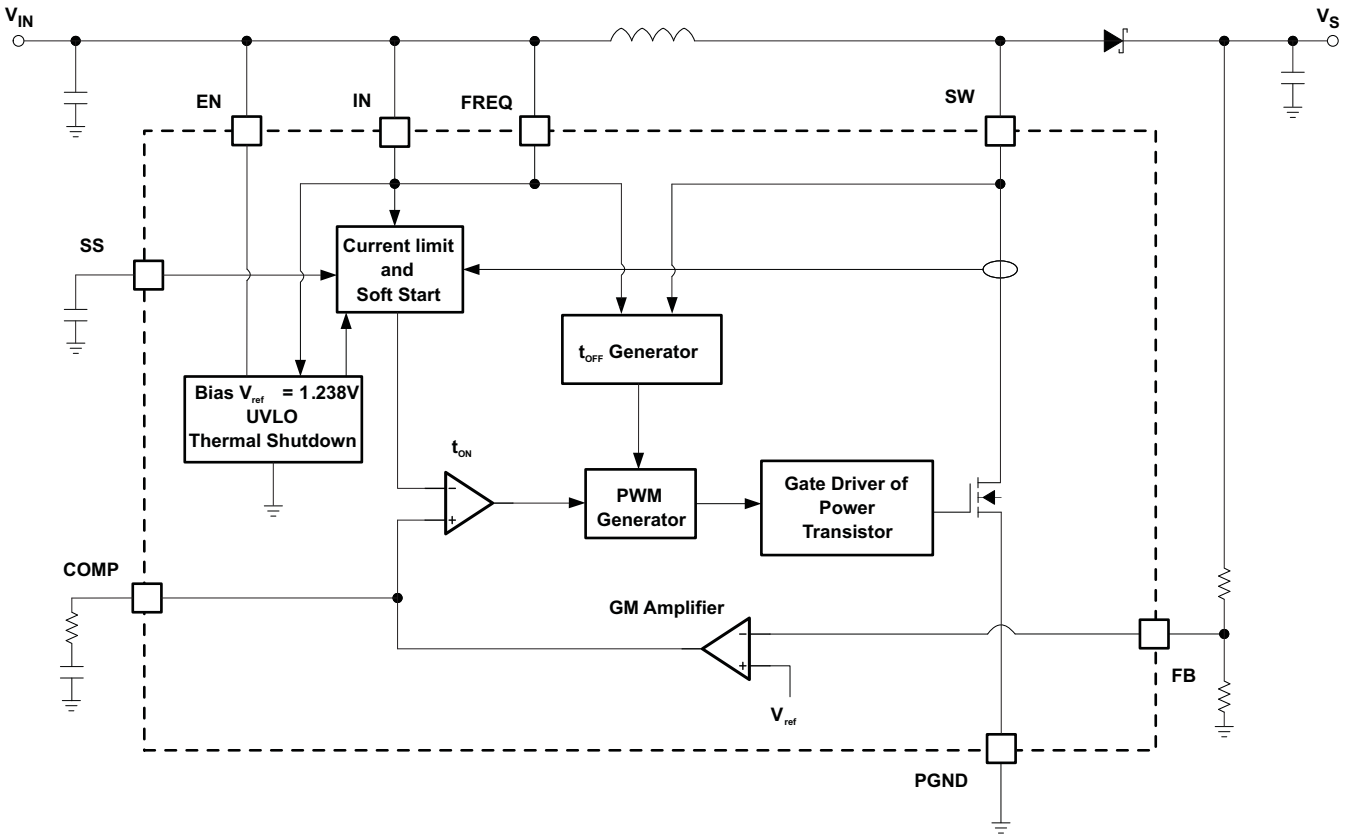
The boost converter is designed for output voltages up to 18.5 V with a switch peak current limit of 2.0 A minimum. The device, which operates in a current mode scheme with quasi-constant frequency, is externally compensated for maximum flexibility and stability. The switching frequency is selectable between 650 kHz and 1.2 MHz and the minimum input voltage is 2.3 V. To control the inrush current at start-up a soft-start pin is available.

TPS61085 boost converter's novel topology using adaptive off-time provides superior load and line transient responses and operates also over a wider range of applications than conventional converters.

The selectable switching frequency offers the possibility to optimize the design either for the use of small sized components (1.2 MHz) or for higher system efficiency (650 kHz). However, the frequency changes slightly because the voltage drop across the $r_{DS(on)}$ has some influence on the current and voltage measurement and thus on the on-time (the off-time remains constant).

The converter operates in continuous conduction mode (CCM) as soon as the input current increases above half the ripple current in the inductor, for lower load currents it switches into discontinuous conduction mode (DCM). If the load is further reduced, the part starts to skip pulses to maintain the output voltage.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Soft-Start

The boost converter has an adjustable soft-start to prevent high inrush current during start-up. To minimize the inrush current during start-up an external capacitor connected to the soft-start pin SS and charged with a constant current, is used to slowly ramp up the internal current limit of the boost converter when charged with a constant current. When the EN pin is pulled high, the soft-start capacitor C_{SS} is immediately charged to 0.3 V. The capacitor is then charged at a constant current of 10 µA typically until the output of the boost converter V_S has reached its Power Good threshold (roughly 98% of V_S nominal value). During this time, the SS voltage directly controls the peak inductor current, starting with 0 A at V_{SS} = 0.3 V up to the full current limit at V_{SS} =0.8 V. The maximum load current is available after the soft-start is completed. The larger the capacitor the slower the ramp of the current limit and the longer the soft-start time. A 100 nF capacitor is usually sufficient for most of the applications. When the EN pin is pulled low, the soft-start capacitor is discharged to ground.

8.3.2 Frequency Select Pin (FREQ)

The frequency select pin FREQ allows to set the switching frequency of the device to 650 kHz (FREQ = low) or 1.2 MHz (FREQ = high). Higher switching frequency improves load transient response but reduces slightly the efficiency. The other benefits of higher switching frequency are a lower output ripple voltage. The use of the 1.2 MHz switching frequency is recommended unless light load efficiency is a major concern.

8.3.3 Undervoltage Lockout (UVLO)

To avoid mis-operation of the device at low input voltages an undervoltage lockout is included that disables the device, if the input voltage falls below 2.2 V.

8.3.4 Thermal Shutdown

A thermal shutdown is implemented to prevent damages due to excessive heat and power dissipation. Typically the thermal shutdown threshold happens at a junction temperature of 150°C. When the thermal shutdown is triggered the device stops switching until the temperature falls below typically 136°C. Then the device starts switching again.

8.3.5 Overvoltage Prevention

If overvoltage is detected on the FB pin (typically 3 % above the nominal value of 1.238 V) the part stops switching immediately until the voltage on this pin drops to its nominal value. This prevents overvoltage on the output and secures the circuits connected to the output from excessive overvoltage.

8.4 Device Functional Modes

The converter operates in continuous conduction mode (CCM) as soon as the input current increases above half the ripple current in the inductor, for lower load currents it switches into discontinuous conduction mode (DCM). If the load is further reduced, the part starts to skip pulses to maintain the output voltage.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS61085 is designed for output voltages up to 18.5 V with a switch peak current limit of 2.0 A minimum. The device, which operates in a current mode scheme with quasi-constant frequency, is externally compensated for maximum flexibility and stability. The switching frequency is selectable between 650 kHz and 1.2 MHz, and the input voltage range is 2.3 V to 6.0V. To control the inrush current at start-up a soft-start pin is available. The following section provides a step-by-step design approach for configuring the TPS61085 as a voltage regulating boost converter.

9.2 Typical Application

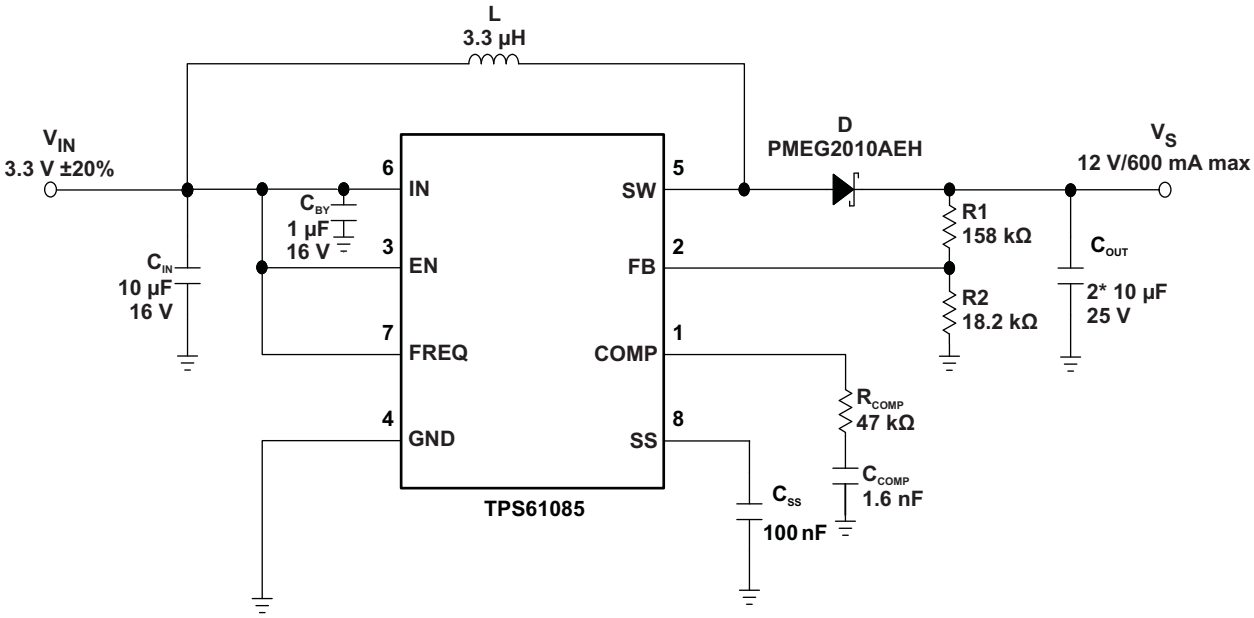


Figure 8. Typical Application, 3.3 V to 12 V (f_S = 1.2 MHz)

9.2.1 Design Requirements

Table 2. TPS61085 12V Output Design Requirements

PARAMETERS	VALUES
Input Voltage	3.3V ± 20%
Output Voltage	12V
Output Current	600mA
Switching Frequency	1.2MHz

9.2.2 Detailed Design Procedure

9.2.2.1 Design Procedure

The first step in the design procedure is to verify that the maximum possible output current of the boost converter supports the specific application requirements. A simple approach is to estimate the converter efficiency, by taking the efficiency numbers from the provided efficiency curves or to use a worst case assumption for the expected efficiency, e.g. 90%.

1. Duty cycle, *D*:

$$D = 1 - \frac{V_{IN} \cdot \eta}{V_S} \tag{1}$$

2. Maximum output current, $I_{OUT(max)}$:

$$I_{OUT(\max)} = \left(I_{LIM(\min)} - \frac{\Delta I_L}{2} \right) \cdot (1 - D) \tag{2}$$

3. Peak switch current in application, $I_{SW(peak)}$:

$$I_{SW(peak)} = \frac{\Delta I_L}{2} + \frac{I_{OUT}}{1 - D} \tag{3}$$

with the inductor peak-to-peak ripple current, ΔI_L

$$\Delta I_L = \frac{V_{IN} \cdot D}{f_S \cdot L} \tag{4}$$

and

V_{IN}	Minimum input voltage
V_S	Output voltage
$I_{LIM(min)}$	Converter switch current limit (minimum switch current limit = 3.2 A)
f_S	Converter switching frequency (typically 1.2 MHz or 650 kHz)
L	Selected inductor value
η	Estimated converter efficiency (please use the number from the efficiency plots or 90% as an estimation)

The peak switch current is the steady state peak switch current that the integrated switch, inductor and external Schottky diode has to be able to handle. The calculation must be done for the minimum input voltage where the peak switch current is the highest.

9.2.2.2 Inductor Selection

The TPS61085 is designed to work with a wide range of inductors. The main parameter for the inductor selection is the saturation current of the inductor which should be higher than the peak switch current as calculated in the *Design Procedure* section with additional margin to cover for heavy load transients. An alternative, more conservative, is to choose an inductor with a saturation current at least as high as the maximum switch current limit of 3.2 A. The other important parameter is the inductor DC resistance. Usually, the lower the DC resistance the higher the efficiency. It is important to note that the inductor DC resistance is not the only parameter determining the efficiency. Especially for a boost converter where the inductor is the energy storage element, the type and core material of the inductor influences the efficiency as well. At high switching frequencies of 1.2 MHz inductor core losses, proximity effects and skin effects become more important. Usually, an inductor with a larger form factor gives higher efficiency. The efficiency difference between different inductors can vary between 2% to 10%. For the TPS61085, inductor values between 3 µH and 6 µH are a good choice with a switching frequency of 1.2 MHz, typically 3.3 µH. At 650 kHz inductors between 6 µH and 13 µH, typically 6.8 µH are recommended. Possible inductors are shown in Table 3.

Typically, it is recommended that the inductor current ripple is below 35% of the average inductor current. Therefore, the following equation can be used to calculate the inductor value, *L*:

$$L = \left(\frac{V_{IN}}{V_S}\right)^2 \cdot \left(\frac{V_S - V_{IN}}{I_{OUT} \cdot f_S}\right) \cdot \left(\frac{\eta}{0.35}\right) \quad (5)$$

with

V_{IN}	Minimum input voltage
V_S	Output voltage
I_{out}	Maximum output current in the application
f_S	Converter switching frequency (typically 1.2 MHz or 650 kHz)
η	Estimated converter efficiency (please use the number from the efficiency plots or 90% as an estimation)

Table 3. Inductor Selection

L (µH)	SUPPLIER	COMPONENT CODE	SIZE (L×W×H mm)	DCR TYP (mΩ)	Isat (A)
1.2 MHz					
3.3	Sumida	CDH38D09	4 x 4 x 1	240	1.25
4.7	Sumida	CDPH36D13	5 × 5 × 1.5	155	1.36
3.3	Sumida	CDPH4D19F	5.2 x 5.2 x 2	33	1.5
3.3	Sumida	CDRH6D12	6.7 x 6.7 x 1.5	62	2.2
4.7	Würth Elektronik	7447785004	5.9 × 6.2 × 3.3	60	2.5
5	Coilcraft	MSS7341	7.3 × 7.3 × 4.1	24	2.9
650 kHz					
6.8	Sumida	CDP14D19	5.2 x 5.2 x 2	50	1
10	Coilcraft	LPS4414	4.3 × 4.3 × 1.4	380	1.2
6.8	Sumida	CDRH6D12/LD	6.7 x 6.7 x 1.5	95	1.25
10	Sumida	CDR6D23	5 × 5 × 2.4	133	1.75
10	Würth Elektronik	744778910	7.3 × 7.3 × 3.2	51	2.2
6.8	Sumida	CDRH6D26HP	7 x 7 x 2.8	52	2.9

9.2.2.3 Rectifier Diode Selection

To achieve high efficiency, a Schottky type should be used for the rectifier diode. The reverse voltage rating should be higher than the maximum output voltage of the converter. The averaged rectified forward current I_{avg}, the Schottky diode needs to be rated for, is equal to the output current I_{OUT}:

$$I_{avg} = I_{OUT} \quad (6)$$

Usually a Schottky diode with 2 A maximum average rectified forward current rating is sufficient for most applications. The Schottky rectifier can be selected with lower forward current capability depending on the output current I_{out} but has to be able to dissipate the power. The dissipated power, P_D , is the average rectified forward current times the diode forward voltage, $V_{forward}$.

$$P_D = I_{avg} \cdot V_{forward} \quad (7)$$

Typically the diode should be able to dissipate around 500mW depending on the load current and forward voltage.

Table 4. Rectifier Diode Selection

CURRENT RATING Iavg	Vr	$V_{forward}$ / Iavg	SUPPLIER	COMPONENT CODE	PACKAGE TYPE
750 mA	20 V	0.425 V / 750 mA	Fairchild Semiconductor	FYV0704S	SOT 23
1 A	20 V	0.39 V / 1 A	NXP	PMEG2010AEH	SOD 123
1 A	20 V	0.52 V / 1 A	Vishay Semiconductor	B120	SMA
1 A	20 V	0.5 V / 1 A	Vishay Semiconductor	SS12	SMA

Table 4. Rectifier Diode Selection (continued)

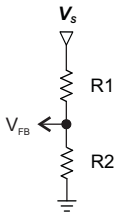
CURRENT RATING Iavg	Vr	$V_{forward\ /\ Iavg}$	SUPPLIER	COMPONENT CODE	PACKAGE TYPE
1 A	20 V	0.44 V / 1 A	Vishay Semiconductor	MSS1P2L	µ-SMP (Low Profile)

9.2.2.4 Setting the Output Voltage

The output voltage is set by an external resistor divider. Typically, a minimum current of 50 µA flowing through the feedback divider gives good accuracy and noise covering. A standard low side resistor of 18 kΩ is typically selected. The resistors are then calculated as:

$$R2 = \frac{V_{FB}}{70\mu A} \approx 18k\Omega \qquad R1 = R2 \cdot \left(\frac{V_S}{V_{FB}} - 1 \right)$$

$$V_{FB} = 1.238V$$



(8)

9.2.2.5 Compensation (COMP)

The regulator loop can be compensated by adjusting the external components connected to the COMP pin. The COMP pin is the output of the internal transconductance error amplifier.

Standard values of R_{COMP} = *13 kΩ* and C_{COMP} = *3.3 nF* will work for the majority of the applications.

See Table 5 for dedicated compensation networks giving an improved load transient response. The following equations can be used to calculate R_{COMP} and C_{COMP} :

$$R_{COMP} = \frac{110 \cdot V_{IN} \cdot V_S \cdot C_{OUT}}{L \cdot I_{OUT}} \qquad C_{COMP} = \frac{V_s \cdot C_{OUT}}{7.5 \cdot I_{OUT} \cdot R_{COMP}}$$

(9)

with

V_{IN}	Minimum input voltage
V_S	Output voltage
C_{out}	Output capacitance
L	Inductor value, e.g. 3.3 µH or 6.8 µH
I_{OUT}	Maximum output current in the application

Make sure that R_{COMP} < *120 kΩ* and C_{COMP}> *820 pF*, independent of the results of the above formulas.

Table 5. Recommended Compensation Network Values at High/Low Frequency

FREQUENCY	L	V_S	V_{IN} ± 20%	R_{COMP}	C_{COMP}	Used I_{OUT}
High (1.2 MHz)	3.3 µH	15 V	5 V	82 kΩ	1.1 nF	0.7A
			3.3 V	75 kΩ	1.6 nF	0.5A
		12 V	5 V	51 kΩ	1.1 nF	0.9A
			3.3 V	47 kΩ	1.6 nF	0.6A
		9 V	5 V	30 kΩ	1.1 nF	1.2A
			3.3 V	27 kΩ	1.6 nF	0.8A
Low (650 kHz)	6.8 µH	15 V	5 V	43 kΩ	2.2 nF	0.7A
			3.3 V	39 kΩ	3.3 nF	0.5A
		12 V	5 V	27 kΩ	2.2 nF	0.9A
			3.3 V	24 kΩ	3.3 nF	0.6A
		9 V	5 V	15 kΩ	2.2 nF	1.2A
			3.3 V	13 kΩ	3.3 nF	0.8A

Table 5 gives conservative R_{COMP} and C_{COMP} values for certain inductors, input and output voltages providing a very stable system. For a faster response time, a higher R_{COMP} value can be used to enlarge the bandwidth, as well as a slightly lower value of C_{COMP} to keep enough phase margin. These adjustments should be performed in parallel with the load transient response monitoring of TPS61087.

9.2.2.6 Input Capacitor Selection

For good input voltage filtering low ESR ceramic capacitors are recommended. TPS61085 has an analog input IN. Therefore, a 1 µF bypass is highly recommended as close as possible to the IC from IN to GND.

One 10 µF ceramic input capacitors are sufficient for most of the applications. For better input voltage filtering this value can be increased. Refer to Table 6 and typical applications for input capacitor recommendations.

9.2.2.7 Output Capacitor Selection

For best output voltage filtering a low ESR output capacitor like ceramic capcaitor is recommended. Two 10 µF ceramic output capacitors (or one 22 µF) work for most of the applications. Higher capacitor values can be used to improve the load transient response. Refer to Table 6 for the selection of the output capacitor.

Table 6. Rectifier Input and Output Capacitor Selection

	CAPACITOR	VOLTAGE RATING	SUPPLIER	COMPONENT CODE
C_{IN}	10 µF/1206	16 V	Taiyo Yuden	EMK212 BJ 106KG
IN bypass	1 µF/0603	16 V	Taiyo Yuden	EMK107 BJ 105KA
C_{OUT}	10 µF/1206	25 V	Taiyo Yuden	TMK316 BJ 106KL

To calculate the output voltage ripple, Equation 10 can be used:

$$\Delta V_C = \frac{V_S - V_{IN}}{V_S \cdot f_S} \cdot \frac{I_{OUT}}{C_{OUT}} \qquad \Delta V_{C\_ESR} = I_{L(peak)} \cdot R_{C\_ESR} \tag{10}$$

with

ΔV_C	Output voltage ripple dependent on output capacitance,output current and switching frequency
V_S	Output voltage
V_{IN}	Minimum input voltage of boost converter
f_S	Converter switching frequency (typically 1.2 MHz or 650 kHz)
I_{out}	Output capacitance
ΔV_{C_ESR}	Output voltage ripple due to output capacitors ESR (equivalent series resistance)
I_{SWPEAK}	Inductor peak switch current in the application
R_{C_ESR}	Output capacitors equivalent series resistance (ESR)

ΔV_{C_ESR} can be neglected in many cases since ceramic capacitors provide low ESR.

9.2.3 Application Curves

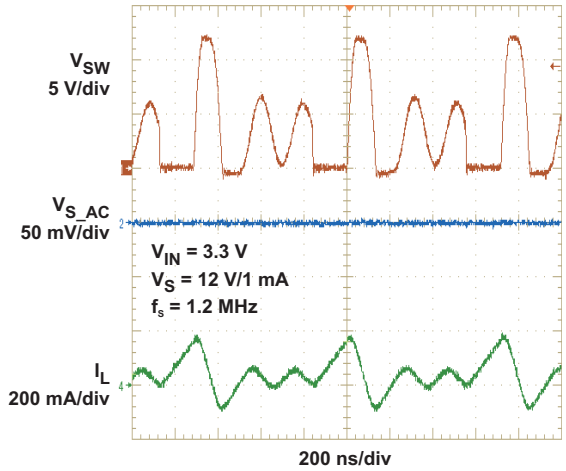


Figure 9. PWM Switching Discontinuous Conduction Mode

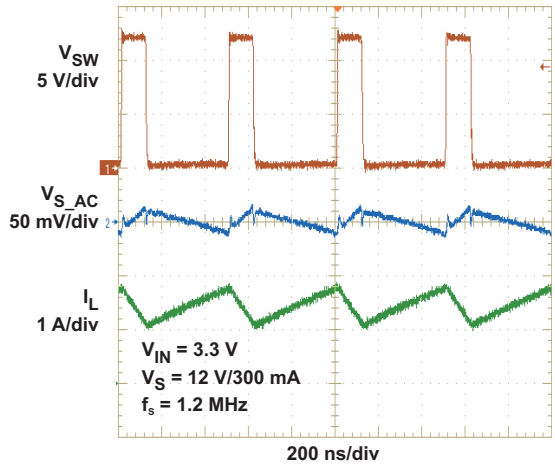


Figure 10. PWM Switching Continuous Conduction Mode

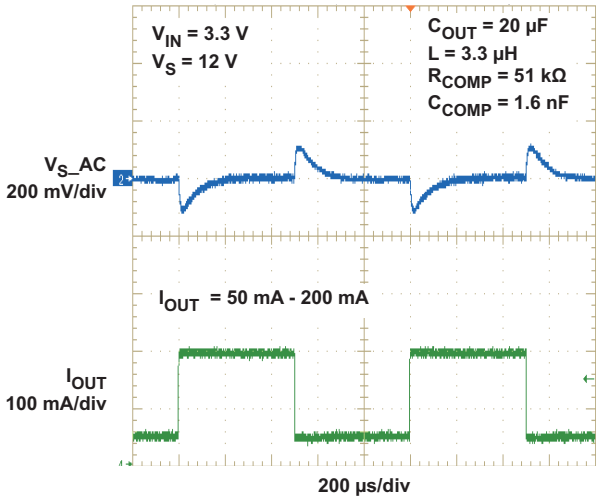


Figure 11. Load Transient Response High Frequency (1.2 MHz)

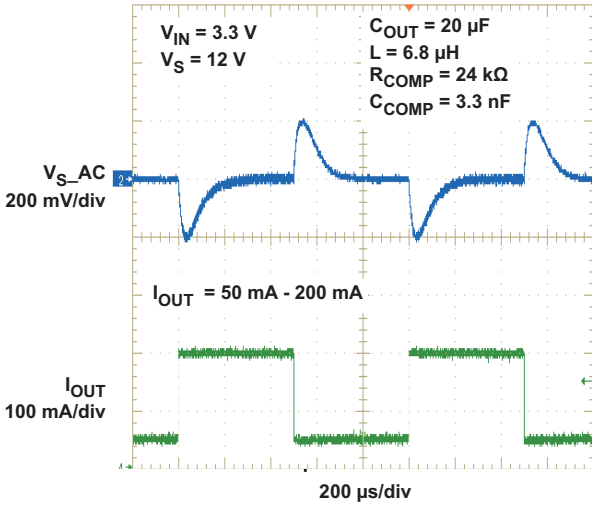


Figure 12. Load Transient Response Low Frequency (650 kHz)

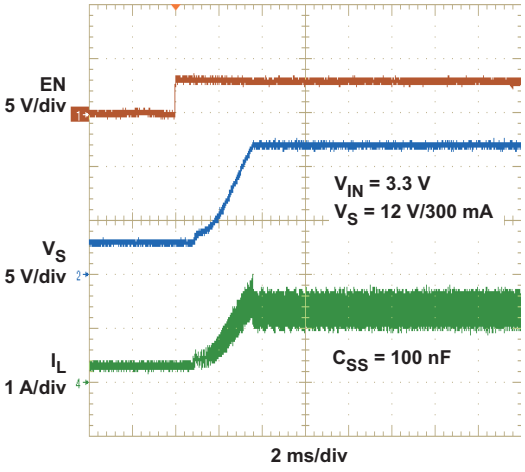


Figure 13. Soft-Start

9.3 System Examples

9.3.1 General Boost Application Circuits

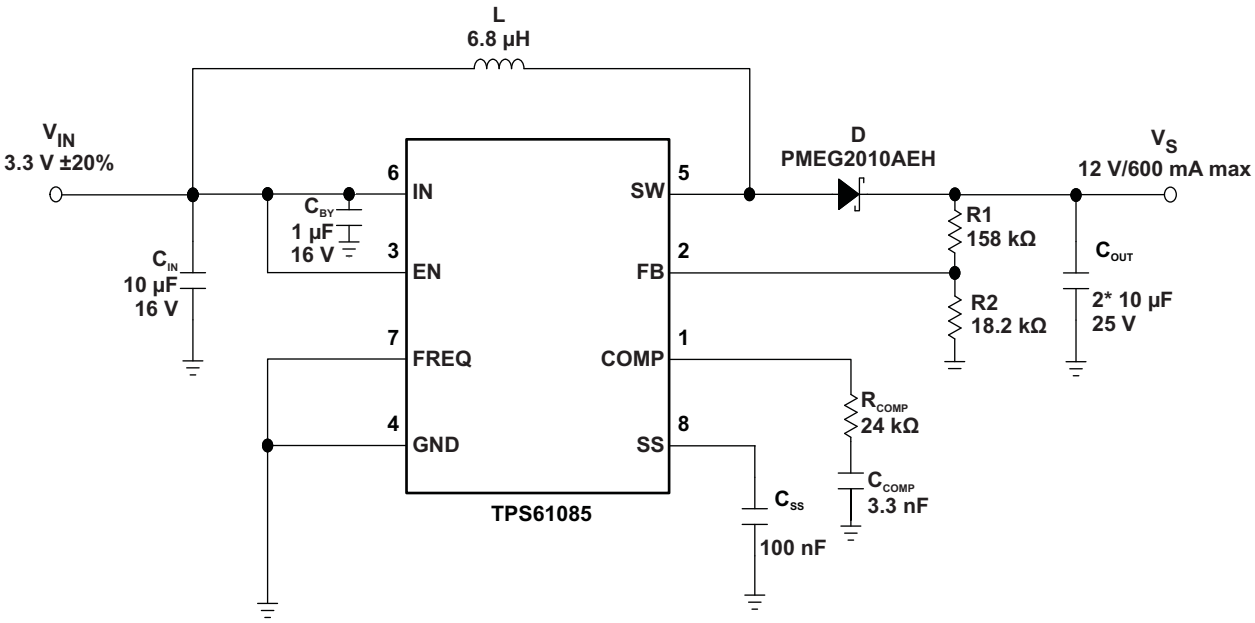


Figure 14. Typical Application, 3.3 V to 12 V (f_S = 650 kHz)

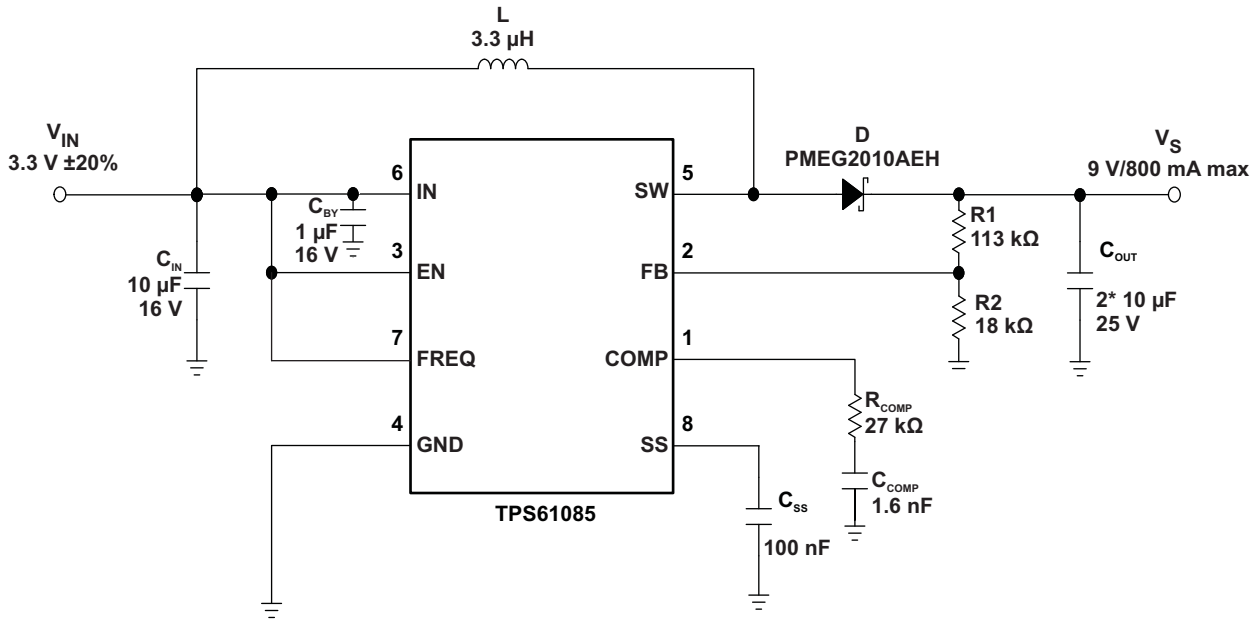


Figure 15. Typical Application, 3.3 V to 9 V (f_S = 1.2 MHz)

System Examples (continued)

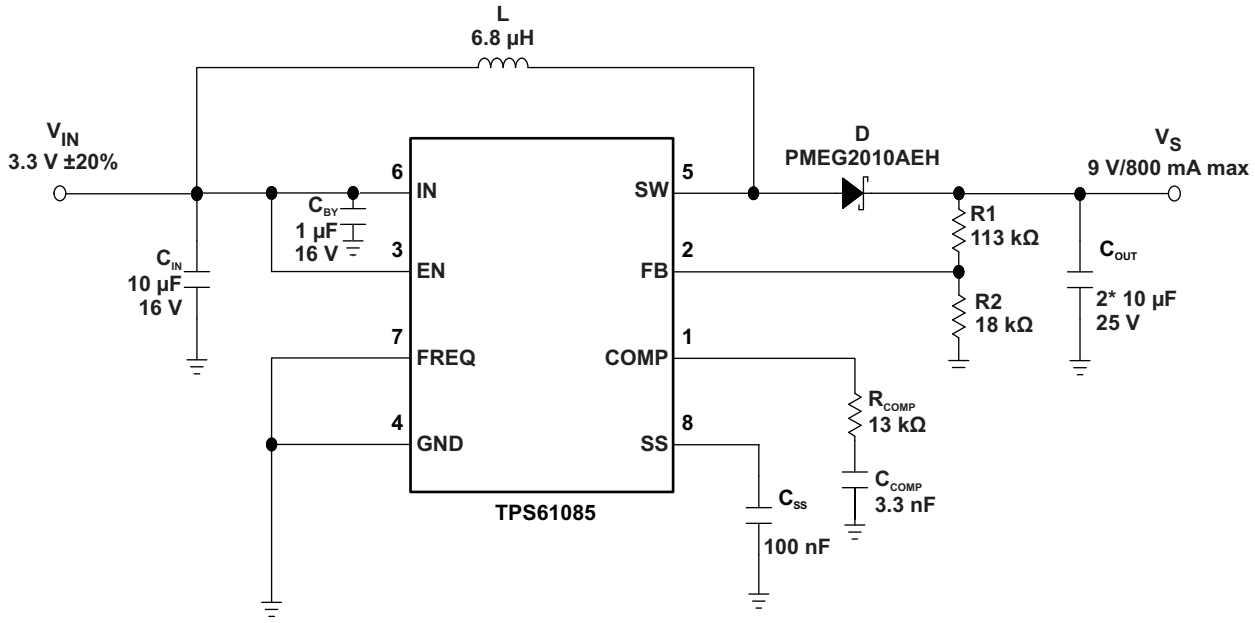


Figure 16. Typical Application, 3.3 V to 9 V (f_S = 650 kHz)

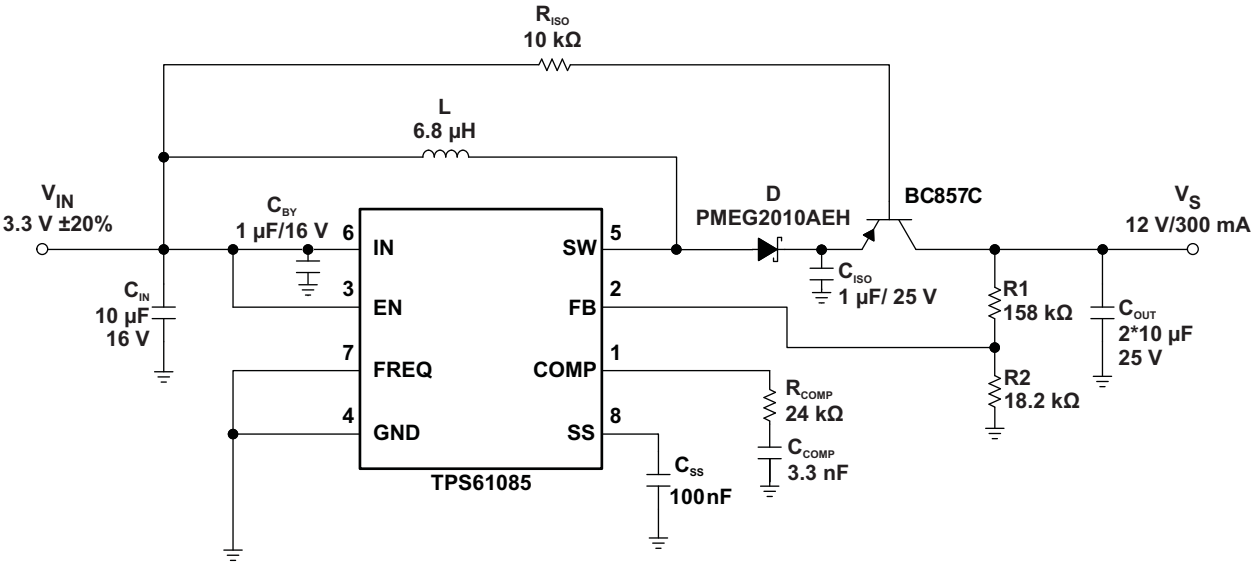


Figure 17. Typical Application With External Load Disconnect Switch

System Examples (continued)

9.3.2 TFT LCD Application Circuit

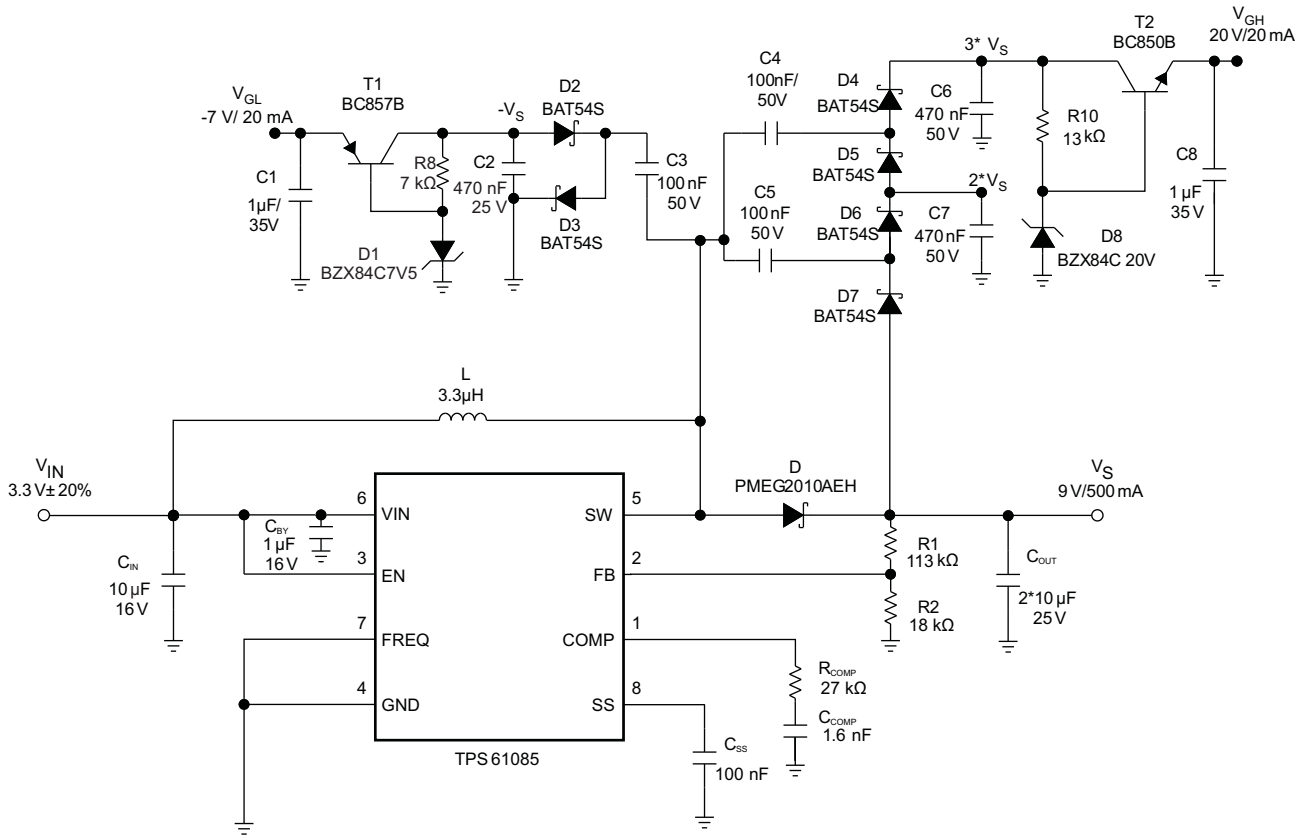


Figure 18. Typical Application 3.3 V to 9 V (f_S = 1.2 MHz) for TFT LCD With External Charge Pumps (VGH, VGL)

9.3.3 WHITE LED Application Circuits

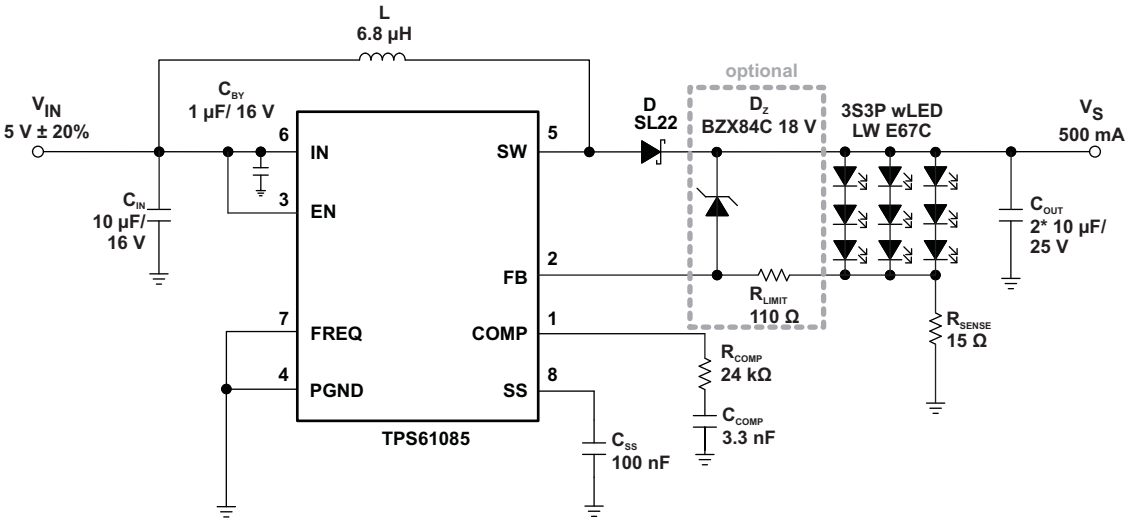


Figure 19. Simple Application (3.3 V Input - f_{sw} = 650 kHz) for wLED Supply (3S3P) (With Optional Clamping Zener Diode)

System Examples (continued)

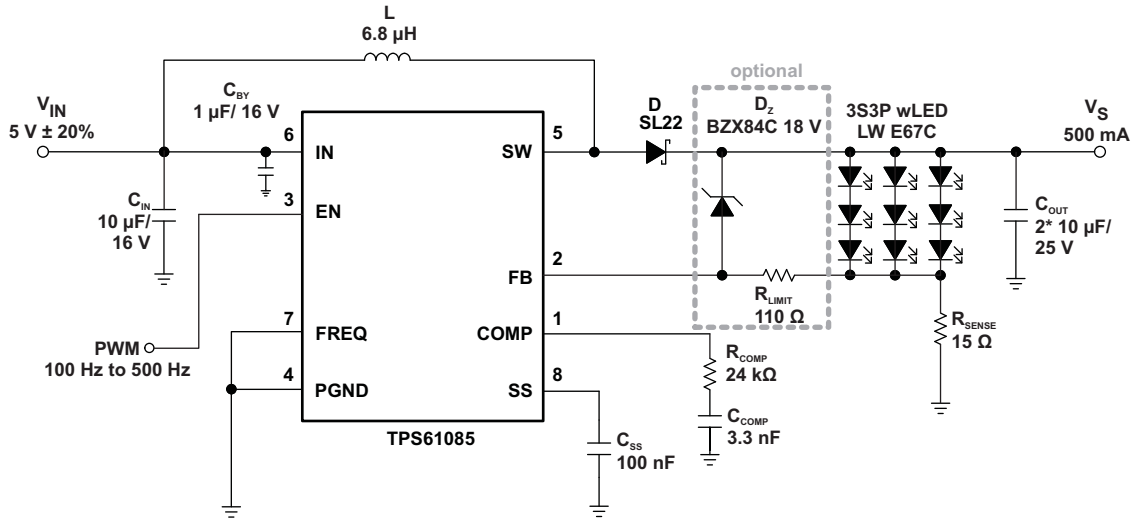


Figure 20. Simple Application (3.3V Input - f_{SW} = 650 kHz) for wLED Supply (3S3P) With Adjustable Brightness Control Using a PWM Signal on the Enable Pin (With Optional Clamping Zener Diode)

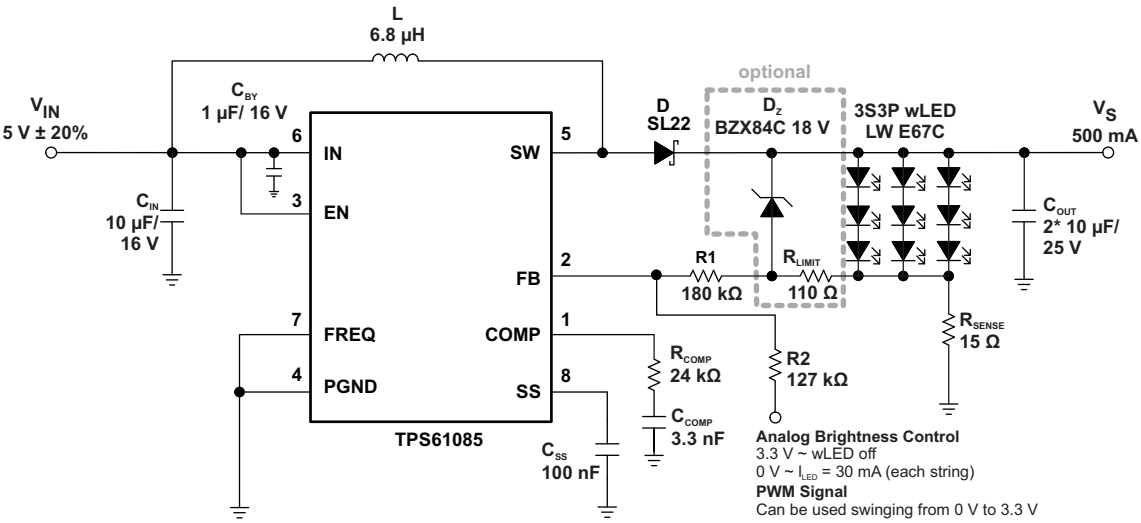


Figure 21. Simple Application (3.3 V Input - f_{SW} = 650 kHz) for wLED Supply (3S3P) With Adjustable Brightness Control Using an Analog Signal on the Feedback Pin (With Optional Clamping Zener Diode)

10 Power Supply Recommendations

The TPS61085 is designed to operate from an input voltage supply range between 2.3 V and 6.0 V. The power supply to the TPS61085 needs to have a current rating according to the supply voltage, output voltage and output current of the TPS61085.

11 Layout

11.1 Layout Guidelines

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at the GND terminal of the IC. The most critical current path for all boost converters is from the switching FET, through the rectifier diode, then the output capacitors, and back to ground of the switching FET. Therefore, the output capacitors and their traces should be placed on the same board layer as the IC and as close as possible between the IC's SW and GND terminal.

11.2 Layout Example

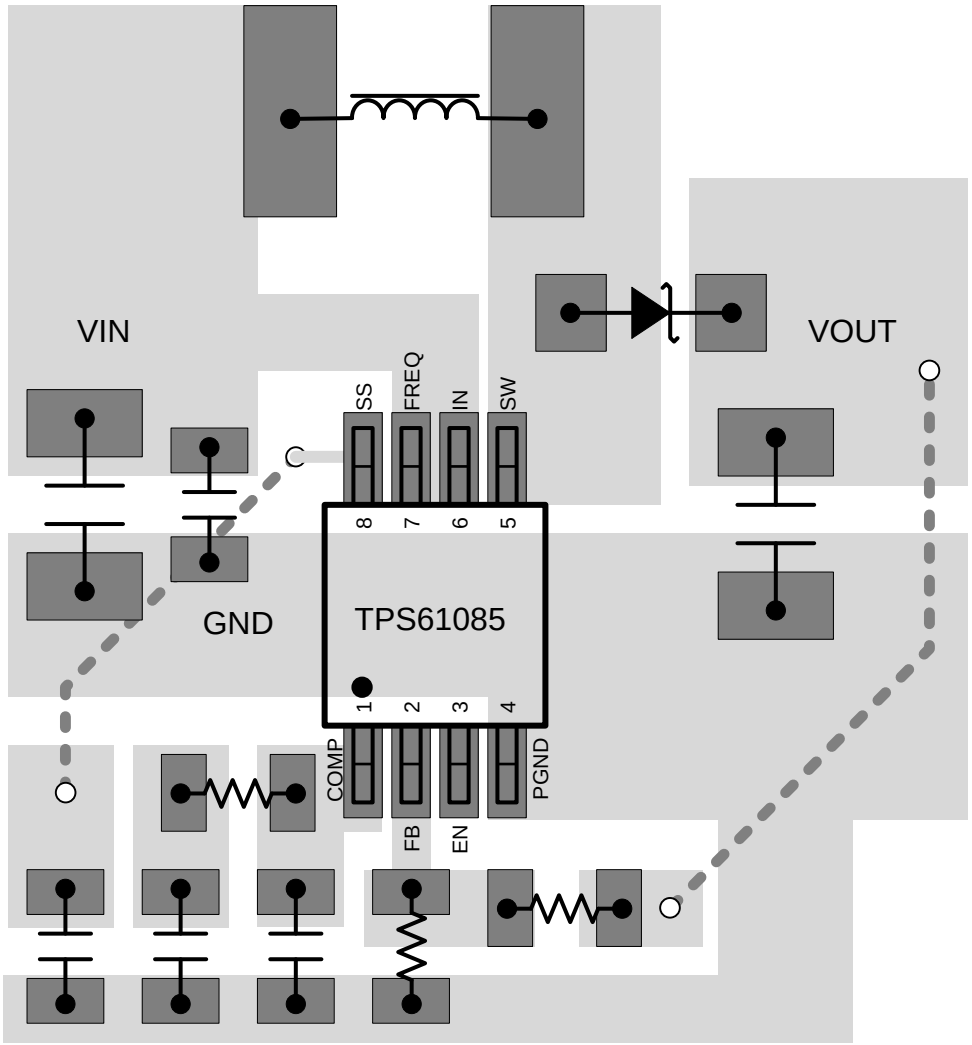


Figure 22. TPS61085 Layout Example

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HPA01142PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	61085	Samples
TPS61085DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PMKI	Samples
TPS61085DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PMKI	Samples
TPS61085DGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PMKI	Samples
TPS61085DGKTG4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PMKI	Samples
TPS61085PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	61085	Samples
TPS61085PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	61085	Samples
TPS61085PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	61085	Samples
TPS61085PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	61085	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS61085 :

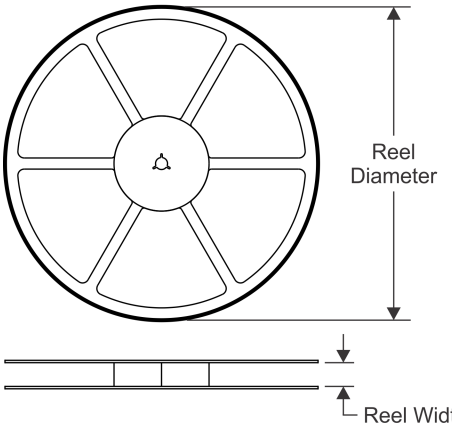
- Automotive: TPS61085-Q1

NOTE: Qualified Version Definitions:

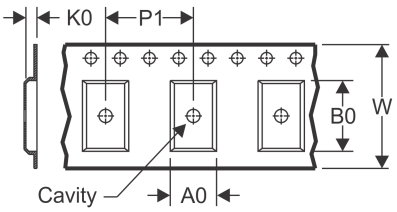
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

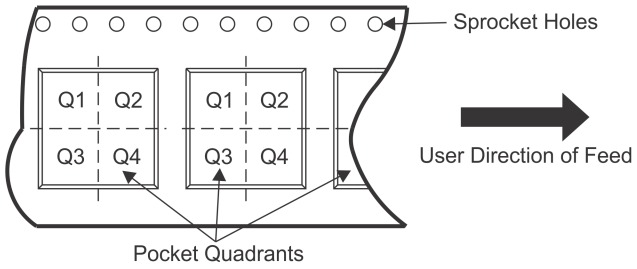


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

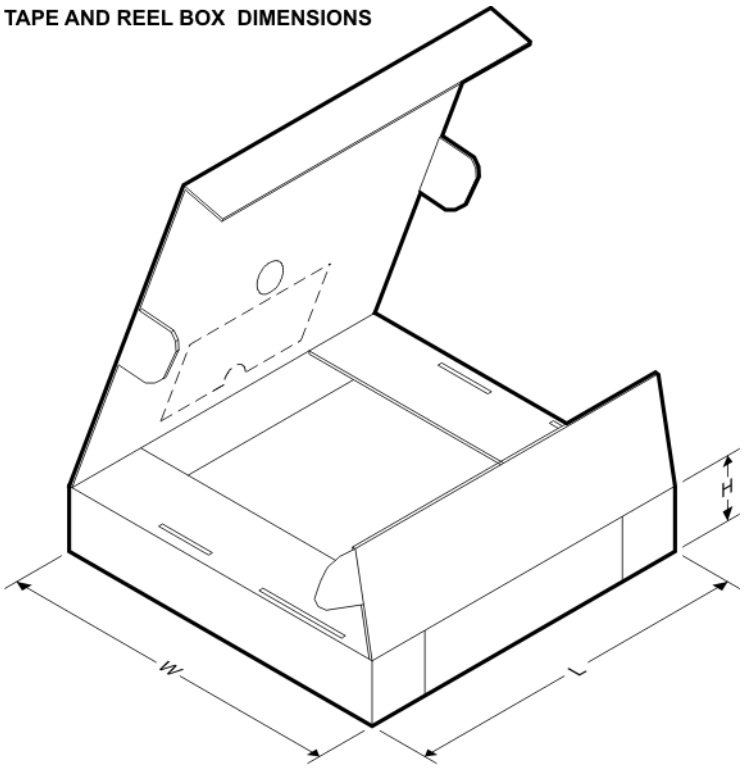
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61085DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS61085DGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS61085PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

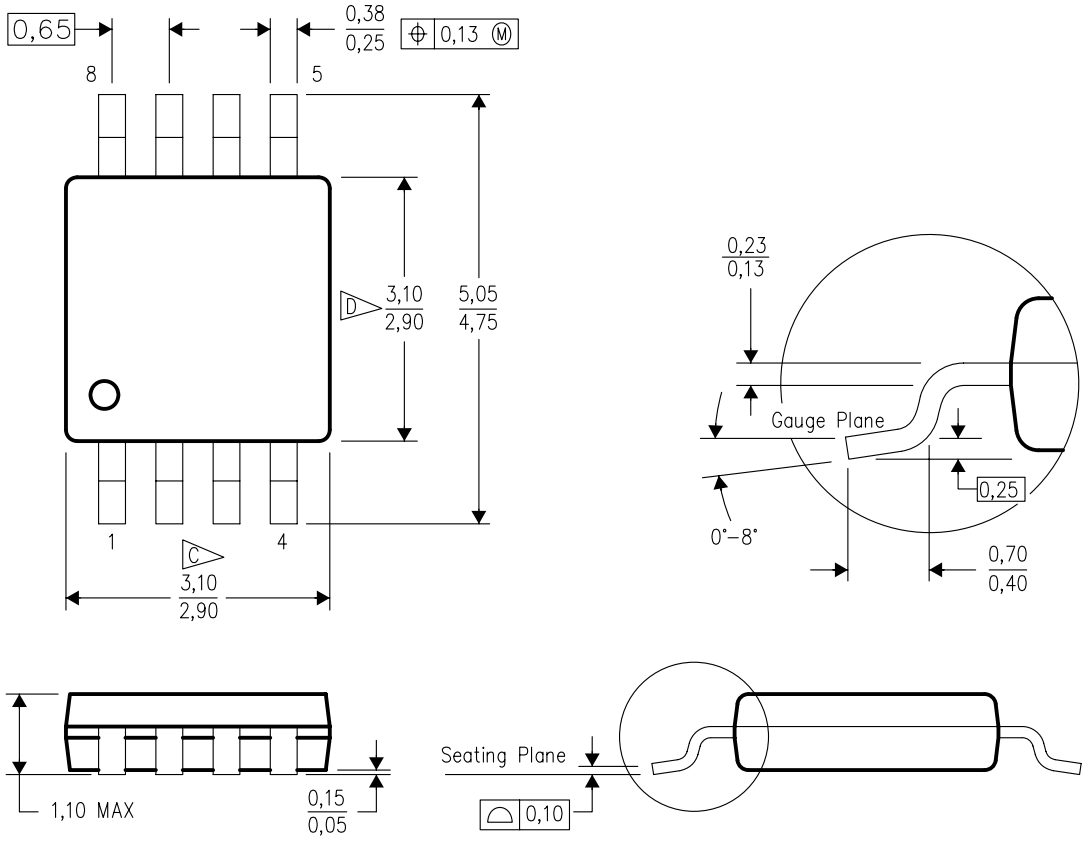
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61085DGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
TPS61085DGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
TPS61085PWR	TSSOP	PW	8	2000	367.0	367.0	35.0

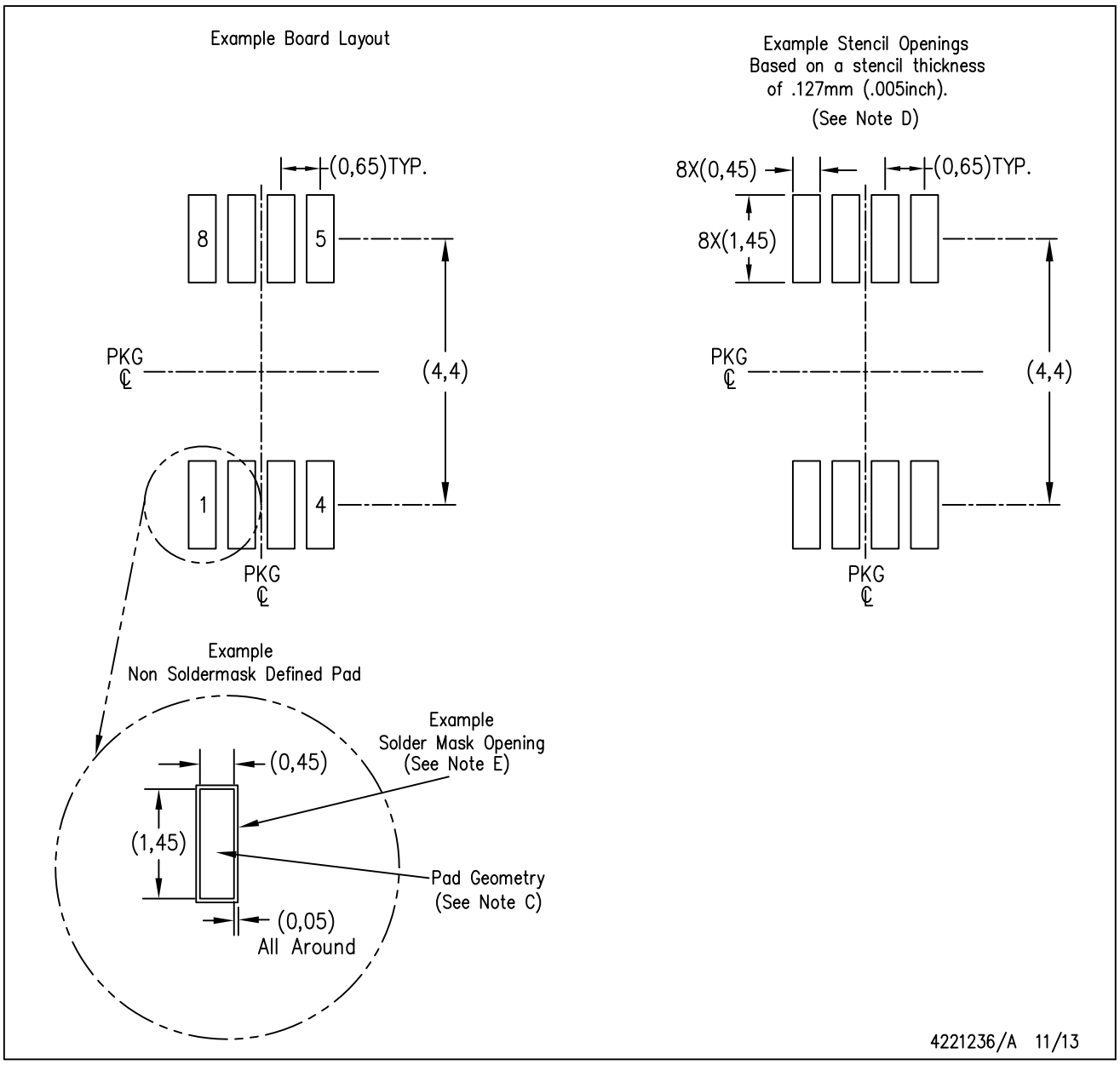
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



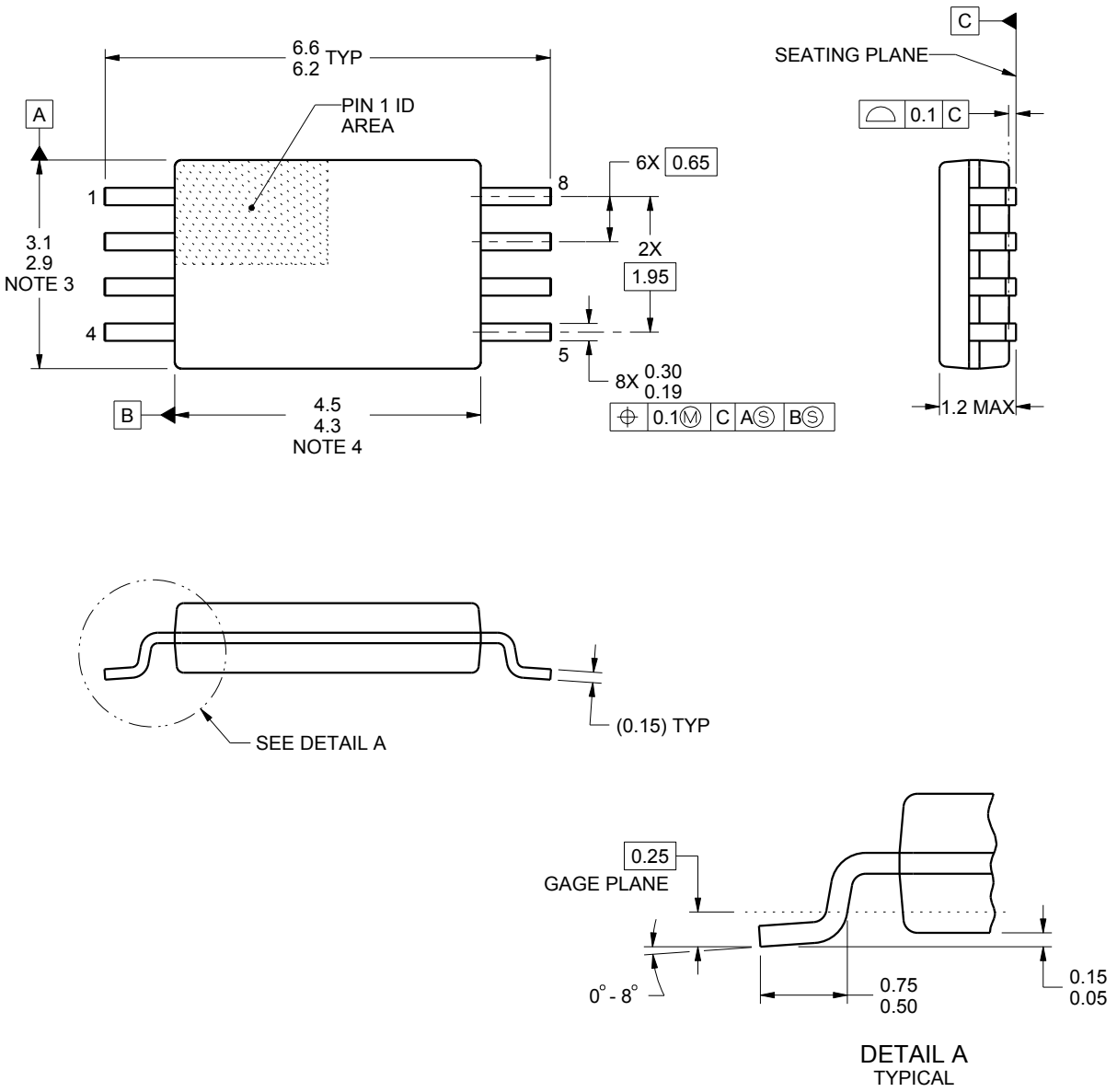
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0008A

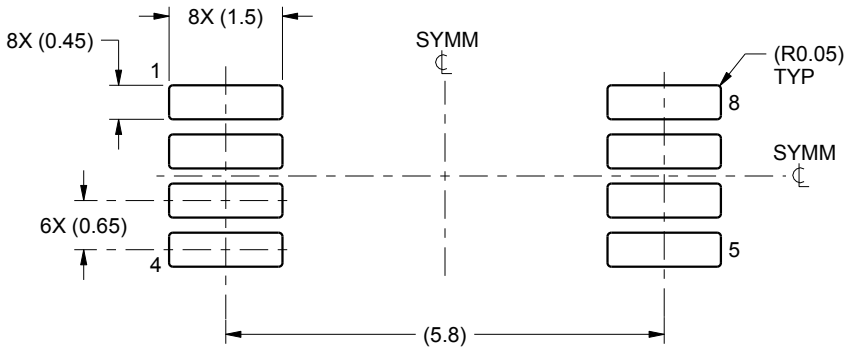
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

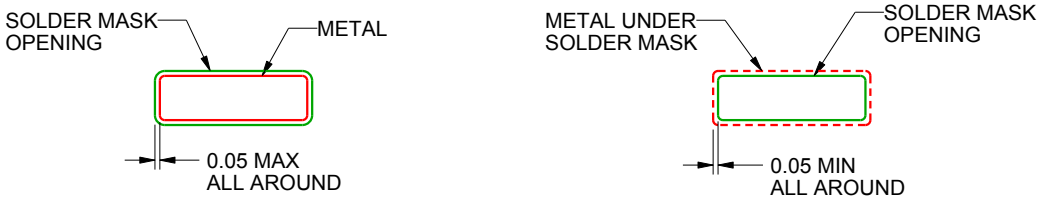


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

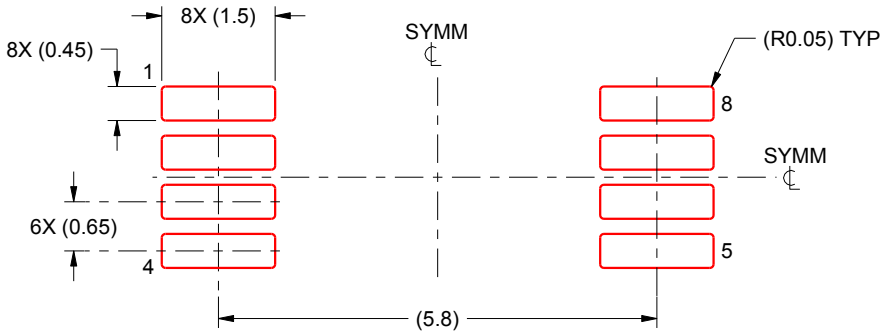


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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