

FEATURES

Low on resistance, 2.5 Ω maximum
<0.65 Ω on-resistance flatness
Dual ± 2.7 V to ± 5.5 V or single +2.7 V to +5.5 V supplies
Rail-to-rail input signal range
Tiny, 6-lead SOT-23; 8-lead MSOP; and 820 $\mu\text{m} \times 2255 \mu\text{m}$ die
Low power consumption
TTL-/CMOS-compatible inputs

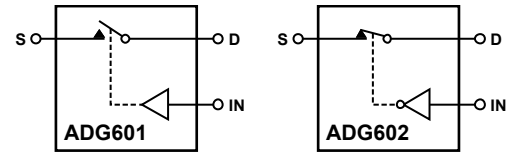
APPLICATIONS

Automatic test equipment
Power routing
Communication systems
Data acquisition systems
Sample-and-hold systems
Avionics
Relay replacement
Battery-powered systems

GENERAL DESCRIPTION

The ADG601/ADG602 are monolithic, CMOS single-pole single-throw (SPST) switches with on resistance typically less than 2.5 Ω . The low on-resistance flatness makes the ADG601/ADG602 ideally suited to many applications, particularly those requiring low distortion. These switches are ideal replacements for mechanical relays because they are more reliable, have lower power requirements, and are available in much smaller package sizes.

The ADG601 is a normally open (NO) switch, and the ADG602 is a normally closed (NC) switch. Each switch conducts equally

FUNCTIONAL BLOCK DIAGRAMS


NOTES
 1. SWITCHES SHOWN FOR A LOGIC 0 INPUT.

Figure 1.

02619-001

Table 1. Truth Table

| ADG601 IN | ADG602 IN | Switch Condition |
|-----------|-----------|------------------|
| 0 | 1 | Off |
| 1 | 0 | On |

well in both directions when the device is on, with the input signal range extending to the supply rails.

The switches are available in tiny, 6-lead SOT-23; 8-lead MSOP; and 820 $\mu\text{m} \times 2255 \mu\text{m}$ die.

PRODUCT HIGHLIGHTS

1. Low on resistance (2 Ω typical)
2. Dual ± 2.7 V to ± 5.5 V or single +2.7 V to +5.5 V supplies
3. Tiny, 6-lead SOT-23; 8-lead MSOP; and 820 $\mu\text{m} \times 2255 \mu\text{m}$ die
4. Rail-to-rail input signal range

Rev. C

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REVISION HISTORY

3/07—Rev. B to Rev. C

| | |
|---------------------------------|-----------|
| Added Die Package..... | Universal |
| Changes to Specifications | 3 |
| Added Figure 4 and Table 6..... | 6 |
| Changes to Ordering Guide | 11 |

3/06—Rev. A to Rev. B

| | |
|---|-----------|
| Updated Format | Universal |
| Changes to 6-Lead SOT-23 (RJ-6) Pin Configuration | 6 |
| Added Pin Function Descriptions Table | 6 |
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| | |
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6/03—Rev. 0 to Rev. A

| | |
|----------------------------------|---|
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| Changes to Ordering Guide | 4 |
| Updated Outline Dimensions | 8 |

SPECIFICATIONS

DUAL SUPPLY

$V_{DD} = 5\text{ V} \pm 10\%$, $V_{SS} = -5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.

Table 2.

| Parameter | B Version ¹ | | Unit | Test Conditions/Comments |
|--|------------------------|----------------------|-------------------|---|
| | +25°C | −40°C to +85°C | | |
| ANALOG SWITCH | | | | |
| Analog Signal Range | | V_{SS} to V_{DD} | V | $V_{DD} = +4.5\text{ V}$, $V_{SS} = -4.5\text{ V}$ |
| On Resistance (R_{ON}) | 2 | | Ω typ | $V_S = \pm 4.5\text{ V}$, $I_{DS} = -10\text{ mA}$; see Figure 15 |
| | 2.5 | 5.5 | Ω max | |
| On-Resistance Flatness ($R_{FLAT(ON)}$) | 0.35 | 0.4 | Ω typ | $V_S = \pm 3.3\text{ V}$, $I_{DS} = -10\text{ mA}$ |
| | 0.6 | 0.65 | Ω max | |
| LEAKAGE CURRENTS | | | | |
| Source Off Leakage, I_S (Off) | ± 0.01 | | nA typ | $V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$ |
| | ± 0.25 | ± 1 | nA max | $V_S = +4.5\text{ V}/-4.5\text{ V}$, $V_D = -4.5\text{ V}/+4.5\text{ V}$; see Figure 16 |
| Drain Off Leakage, I_D (Off) | ± 0.01 | | nA typ | $V_S = +4.5\text{ V}/-4.5\text{ V}$, $V_D = -4.5\text{ V}/+4.5\text{ V}$; see Figure 16 |
| | ± 0.25 | ± 1 | nA max | |
| Channel On Leakage, I_D , I_S (On) | ± 0.01 | | nA typ | $V_S = V_D = +4.5\text{ V}$ or -4.5 V ; see Figure 17 |
| | ± 0.25 | ± 1 | nA max | |
| DIGITAL INPUTS | | | | |
| Input High Voltage, V_{INH} | | 2.4 | V min | |
| Input Low Voltage, V_{INL} | | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | 0.005 | | μA typ | $V_{IN} = V_{INL}$ or V_{INH} |
| | | ± 0.1 | μA max | |
| Digital Input Capacitance, C_{IN} | 2 | | pF typ | |
| DYNAMIC CHARACTERISTICS² | | | | |
| t_{ON} | 80 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 120 | 155 | ns max | $V_S = 3.3\text{ V}$; see Figure 18 |
| t_{OFF} | 45 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 75 | 90 | ns max | $V_S = 3.3\text{ V}$; see Figure 18 |
| Charge Injection | 250 | | pC typ | $V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 19 |
| Off Isolation | −60 | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 20 |
| Bandwidth −3 dB | 180 | | MHz typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 21 |
| C_S (Off) | 50 | | pF typ | $f = 1\text{ MHz}$ |
| C_D (Off) | 50 | | pF typ | $f = 1\text{ MHz}$ |
| C_D , C_S (On) | 145 | | pF typ | $f = 1\text{ MHz}$ |
| POWER REQUIREMENTS | | | | |
| I_{DD} | 0.001 | | μA typ | $V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$ |
| | | 1.0 | μA max | Digital inputs = 0 V or 5.5 V |
| I_{SS} | 0.001 | | μA typ | Digital inputs = 0 V or 5.5 V |
| | | 1.0 | μA max | |

¹ Temperature range for B version is −40°C to +85°C.

² Guaranteed by design, not subject to production test.

ADG601/ADG602

SINGLE SUPPLY

$V_{DD} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 3.

| Parameter | B Version ¹ | | Unit | Test Conditions/Comments |
|--|------------------------|-----------------|-------------------|---|
| | +25°C | −40°C to +85°C | | |
| ANALOG SWITCH | | | | |
| Analogue Signal Range | | 0 V to V_{DD} | V | $V_{DD} = 4.5\text{ V}$ |
| On Resistance (R_{ON}) | 3.5 | | Ω typ | $V_S = 0\text{ V to }4.5\text{ V}$, $I_{DS} = -10\text{ mA}$; see Figure 15 |
| | 5 | 8 | Ω max | |
| On-Resistance Flatness ($R_{FLAT(ON)}$) | 0.2 | 0.2 | Ω typ | $V_S = 1.5\text{ V to }3.3\text{ V}$, $I_{DS} = -10\text{ mA}$ |
| | | 0.6 | Ω max | |
| LEAKAGE CURRENTS | | | | |
| Source Off Leakage, I_S (Off) | ± 0.01 | | nA typ | $V_{DD} = 5.5\text{ V}$ |
| | ± 0.25 | ± 1 | nA max | $V_S = 4.5\text{ V/1 V}$, $V_D = 1\text{ V/4.5 V}$; see Figure 16 |
| Drain Off Leakage, I_D (Off) | ± 0.01 | | nA typ | $V_S = 4.5\text{ V/1 V}$, $V_D = 1\text{ V/4.5 V}$; see Figure 16 |
| | ± 0.25 | ± 1 | nA max | |
| Channel On Leakage, I_D , I_S (On) | ± 0.01 | | nA typ | $V_S = V_D = 4.5\text{ V or }1\text{ V}$; see Figure 17 |
| | ± 0.25 | ± 1 | nA max | |
| DIGITAL INPUTS | | | | |
| Input High Voltage, V_{INH} | | 2.4 | V min | |
| Input Low Voltage, V_{INL} | | 0.8 | V max | |
| Input Current, I_{INL} or I_{INH} | 0.005 | | μA typ | $V_{IN} = V_{INL}$ or V_{INH} |
| | | ± 0.1 | μA max | |
| Digital Input Capacitance, C_{IN} | 2 | | pF typ | |
| DYNAMIC CHARACTERISTICS² | | | | |
| t_{ON} | 110 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 220 | 280 | ns max | $V_S = 3.3\text{ V}$; see Figure 18 |
| t_{OFF} | 50 | | ns typ | $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ |
| | 80 | 110 | ns max | $V_S = 3.3\text{ V}$; see Figure 18 |
| Charge Injection | 20 | | pC typ | $V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 19 |
| Off Isolation | −60 | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 20 |
| Bandwidth −3 dB | 180 | | MHz typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 21 |
| C_S (Off) | 50 | | pF typ | $f = 1\text{ MHz}$ |
| C_D (Off) | 50 | | pF typ | $f = 1\text{ MHz}$ |
| C_D , C_S (On) | 145 | | pF typ | $f = 1\text{ MHz}$ |
| POWER REQUIREMENTS | | | | |
| I_{DD} | 0.001 | | μA typ | $V_{DD} = 5.5\text{ V}$ |
| | | 1.0 | μA max | Digital inputs = 0 V or 5.5 V |

¹ Temperature range for B version is −40°C to +85°C.

² Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 4.

| Parameter | Rating |
|--|---|
| V_{DD} to V_{SS} | 13 V |
| V_{DD} to GND | -0.3 V to +6.5 V |
| V_{SS} to GND | +0.3 V to -6.5 V |
| Analog Inputs ¹ | $V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ |
| Digital Inputs ¹ | -0.3 V to $V_{DD} + 0.3\text{ V}$ or 30 mA (whichever occurs first) |
| Continuous Current, S or D | 100 mA |
| Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Max) | 200 mA |
| Operating Temperature Range Industrial (B Version) | -40°C to +85°C |
| Storage Temperature Range | -65°C to +150°C |
| Junction Temperature | 150°C |
| Thermal Resistance | |
| MSOP | |
| θ_{JA} | 206°C/W |
| θ_{JC} | 44°C/W |
| SOT-23 | |
| θ_{JA} | 229.6°C/W |
| θ_{JC} | 91.99°C/W |
| Lead Temperature, Soldering (10 sec) | 300°C |
| IR Reflow, Peak Temperature | 220°C |

¹ Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at a time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ADG601/ADG602

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

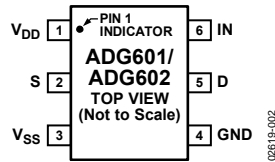


Figure 2. 6-Lead SOT-23 (RJ-6)

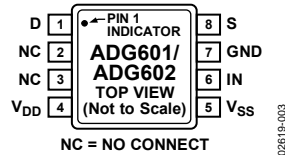


Figure 3. 8-Lead MSOP (RM-8)

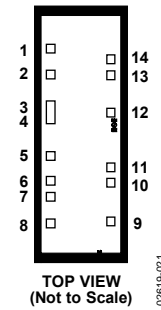


Figure 4. Die (820 μm × 2255 μm)

Table 5. Pin Function Descriptions

| Pin No. | | Mnemonic | Description |
|---------------|-------------|-----------------|---|
| 6-Lead SOT-23 | 8-Lead MSOP | | |
| 1 | 4 | V _{DD} | Most Positive Power Supply Potential. |
| 2 | 8 | S | Source Terminal. Can be an input or output. |
| 3 | 5 | V _{SS} | Most Negative Power Supply Potential. |
| 4 | 7 | GND | Ground (0 V) Reference. |
| 5 | 1 | D | Drain Terminal. Can be an input or output. |
| 6 | 6 | IN | Logic Control Input. |
| N/A | 2, 3 | NC | No Connect. |

Table 6. Die Pad Coordinates¹

| Die Pad No. | Die Pad Coordinates | | Mnemonic | Description |
|-------------|---------------------|--------|-----------------|--|
| | X (μm) | Y (μm) | | |
| 1 | -265 | +754 | NC | No Connect. |
| 2 | -265 | +525 | D | Drain Terminal. Can be an input or output. ² |
| 3 | -265 | +241 | D | Drain Terminal. Can be an input or output. ² |
| 4 | -265 | +141 | D | Drain Terminal. Can be an input or output. ² |
| 5 | -265 | -191 | NC | No Connect. |
| 6 | -265 | -409 | NC | No Connect. |
| 7 | -265 | -549 | NC | No Connect. |
| 8 | -265 | -787 | V _{DD} | Most Positive Power Supply Potential. |
| 9 | +265 | -767 | V _{SS} | Most Negative Power Supply Potential. |
| 10 | +265 | -429 | IN | Logic Control Input. |
| 11 | +265 | -289 | GND | Ground (0 V) Reference. |
| 12 | +265 | +189 | S | Source Terminal. Can be an input or output. ³ |
| 13 | +265 | +521 | S | Source Terminal. Can be an input or output. ³ |
| 14 | +265 | +661 | NC | Source Terminal. Can be an input or output. |

¹ Measured from the center of the die.

² Bond the D pads together to a single point to preserve the on resistance and current handling capability. The common point acts as the drain pin of the switch.

³ Bond the S pads together to a single point to preserve the on resistance and current handling capability. The common point acts as the source pin of the switch.

TYPICAL PERFORMANCE CHARACTERISTICS

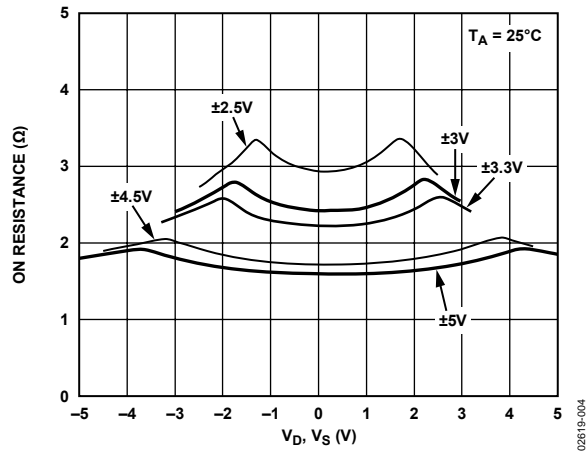


Figure 5. On Resistance vs. V_D , V_S (Dual Supply)

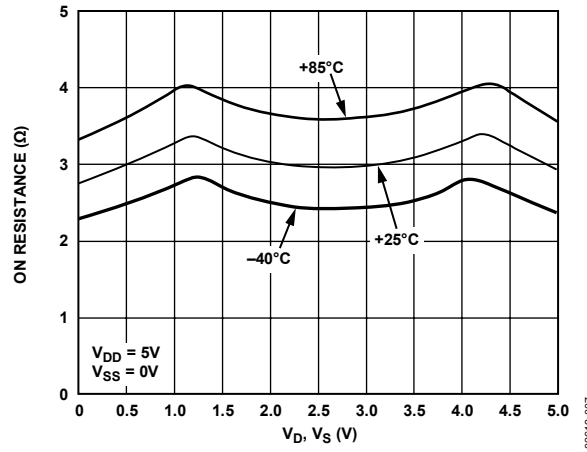


Figure 8. On Resistance vs. V_D , V_S for Different Temperatures (Single Supply)

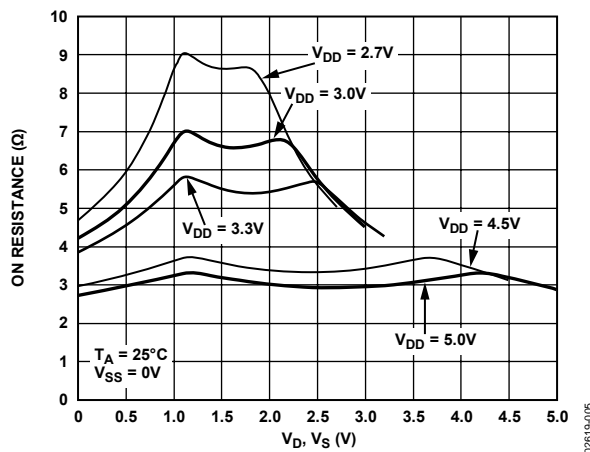


Figure 6. On Resistance vs. V_D , V_S (Single Supply)

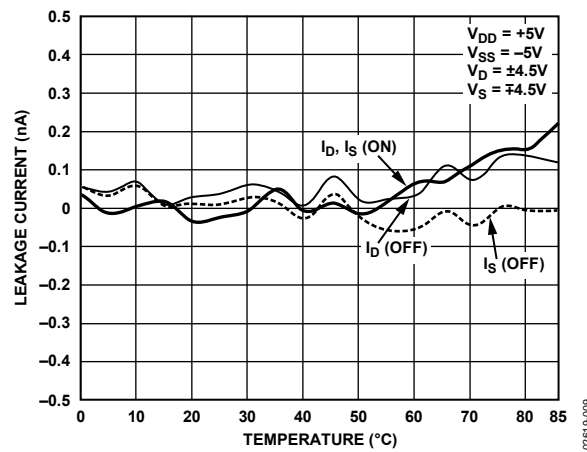


Figure 9. Leakage Currents vs. Temperature (Dual Supply)

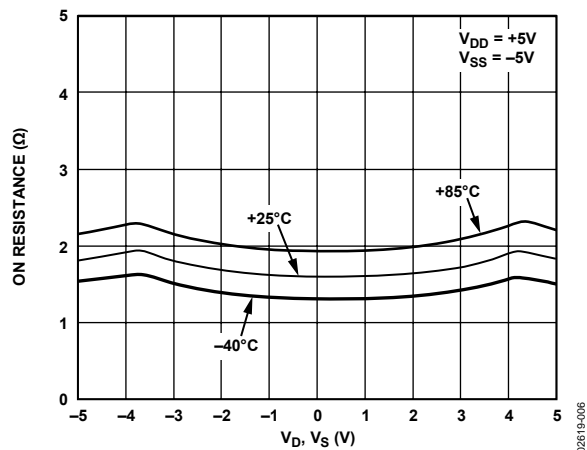


Figure 7. On Resistance vs. V_D , V_S for Different Temperatures (Dual Supply)

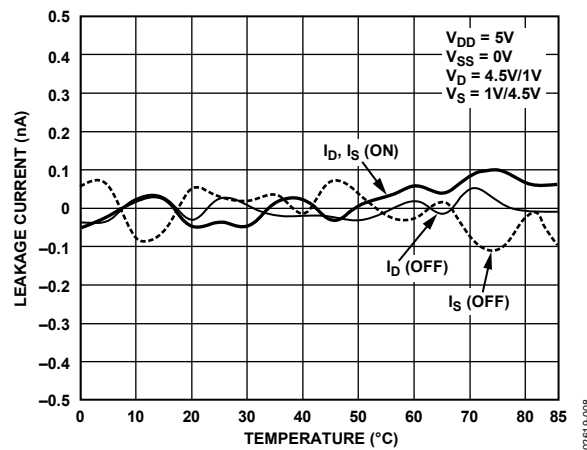


Figure 10. Leakage Currents vs. Temperature (Single Supply)

ADG601/ADG602

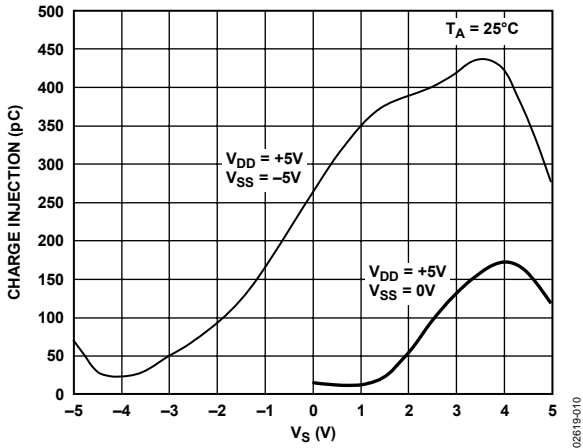


Figure 11. Charge Injection vs. Source Voltage

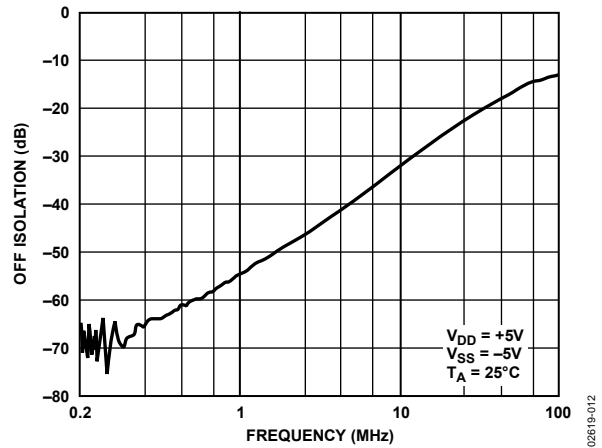


Figure 13. Off Isolation vs. Frequency

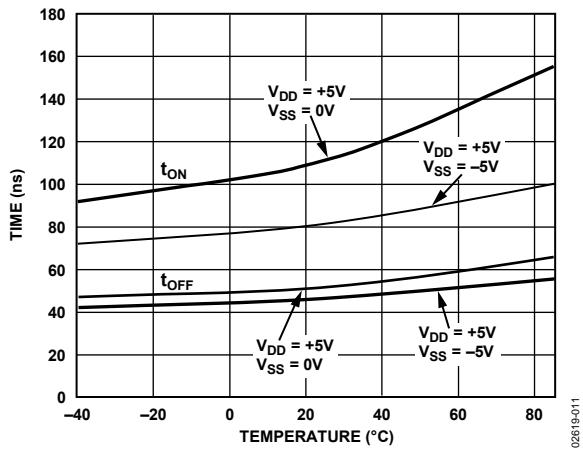


Figure 12. t_{ON}/t_{OFF} Times vs. Temperature

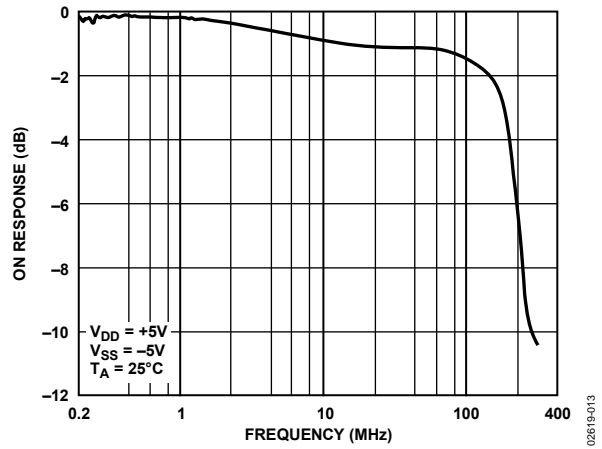


Figure 14. On Response vs. Frequency

TERMINOLOGY

V_{DD}

Most positive power supply potential.

V_{SS}

Most negative power supply potential.

I_{DD}

Positive supply current.

I_{SS}

Negative supply current.

GND

Ground (0 V) reference.

S

Source terminal. Can be an input or an output.

D

Drain terminal. Can be an input or an output.

IN

Logic control input.

V_D, V_S

Analog voltage on Terminal D and Terminal S.

R_{ON}

Ohmic resistance between Terminal D and Terminal S.

$R_{FLAT (ON)}$

Flatness is defined as the difference between the maximum and minimum values of on resistance as measured over the specified analog signal range.

$I_S (Off)$

Source leakage current with the switch off.

$I_D (Off)$

Drain leakage current with the switch off.

$I_D, I_S (On)$

Channel leakage current with the switch on.

V_{INL}

Maximum input voltage for Logic 0.

V_{INH}

Minimum input voltage for Logic 1.

$I_{INL} (I_{INH})$

Input current of the digital input.

$C_S (Off)$

Off switch source capacitance. Measured with reference to ground.

$C_D (Off)$

Off switch drain capacitance. Measured with reference to ground.

$C_D, C_S (On)$

On switch capacitance. Measured with reference to ground.

C_{IN}

Digital input capacitance.

t_{ON}

Delay between applying the digital control input and the output switching on.

t_{OFF}

Delay between applying the digital control input and the output switching off.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Off Isolation

A measure of unwanted signal coupling through an off switch.

On Response

Frequency response of the on switch.

Insertion Loss

Loss due to the on resistance of the switch.

TEST CIRCUITS

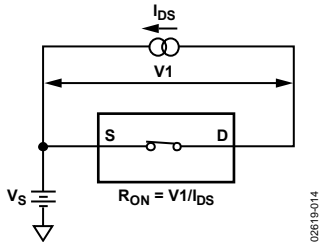


Figure 15. On Resistance

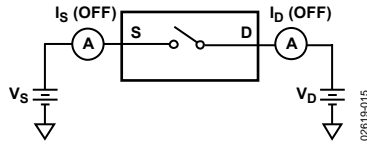


Figure 16. Off Leakage

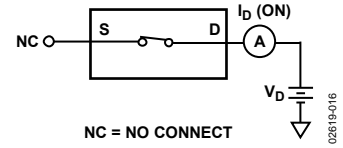


Figure 17. On Leakage

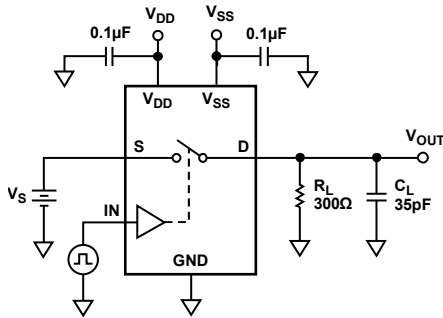


Figure 18. Switching Times

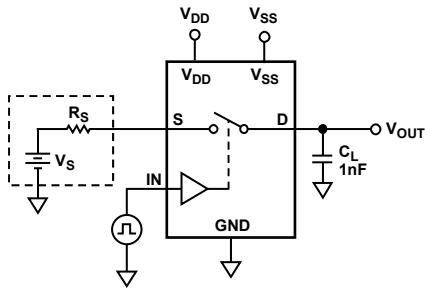
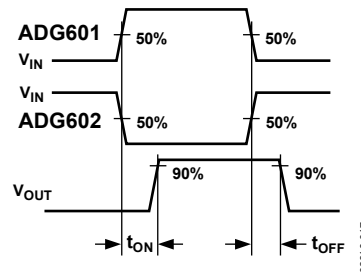
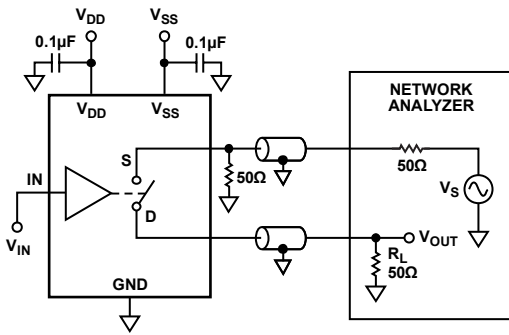
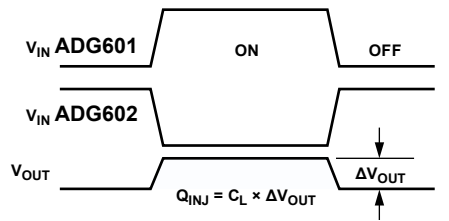
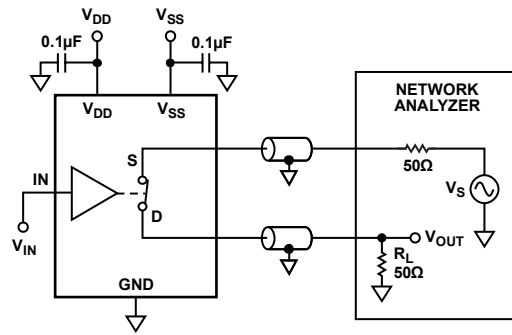


Figure 19. Charge Injection



$$\text{OFF ISOLATION} = 20 \log \frac{V_{OUT}}{V_S}$$

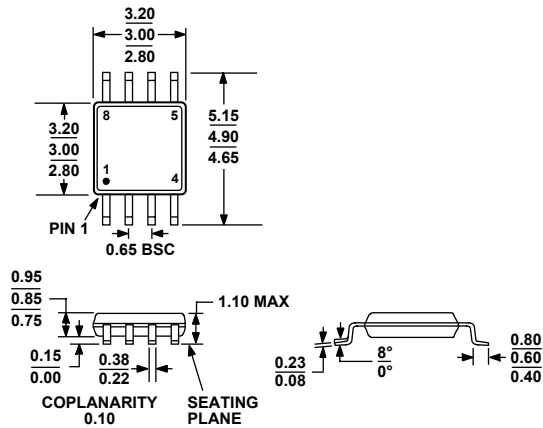
Figure 20. Off Isolation



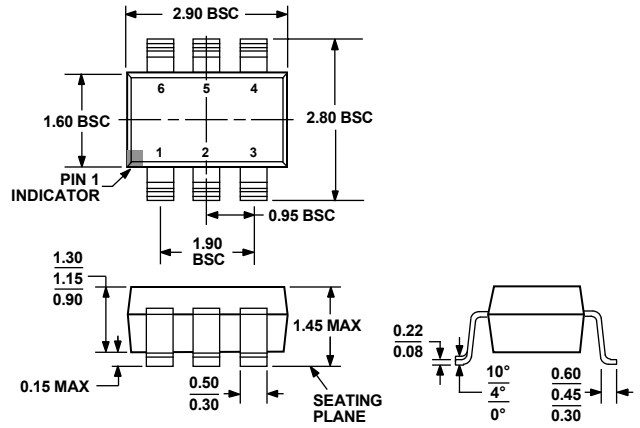
$$\text{INSERTION LOSS} = 20 \log \frac{V_{OUT \text{ WITH SWITCH}}}{V_S \text{ WITHOUT SWITCH}}$$

Figure 21. Bandwidth

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA
 Figure 22. 8-Lead Mini Small Outline Package [MSOP] (RM-8)
 Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-178-AB
 Figure 23. 6-Lead Small Outline Transistor Package [SOT-23] (RJ-6)
 Dimensions shown in millimeters

ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option | Branding ¹ |
|-------------------------------|-------------------|---------------------|----------------|-----------------------|
| ADG601BRT-REEL | -40°C to +85°C | 6-Lead SOT-23 | RJ-6 | STB |
| ADG601BRT-REEL7 | -40°C to +85°C | 6-Lead SOT-23 | RJ-6 | STB |
| ADG601BRTZ-REEL ² | -40°C to +85°C | 6-Lead SOT-23 | RJ-6 | STB# |
| ADG601BRTZ-REEL7 ² | -40°C to +85°C | 6-Lead SOT-23 | RJ-6 | STB# |
| ADG601BRM | -40°C to +85°C | 8-Lead MSOP | RM-8 | STB |
| ADG601BRM-REEL | -40°C to +85°C | 8-Lead MSOP | RM-8 | STB |
| ADG601BRM-REEL7 | -40°C to +85°C | 8-Lead MSOP | RM-8 | STB |
| ADG601BRMZ ² | -40°C to +85°C | 8-Lead MSOP | RM-8 | S1G |
| ADG601BRMZ-REEL ² | -40°C to +85°C | 8-Lead MSOP | RM-8 | S1G |
| ADG601BRMZ-REEL7 ² | -40°C to +85°C | 8-Lead MSOP | RM-8 | S1G |
| ADG601CSURF | | Die | | |
| ADG602BRT-REEL | -40°C to +85°C | 6-Lead SOT-23 | RJ-6 | SUB |
| ADG602BRT-REEL7 | -40°C to +85°C | 6-Lead SOT-23 | RJ-6 | SUB |
| ADG602BRTZ-REEL ² | -40°C to +85°C | 6-Lead SOT-23 | RJ-6 | S18 |
| ADG602BRTZ-REEL7 ² | -40°C to +85°C | 6-Lead SOT-23 | RJ-6 | S18 |
| ADG602BRM | -40°C to +85°C | 8-Lead MSOP | RM-8 | SUB |
| ADG602BRM-REEL | -40°C to +85°C | 8-Lead MSOP | RM-8 | SUB |
| ADG602BRM-REEL7 | -40°C to +85°C | 8-Lead MSOP | RM-8 | SUB |
| ADG602BRMZ ² | -40°C to +85°C | 8-Lead MSOP | RM-8 | S18 |
| ADG602BRMZ-REEL7 ² | -40°C to +85°C | 8-Lead MSOP | RM-8 | S18 |

¹ Branding on SOT-23 and MSOP is limited to three characters due to space constraints.
² Z = RoHS Compliant Part, # denotes RoHS compliant product, may be top or bottom marked.

NOTES