

# DATA SHEET

**BT148W series**  
Thyristors  
logic level

Product specification

October 1997



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logic level**

**BT148W series**

**GENERAL DESCRIPTION**

Glass passivated, sensitive gate thyristors in a plastic envelope suitable for surface mounting, intended for use in general purpose switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

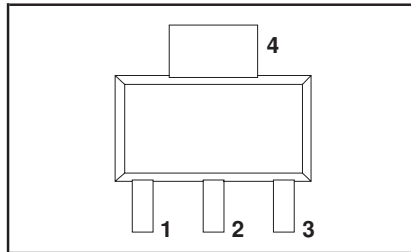
**QUICK REFERENCE DATA**

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
$V_{DRM}$ , $V_{RRM}$	Repetitive peak off-state voltages	<b>400R</b> 400	<b>500R</b> 500	<b>600R</b> 600	V
$I_{T(AV)}$	Average on-state current	0.6	0.6	0.6	A
$I_{T(RMS)}$	RMS on-state current	1	1	1	A
$I_{TSM}$	Non-repetitive peak on-state current	10	10	10	A

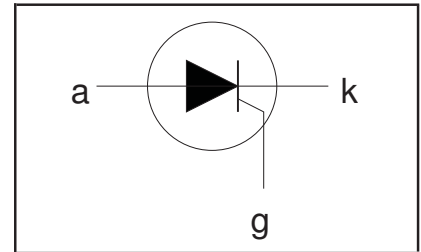
**PINNING - SOT223**

PIN	DESCRIPTION
1	cathode
2	anode
3	gate
tab	anode

**PIN CONFIGURATION**



**SYMBOL**



**LIMITING VALUES**

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
$V_{DRM}$ , $V_{RRM}$	Repetitive peak off-state voltages		-	<b>-400R</b> 400 <sup>1</sup>	<b>-500R</b> 500 <sup>1</sup>	<b>-600R</b> 600 <sup>1</sup>	V
$I_{T(AV)}$	Average on-state current	half sine wave; $T_{sp} \leq 112\text{ °C}$	-	0.6			A
$I_{T(RMS)}$	RMS on-state current	all conduction angles	-	1			A
$I_{TSM}$	Non-repetitive peak on-state current	half sine wave; $T_j = 25\text{ °C}$ prior to surge	-	10			A
		$t = 10\text{ ms}$	-	11			A
		$t = 8.3\text{ ms}$	-	0.5			A <sup>2</sup> s
$I^2t$	$I^2t$ for fusing	$t = 10\text{ ms}$	-	50			A/μs
$dl_T/dt$	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 4\text{ A}$ ; $I_G = 200\text{ mA}$ ; $dl_G/dt = 200\text{ mA}/\mu\text{s}$	-	50			A/μs
$I_{GM}$	Peak gate current		-	1			A
$V_{GM}$	Peak gate voltage		-	5			V
$V_{RGM}$	Peak reverse gate voltage		-	5			V
$P_{GM}$	Peak gate power		-	1.2			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.12			W
$T_{stg}$	Storage temperature		-40	150			°C
$T_j$	Operating junction temperature		-	125 <sup>2</sup>			°C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/μs.

2 Note: Operation above 110°C may require the use of a gate to cathode resistor of 1kΩ or less.

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**THERMAL RESISTANCES**

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-sp}$	Thermal resistance junction to solder point		-	-	15	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	pcb mounted, minimum footprint pcb mounted, pad area as in fig:14	-	156 70	-	K/W K/W

**STATIC CHARACTERISTICS**

$T_j = 25\text{ °C}$  unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{GT}$	Gate trigger current	$V_D = 12\text{ V}; I_T = 0.1\text{ A}$	-	50	200	$\mu\text{A}$
$I_L$	Latching current	$V_D = 12\text{ V}; I_{GT} = 0.1\text{ A}$	-	0.17	10	mA
$I_H$	Holding current	$V_D = 12\text{ V}; I_{GT} = 0.1\text{ A}$	-	0.10	6	mA
$V_T$	On-state voltage	$I_T = 2\text{ A}$	-	1.3	1.5	V
$V_{GT}$	Gate trigger voltage	$V_D = 12\text{ V}; I_T = 0.1\text{ A}$	-	0.4	1.5	V
$I_D, I_R$	Off-state leakage current	$V_R = V_{RRM(max)}; I_T = 0.1\text{ A}; T_j = 110\text{ °C}$ $V_D = V_{DRM(max)}; V_R = V_{RRM(max)}; T_j = 125\text{ °C}$	0.1	0.2	-	V
			-	0.1	0.5	mA

**DYNAMIC CHARACTERISTICS**

$T_j = 25\text{ °C}$  unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$dV_D/dt$	Critical rate of rise of off-state voltage	$V_{DM} = 67\% V_{DRM(max)}; T_j = 125\text{ °C};$ exponential waveform; $R_{GK} = 100\ \Omega$	-	50	-	V/ $\mu\text{s}$
$t_{gt}$	Gate controlled turn-on time	$I_{TM} = 4\text{ A}; V_D = V_{DRM(max)}; I_G = 5\text{ mA};$ $dI_G/dt = 0.2\text{ A}/\mu\text{s}$	-	2	-	$\mu\text{s}$
$t_q$	Circuit commutated turn-off time	$V_D = 67\% V_{DRM(max)}; T_j = 125\text{ °C}; I_{TM} = 2\text{ A};$ $V_R = 35\text{ V}; dI_{TM}/dt = 30\text{ A}/\mu\text{s};$ $dV_D/dt = 2\text{ V}/\mu\text{s}; R_{GK} = 1\text{ k}\Omega$	-	100	-	$\mu\text{s}$

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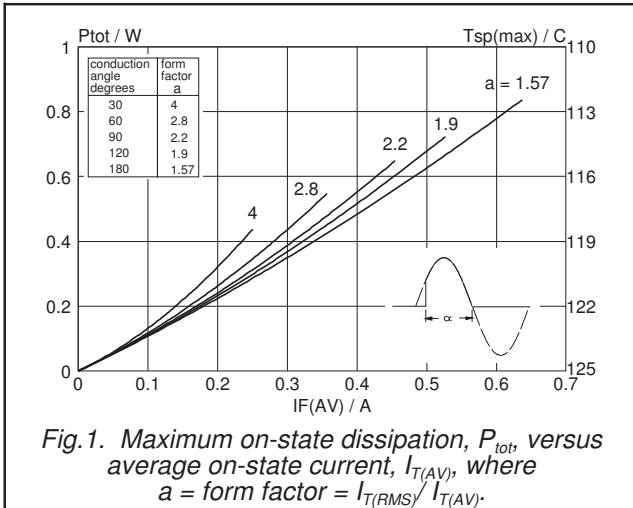


Fig. 1. Maximum on-state dissipation,  $P_{tot}$ , versus average on-state current,  $I_{T(AV)}$ , where  $a = \text{form factor} = I_{T(RMS)} / I_{T(AV)}$ .

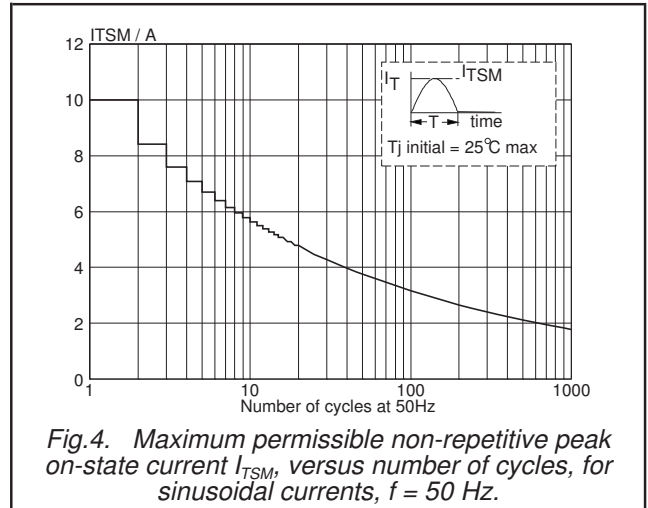


Fig. 4. Maximum permissible non-repetitive peak on-state current  $I_{TSM}$ , versus number of cycles, for sinusoidal currents,  $f = 50 \text{ Hz}$ .

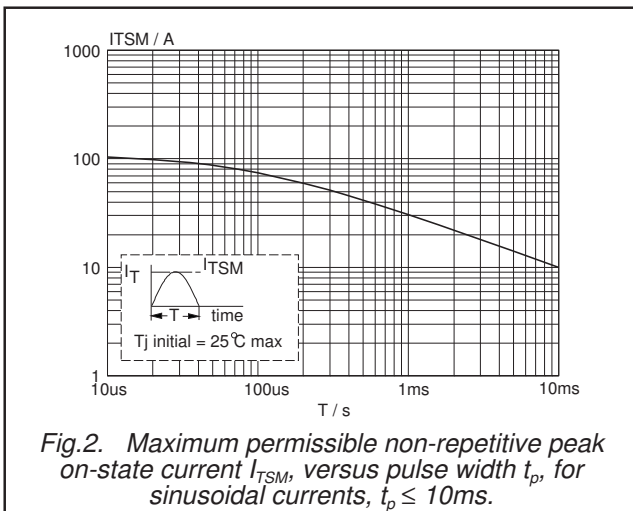


Fig. 2. Maximum permissible non-repetitive peak on-state current  $I_{TSM}$ , versus pulse width  $t_p$ , for sinusoidal currents,  $t_p \leq 10 \text{ ms}$ .

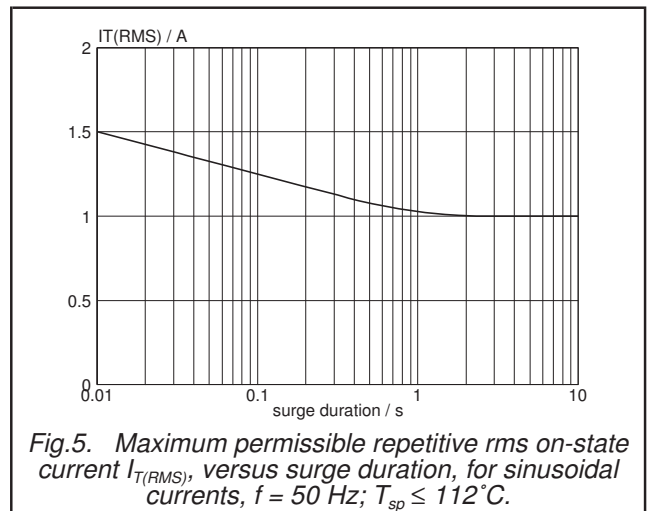


Fig. 5. Maximum permissible repetitive rms on-state current  $I_{T(RMS)}$ , versus surge duration, for sinusoidal currents,  $f = 50 \text{ Hz}$ ;  $T_{sp} \leq 112^\circ\text{C}$ .

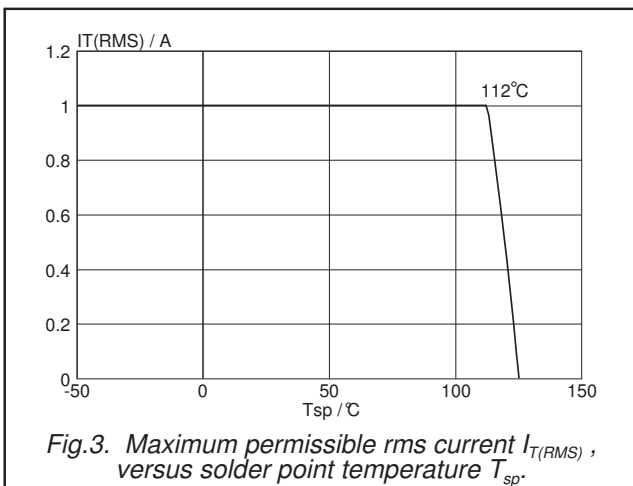


Fig. 3. Maximum permissible rms current  $I_{T(RMS)}$ , versus solder point temperature  $T_{sp}$ .

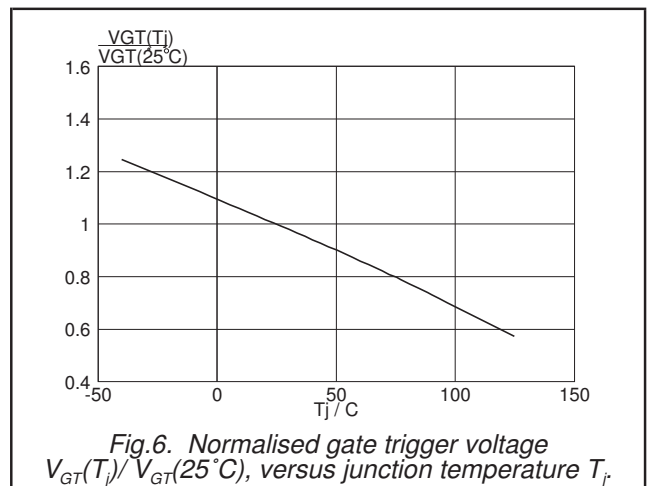
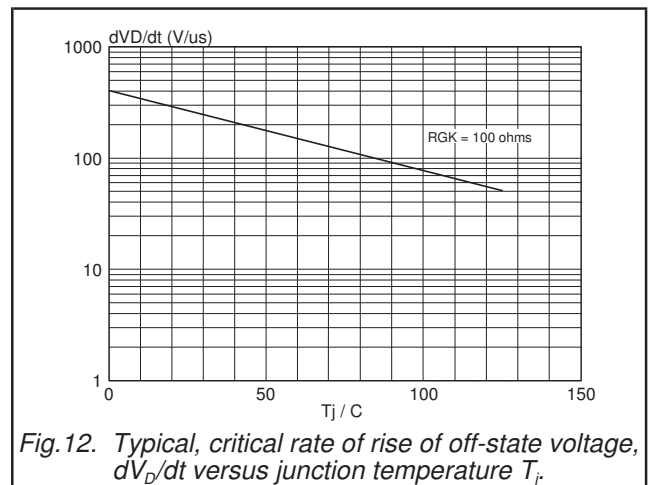
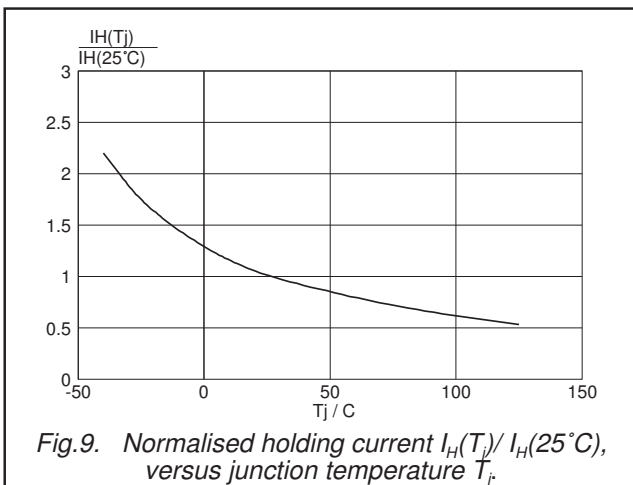
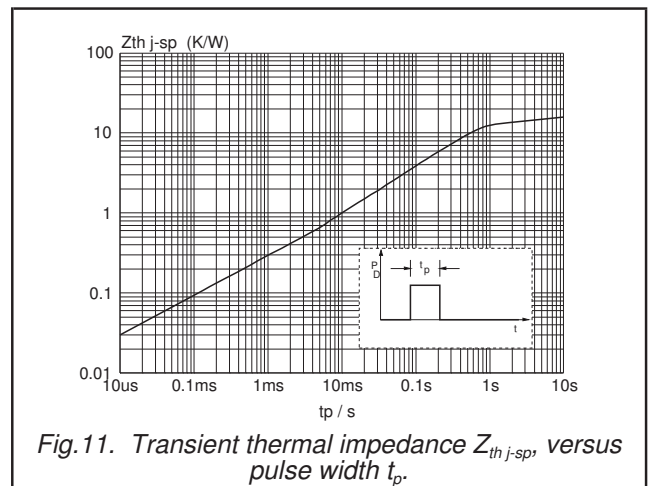
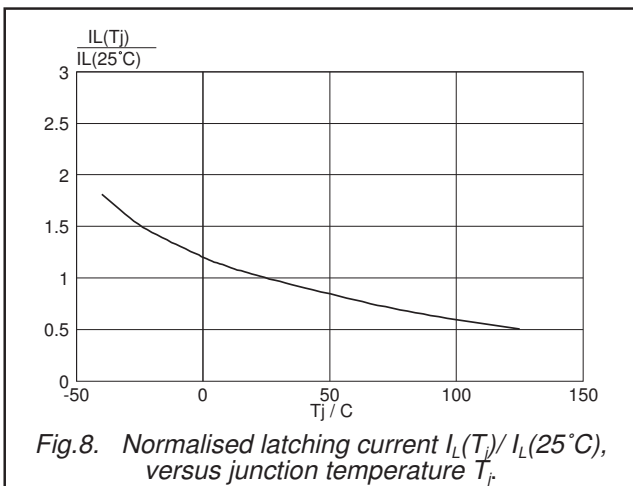
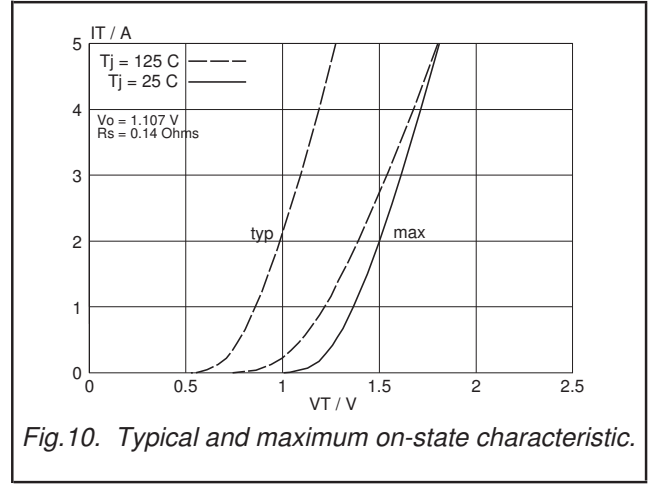
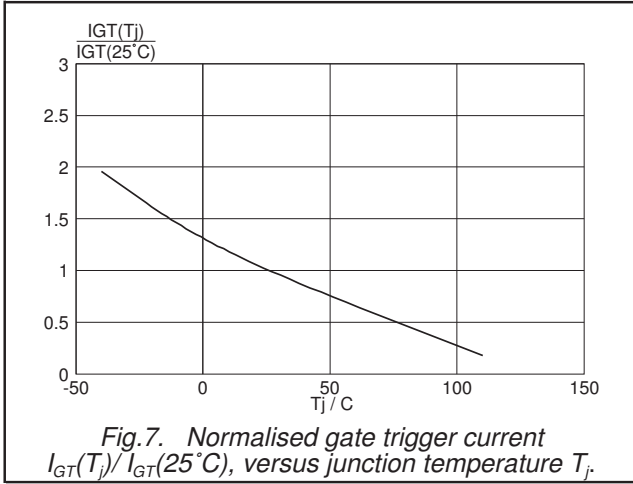


Fig. 6. Normalised gate trigger voltage  $V_{GT}(T_j) / V_{GT}(25^\circ\text{C})$ , versus junction temperature  $T_j$ .

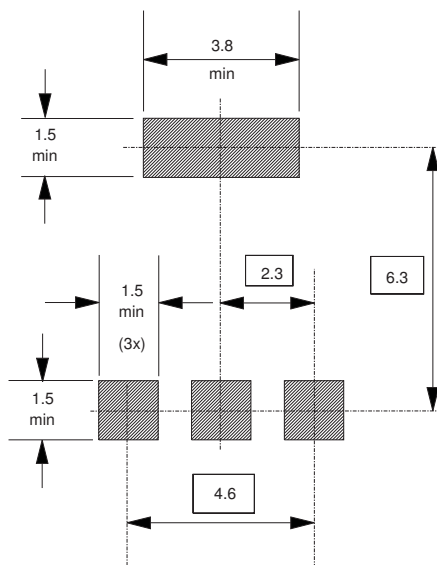
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**MOUNTING INSTRUCTIONS**

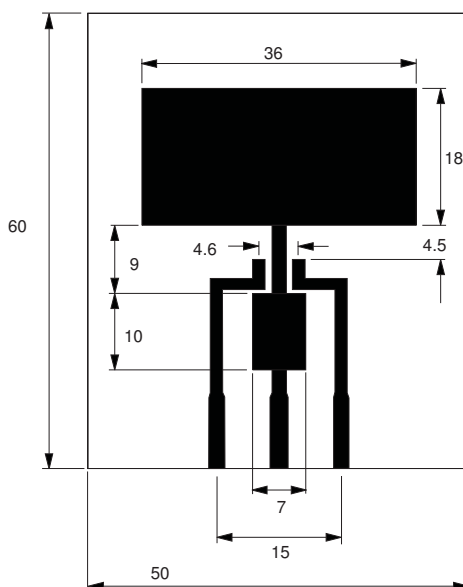
*Dimensions in mm.*



*Fig.13. soldering pattern for surface mounting SOT223.*

**PRINTED CIRCUIT BOARD**

*Dimensions in mm.*



*Fig.14. PCB for thermal resistance and power rating for SOT223.  
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).*



## Legal information

### DATA SHEET STATUS

DOCUMENT STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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