Application Note: SY9702

High Efficiency, 1MHz, 2A Buck-Boost DC/DC Regulator

General Description

SY9702 is a wide input voltage range, high efficiency, fixed frequency buck-boost converter that operates from input voltage above, below or equal to the output voltage. It provides a power supply for system powered by either a two-cell or three-cell alkaline, Ni-Cd or Ni-MH battery, or a one-cell Li-Ion or Li-polymer battery.

SY9702 can support for 2A load current capability. It is based on a fixed frequency, pulse-width-modulation (PWM) controller using synchronous rectification to obtain maximum efficiency. The output voltage and compensation circuit can be programmed using external resistors and capacitors network. During shutdown, the load is disconnected from the battery. The device is packaged in tight QFN2x3-13.

Ordering Information

SY9702□(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY9702QOC	QFN2x3-13	----

Features

- Fixed frequency operation with battery voltage above, below or equal to the output.
- Four internal power switches to form true 4-switches buck-boost with single inductor.
- Seamless buck-boost transition.
- 2.6V to 5.5V Input Voltage Range.
- 2A continuous output current capability.
- Output disconnect at shutdown.
- Power good indicator.
- Compact package: QFN2x3-13
- Built in thermal shut down protection, hard short protection.

Applications

- Palmtop Computers
- Handheld Instruments
- MP3/MP4 Players
- Digital Cameras/Camcorders
- Personal Medical Products
- High Power LED's
- All two-cell and three-cell alkaline, Ni-Cd or Ni-MH or signal-cell Li battery powered products

Typical Applications

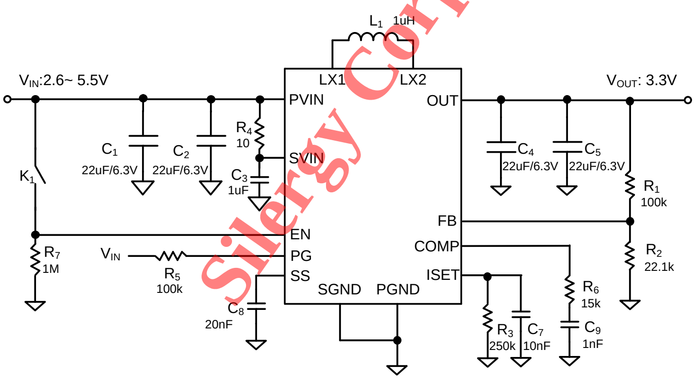


Figure 1. Schematic diagram

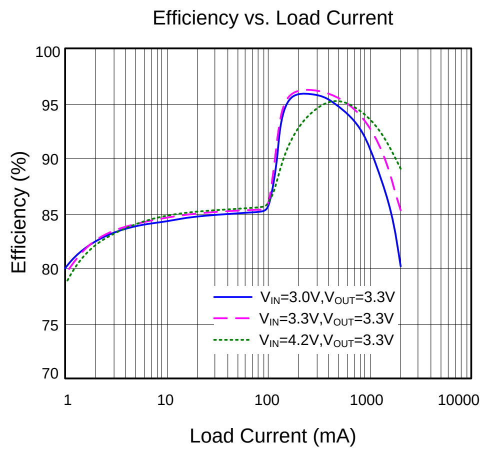
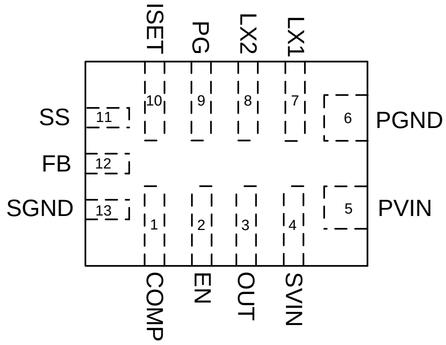


Figure 2. Efficiency Figure

Pinout (top view)



Top Mark: ZN*xyz* (device code: ZN, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Description
COMP	1	External compensation for voltage loop.
EN	2	Enable control. Pull high to turn on. Internal integrated with 1MΩ pull down Resistor.
OUT	3	Output of the synchronous rectifier. Decouple this pin to GND with at least 22uF ceramic cap. Minimize the loop area formed by output cap, OUT pin and GND paddles.
SVIN	4	Signal power input pin. Decouple this pin to GND with at least 1uF ceramic cap.
PVIN	5	Power input pin. Decouple this pin to GND with at least 22uF ceramic cap. Minimize the loop area formed by input cap, PVIN pin and GND paddles.
PGND	6	Power ground pin.
LX1	7	Inductor connection 1.Connect this node to the switching node of the inductor.
LX2	8	Inductor connection 2. Connect this node to the switching node of the inductor.
PG	9	Power good indicator.
ISET	10	Apply a resistor and capacitor parallel network to sense the output average current. If V_{ISET} is lower than 0.2V, IC will go into PFM mode. Do not let it floating. Tie to ground for forced PWM operation.
SS	11	Connect this pin to a soft-start capacitor to program soft-start time.
FB	12	Output feedback pin. Connect this pin to the center point of the output resistor divider to program the output voltage.
SGND	13	Signal ground pin.

Absolute Maximum Ratings (Note 1)

OUT -- 4 V
All Other Pins-- 6V
Power Dissipation, P_D @ T_A = 25 ℃ --- 3W
Package Thermal Resistance (Note 2)
θ_{JA} -- 40 ℃/W
θ_{JC} -- 18 ℃/W
Junction Temperature Range --- 150 ℃

Lead Temperature (Soldering, 10 sec.) --- 260 ℃
Storage Temperature Range --- -65 ℃ to 150 ℃

Recommended Operating Conditions (Note 3)

Supply Input Voltage --- 2.6V to 5.5V
Output Voltage --- 2.6V to 3.8V
Junction Temperature Range --- -40 ℃ to 125 ℃
Ambient Temperature Range --- -40 ℃ to 85 ℃

Electrical Characteristics

(V_{IN} = 4.2V, V_{OUT} = 3.3V, L =1μH, C_{OUT} = 22uFx2, T_A = 25 ℃, I_{OUT} = 1A unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.6		5.5	V
Output Voltage Range	V_{OUT}		2.6		3.8	V
Quiescent Current	I_Q	I_{OUT}=0, EN=1, ISET=250kΩ, FB=105%*V_{REF}		60	100	μA
Shutdown Current	I_{SHDN}	EN=0		0.1	1	μA
Feedback Reference Voltage	V_{REF}		0.591	0.6	0.609	V
NFET $R_{DS(ON)}$	$R_{DS(ON)1}$			50		mΩ
PFET $R_{DS(ON)}$	$R_{DS(ON)2}$			50		mΩ
Input Peak Current Limit	I_{LIM}		4.5	5		A
Output Negative Current Limit	I_{NEG}			-1		A
Soft-start current	I_{SS}	Soft-start time: $t_{ss}=\frac{0.7V}{I_{ss}}\times C_{ss}$		5		μA
EN rising threshold	V_{ENH}		1.5			V
EN falling threshold	V_{ENL}				0.4	V
Input UVLO rising threshold	V_{UVLO}			2.45	2.55	V
UVLO hysteresis	V_{HYS}			0.2		V
PG rising threshold	$V_{FB,HV}$			0.48		V
PG under-voltage threshold	$V_{FB,LV}$			0.48		V
PG over voltage threshold	$V_{FB,OV}$			0.72		V
Output current sense	I_{SET}	I_{OUT}=1A		5		μA
Output Voltage Over Protection	V_{OVP}			125		%
OVP protection delay time	T_{OVP_delay}			16		μs
ISET pin threshold for PFM mode	V_{PFM}			0.2		V
Oscillator Frequency	F_{OSC}	I_{OUT}=1.0A	0.8	1.0	1.2	MHz
Min Duty Cycle		Boost & Buck		10		%
Max Duty Cycle		Boost & Buck		90		%
Thermal Shutdown Temperature	T_{SD}			150		℃
Thermal Shutdown Hysteresis	T_{HYS}			15		℃

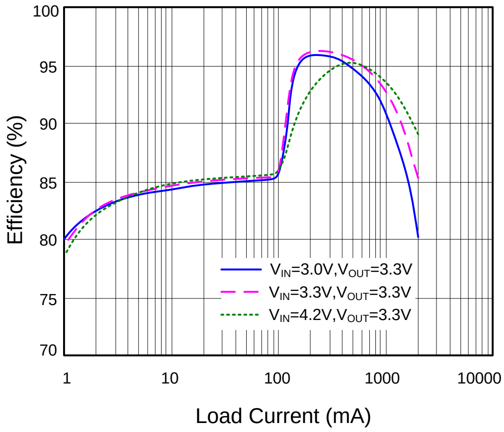
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25 ℃ on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Paddle of QFN2x3-13 package is the case position for θ_{JC} measurement.

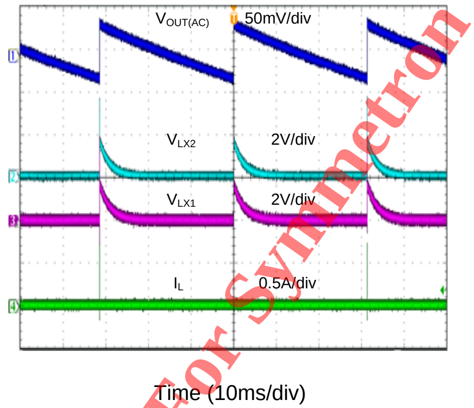
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

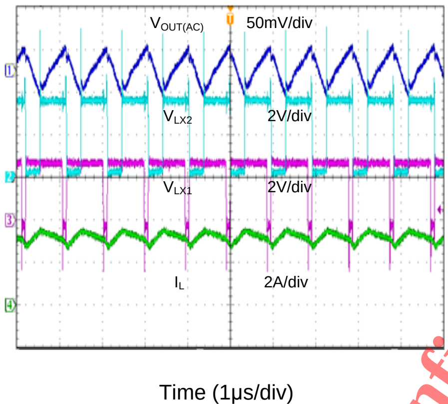
Efficiency vs. Load Current



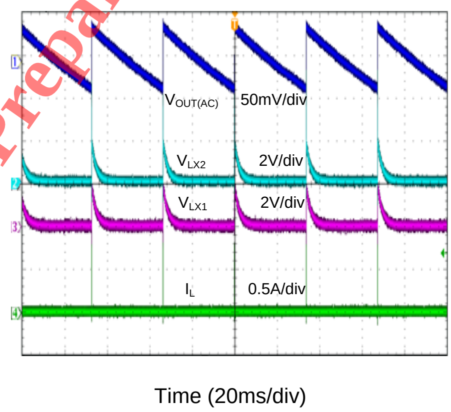
Output Ripple
(V_{IN}=3.0V, V_{OUT}=3.3V, I_{OUT}=0A)



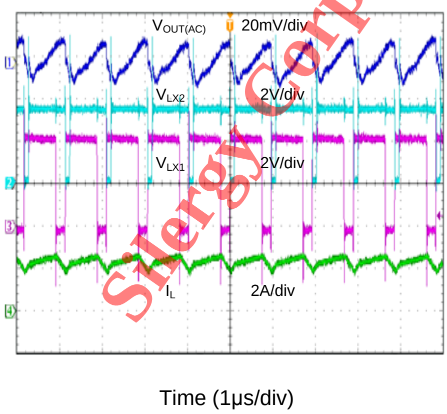
Output Ripple
(V_{IN}=3.0V, V_{OUT}=3.3V, I_{OUT}=2A)



Output Ripple
(V_{IN}=4.2V, V_{OUT}=3.3V, I_{OUT}=0A)

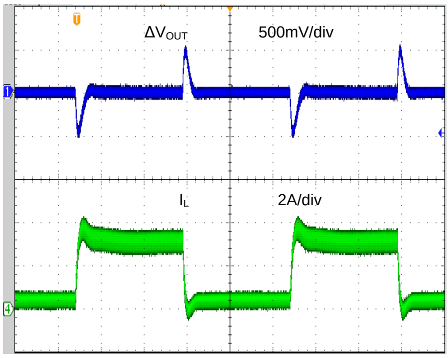


Output Ripple
(V_{IN}=4.2V, V_{OUT}=3.3V, I_{OUT}=2A)



Load Transient

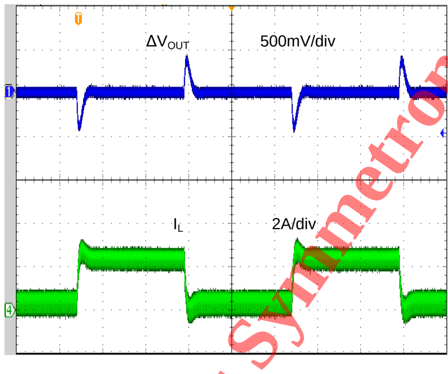
(V_{IN}=3.0V, V_{OUT}=3.3V, I_{OUT}=0.2~2A)



Time (200μs/div)

Load Transient

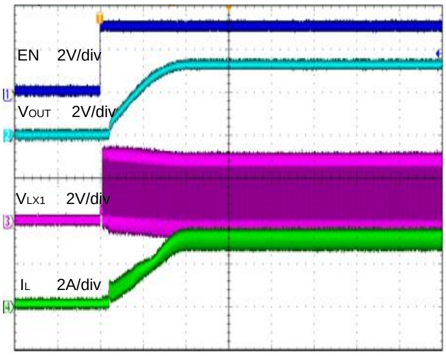
(V_{IN}=4.2V, V_{OUT}=3.3V, I_{OUT}=0.2~2A)



Time (200μs/div)

Startup From Enable

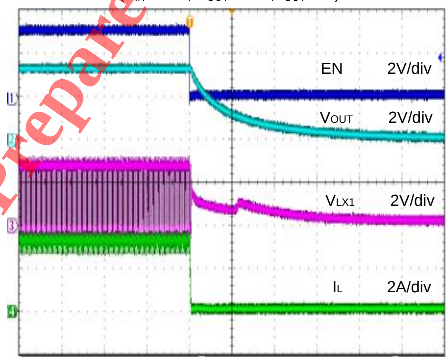
(V_{IN}=3.0V, V_{OUT}=3.3V, I_{OUT}=2A)



Time (800μs/div)

Shutdown From Enable

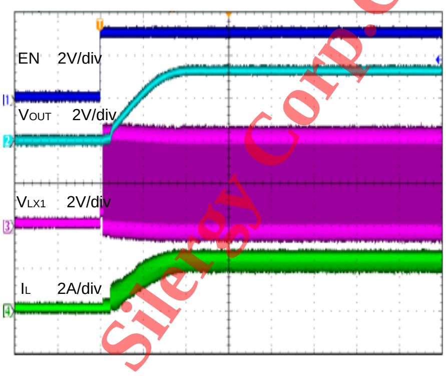
(V_{IN}=3.0V, V_{OUT}=3.3V, I_{OUT}=2A)



Time (40μs/div)

Startup From Enable

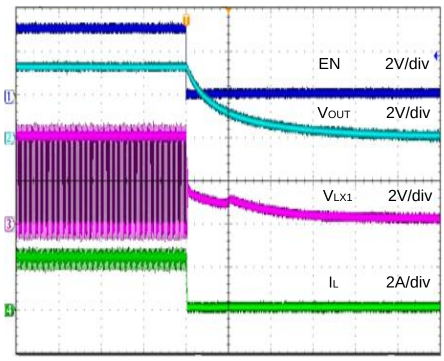
(V_{IN}=4.2V, V_{OUT}=3.3V, I_{OUT}=2A)



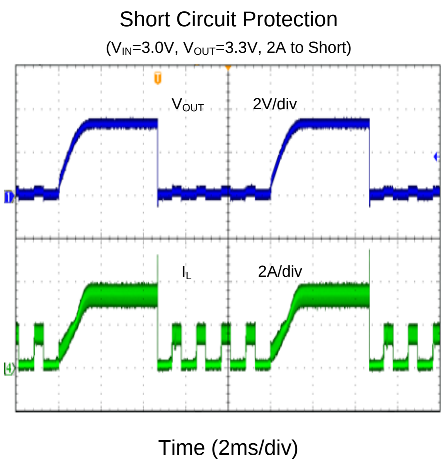
Time (800μs/div)

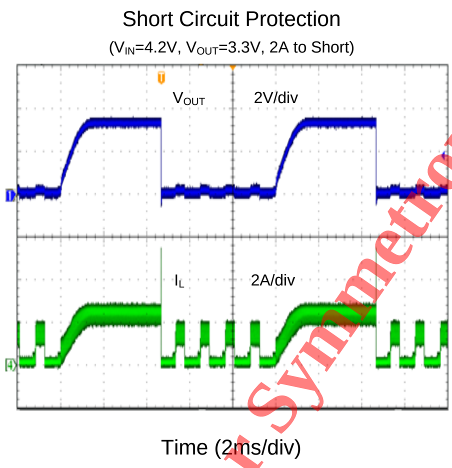
Shutdown From Enable

(V_{IN}=4.2V, V_{OUT}=3.3V, I_{OUT}=2A)



Time (40μs/div)


Short Circuit Protection
(VIN=3.0V, VOUT=3.3V, 2A to Short)
VOUT
2V/div
IL
2A/div
Time (2ms/div)


Short Circuit Protection
(VIN=4.2V, VOUT=3.3V, 2A to Short)
VOUT
2V/div
IL
2A/div
Time (2ms/div)

Operation

SY9702 is a wide input voltage range, high efficiency, fixed frequency buck-boost converter that operates from input voltage above, below or equal to the output voltage. It provides a power supply for system powered by either a two-cell or three-cell alkaline, Ni-Cd or Ni-MH battery, or a one-cell Li-Ion or Li-polymer battery.

SY9702 can support for 2A load current capability. It is based on a fixed frequency, pulse-width-modulation (PWM) controller using synchronous rectification to obtain maximum efficiency. The output voltage and compensation circuit can be programmed using external resistors and capacitors network. During shutdown, the load is disconnected from the battery. The device is packaged in tight QFN2x3-13.

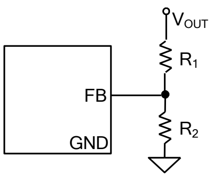
Applications Information

Because of the high integration in SY9702, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, inductor L and feedback resistors (R_1 and R_2) need to be selected for the targeted applications.

Feedback resistor divider R1 and R2

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light load, it is desirable to choose large resistance values for both R_1 and R_2. A value between 10k and 1M is recommended for both resistors. If R_1=100k is chosen, then R_2 can be calculated to be:

$$R_2 = \frac{0.6R_1}{V_{OUT} - 0.6}(\Omega)$$



Input capacitor C_{IN}

With the maximum load current at 2A, a typical X5R or better grade ceramic capacitor with 6.3V rating and greater than 22µF capacitors can handle this ripple current well. To minimize the potential noise problem, place this ceramic capacitor really close to the V_{IN} and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and VIN/GND pins.

Output capacitor C_{OUT}

Both steady state ripple and transient requirements must be taken into account when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor with 6.3V rating and more than two 22µF capacitors.

Output inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum average input current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN\_MAX})}{F_{SW} \times I_{OUT\_MAX} \times 40\%}(H)$$

where F_{SW} is the switching frequency and I_{OUT_MAX} is the maximum load current.

SY9702 is less sensitive to the ripple current variations. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of an inductor must be selected to guarantee an adequate margin to the peak inductor current under full load conditions. The maximum peak current happens under minimum input voltage condition.

$$I_{SAT,MIN} > \left(\frac{V_{OUT}}{V_{IN\_MIN}}\right) \times I_{OUT,MAX} + \frac{V_{IN\_MIN}}{V_{OUT}} \frac{(V_{OUT} - V_{IN\_MIN})}{2 \times F_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<15mΩ to achieve a good overall efficiency.

Enable Operation

Pulling the EN pin low (<0.4V) will shut down the device. During shutdown, the SY9702 shutdown current drops to lower than 0.1µA, Driving the EN pin high (>1.5V) will turn on the IC again.

Soft Start Programming

SY9702 provides an external soft-start pin that gradually raises the output voltage. The soft-start time can be programmed by the external capacitor across SS pin and GND. The soft start time is calculated as:

$$t_{ss} = \frac{0.7}{I_{ss}} \times C_{ss}$$

If a 20nF capacitor is used, the typical soft-start time will be 2.8ms. Don't leave SS pin floating.

Layout Design:

To achieve a higher efficiency and better noise immunity, following components should be placed close to the IC: C_{IN}, C_{OUT}, L, R_1 and R_2.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. Reasonable vias are suggested to be placed underneath the ground pad to enhance the soldering quality and thermal performance.

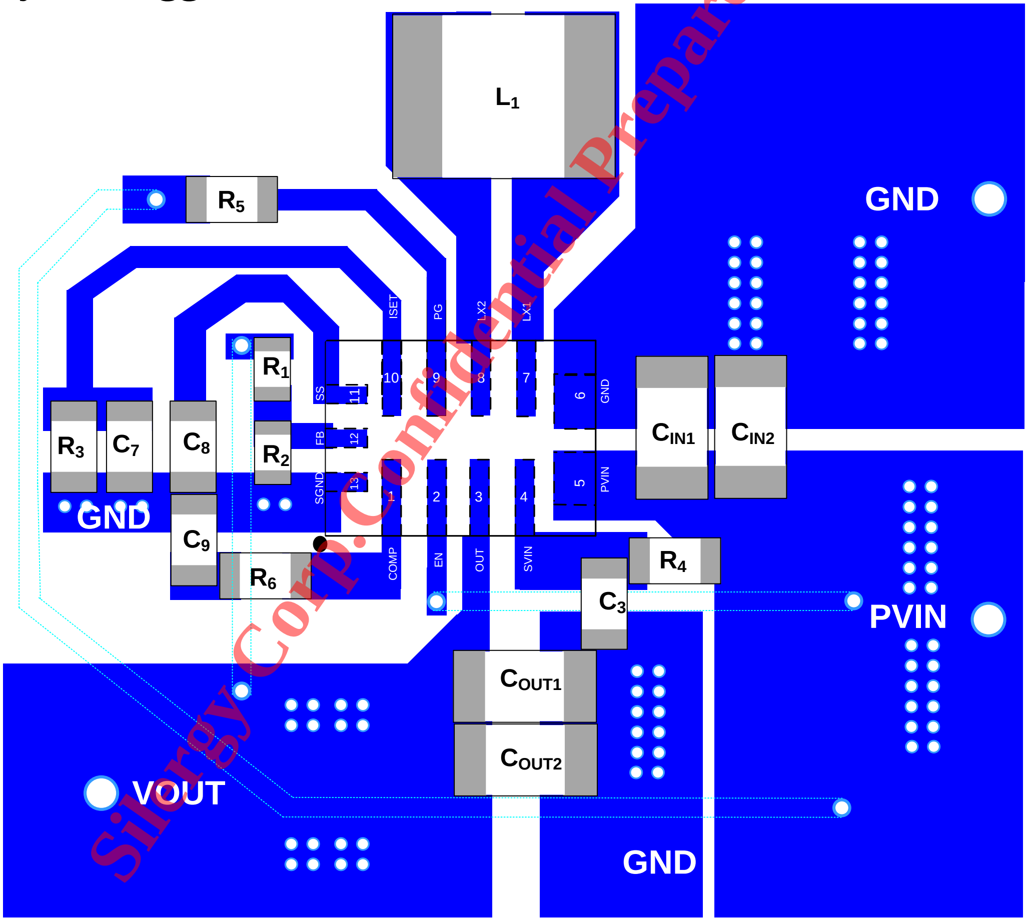
2) SVIN is the power supply pin for the internal control circuit. Don't connect SVIN pin to PVIN pin directly. A separated 1uF ceramic cap is strongly recommended to decouple SVIN pin to GND.

3) The decoupling capacitor of VIN must be placed close enough to the VIN pin and GND pins. The loop area formed by the input capacitors, VIN pin and GND pins must be minimized.

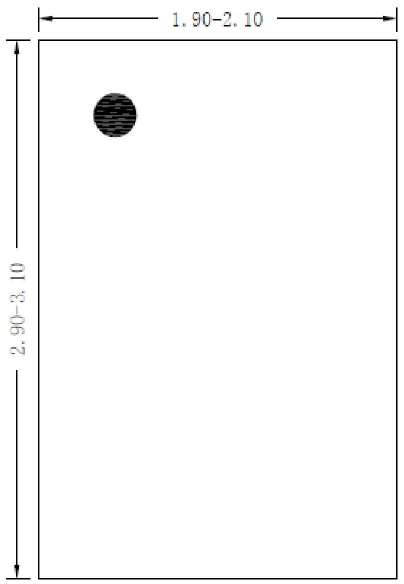
4) The PCB copper area associated with LX pin must be minimized to improve the noise immunity.

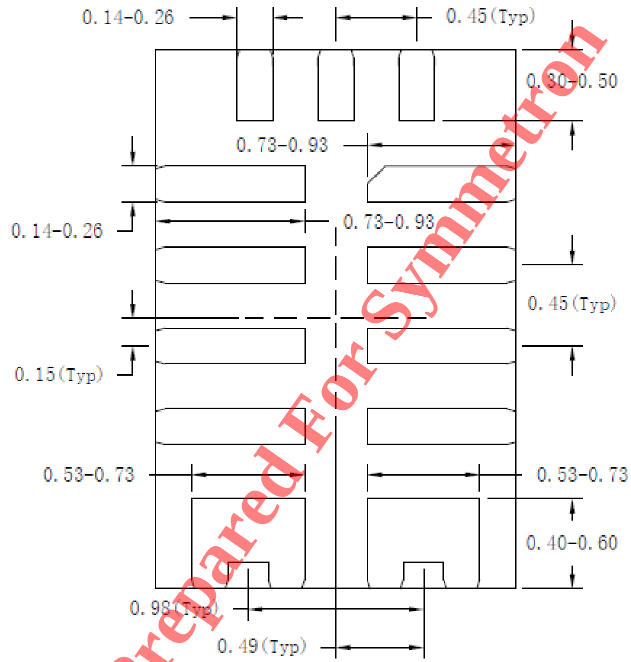
5) The components R_1, R_2 and the trace connecting to the FB/OUT pin must NOT be adjacent to the LX node on the PCB layout to minimize the noise coupling to FB/OUT pin.

PCB layout Suggestion



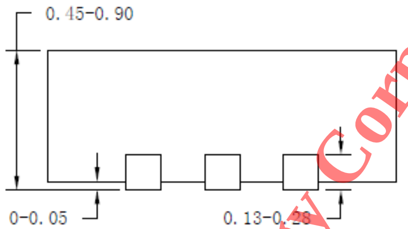
QFN2x3-13 Package Outline Drawing

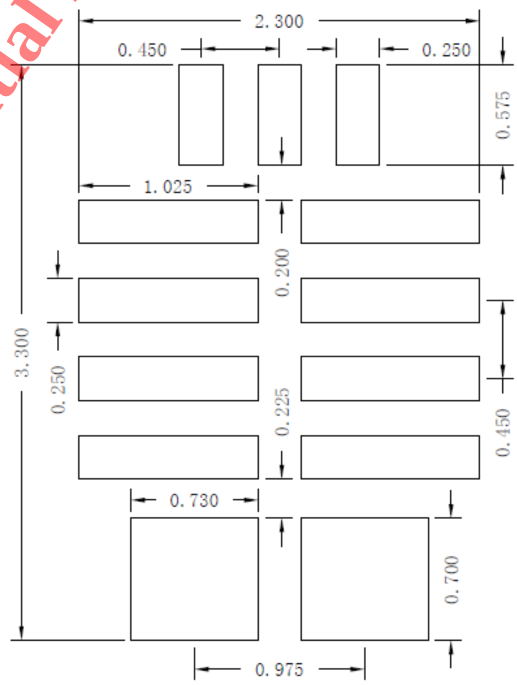




Top View

Bottom View





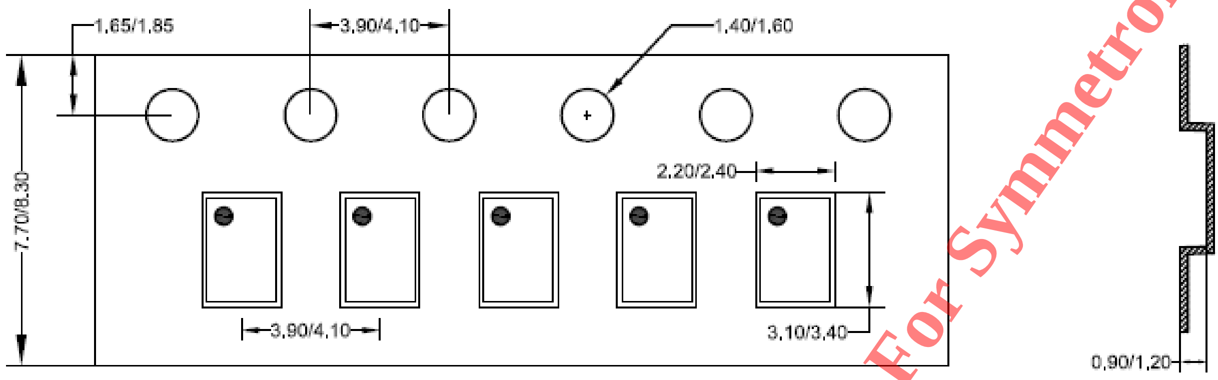
Side View

Recommended PCB layout
(Reference Only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

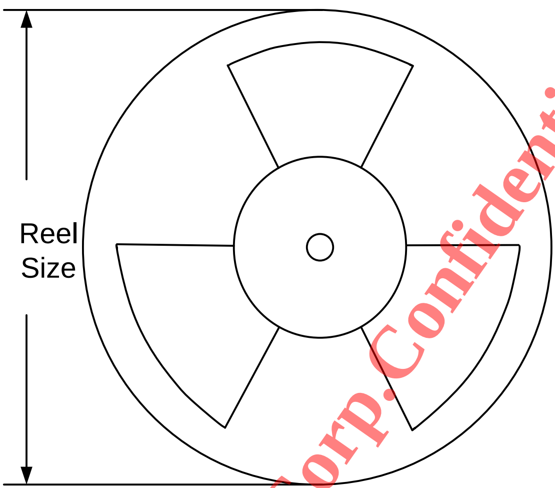
Taping & Reel Specification

1. QFN2x3-13 taping orientation



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN2x3	8	4	7"	400	160	3000

3. Others: NA

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