LMV727x Single and Dual, 1.8-V Low Power Comparators With Rail-to-Rail Input

1 Features

- (V_S = 1.8 V, T_A = 25°C, Typical Values Unless Specified).
- Single or Dual Supplies
- Ultra Low Supply Current 9 µA Per Channel
- Low Input Bias Current 10 nA
- Low Input Offset Current 200 pA
- Low Ensured V_{OS} 4 mV
- Propagation Delay 880 ns (20-mV Overdrive)
- Input Common Mode Voltage Range 0.1 V Beyond Rails
- LMV7272 is Available in DSBGA Package

2 Applications

- Wearable Devices
- Mobile Phones and Tablets
- Battery-Powered Electronics
- General Purpose Low Voltage Applications

3 Description

The LMV727x devices are rail-to-rail input low power comparators, characterized at supply voltages 1.8 V, 2.7 V, and 5 V. They consume as little as 9-uA supply current per channel while achieving a 800-ns propagation delay.

The LMV7271 and LMV7275 (single) are available in SC70 and SOT-23 packages. The LMV7272 (dual) is available in the DSBGA package. With these tiny packages, the PCB area can be significantly reduced. They are ideal for low voltage, low power, and space-critical designs.

The LMV7271 and LMV7272 both feature a push-pull output stage which allows operation with minimum power consumption when driving a load.

The LMV7275 features an open-drain output stage that allows for wired-OR configurations. The open-drain output also offers the advantage of allowing the output to be pulled to any voltage up to 5.5 V, regardless of the supply voltage of the LMV7275, which is useful for level-shifting applications.

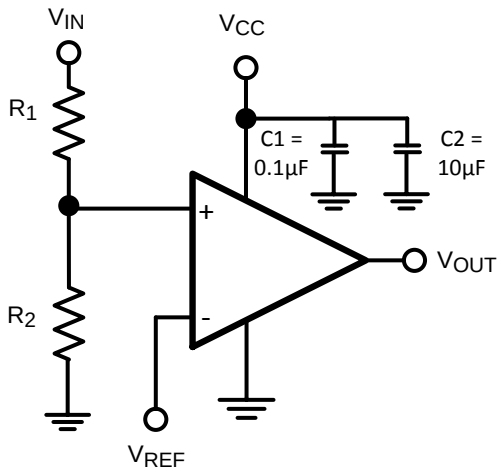
The LMV727x devices are built with Texas Instruments' advance submicron silicon-gate BiCMOS process. They all have bipolar inputs for improved noise performance, and CMOS outputs for rail-to-rail output swing.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMV7271, LMV7275	SC70 (5)	1.25 mm × 2.00 mm
	SOT-23 (5)	1.60 mm × 2.90 mm
LMV7272	DSBGA (8)	1.50 mm x 1.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Circuit



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (February 2013) to Revision I — **Page**

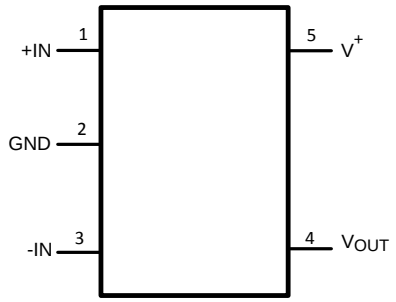
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Removed Soldering Information from *Absolute Maximum Ratings* table ... 4

Changes from Revision G (February 2013) to Revision H — **Page**

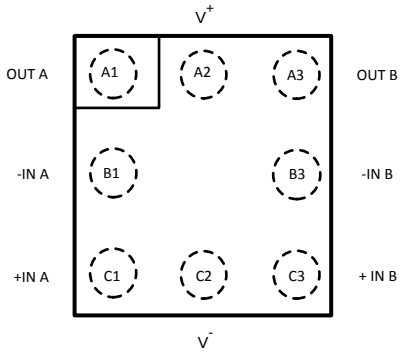
- Changed layout of National Data Sheet to TI format ... 19

5 Pin Configuration and Functions

DBV or DGK Package
5-Pin SOT-23 or SC70
Top View



YZR Package
8-Pin DSBGA
Top View



See *DSBGA Light Sensitivity* and *DSBGA Mounting* in the *Layout Guidelines* section for mounting precautions.

Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOT-23, SC70	DSBGA		
+IN	1	—	I	Noninverting Input
GND	2	—	P	Negative Supply Voltage
-IN	3	—	I	Invering Input
V_{OUT}	4	—	O	Output
V^+	5	A2	P	Positive Supply Voltage
OUT A	—	A1	O	Output, Channel A
-IN A	—	B1	I	Inverting Input, Channel A
+IN A	—	C1	I	Noninverting Input, Channel A
V^-	—	C2	P	Negative Supply Voltage
+IN B	—	C3	I	Noninverting Input, Channel B
-IN B	—	B3	I	Inverting Input, Channel B
OUT B	—	A3	O	Output, Channel B

6 Specifications

6.1 Absolute Maximum Ratings (1)(2)

	MIN	MAX	UNIT
V_{IN} Differential		±Supply Voltage	V
Supply Voltage (V^+ - V^-)		6	V
Voltage at Input/Output pins	(V^+) + 0.1	(V^-) − 0.1	V
Junction Temperature (3)		150	°C
Storage Temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office / Distributors for availability and specifications.
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly into a PCB.

6.2 ESD Ratings

			VALUE	UNIT
SOT-23, SC70 PACKAGE				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)(2)	±2000	V
		Machine Model (MM) (3)	±200	
DSBGA PACKAGE				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)(2)	±2000	V
		Machine Model (MM) (3)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Human body model, 1.5 kΩ in series with 100 pF.
(3) Machine Model, 0 Ω in series with 200 pF.

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Supply Voltage	1.8	5.5	V
Temperature (1)	–40	85	°C

(1) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly into a PCB.

6.4 Thermal Information

THERMAL METRIC (1)		LMV7271, LMV7275		LMV7272	UNIT
		DBV (SOT-23)	DGK (SC70)	YZR (DSBGA)	
		5 PINS	5 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	325	265	220	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly into a PCB.

6.5 1.8-V Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 1.8 V, V^- = 0 V.

PARAMETER		CONDITION		MIN(1)	TYP(2)	MAX(1)	UNIT
V_{OS}	Input Offset Voltage				0.3	4	mV
		At the temperature extremes				6	
TC V_{OS}	Input Offset Temperature Drift	V_{CM} = 0.9 V (3)			20		uV/°C
I_B	Input Bias Current				10		nA
I_{OS}	Input Offset Current				200		pA
I_S	Supply Current	LMV7271/LMV7275			9	12	µA
			At the temperature extremes			14	
		LMV7272			18	25	µA
			At the temperature extremes			28	
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 0.9 V (LMV7271/LMV7272 only)		3.5	6		mA
		Sinking, V_O = 0.9 V		4	6		
V_{OH}	Output Voltage High (LMV7271/LMV7272 only)	I_O = 0.5 mA		1.7	1.74		V
		I_O = 1.5 mA		1.47	1.63		
V_{OL}	Output Voltage Low	I_O = −0.5 mA			52	100	mV
		I_O = −1.5 mA			166	220	
V_{CM}	Input Common-Mode Voltage Range	CMRR > 45 dB				1.9	V
				−0.1			V
CMRR	Common-Mode Rejection Ratio	0 < V_{CM} < 1.8 V		46	78		dB
PSRR	Power Supply Rejection Ratio	V^+ = 1.8 V to 5 V		55	80		dB
$I_{LEAKAGE}$	Output Leakage Current	V_O = 1.8 V (LMV7275 only)			2		pA

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Offset Voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

6.6 1.8-V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 1.8 V, V^- = 0 V, V_{CM} = 0.5 V, V_O = V^+/2 and R_L > 1 MΩ to V^-.

PARAMETER		CONDITION	MIN(1)	TYP(2)	MAX(1)	UNIT
t_{PHL}	Propagation Delay (High to Low)	Input Overdrive = 20 mV Load = 50 pF//5 kΩ		880		ns
		Input Overdrive = 50 mV Load = 50 pF//5 kΩ		570		ns
t_{PLH}	Propagation Delay (Low to High)	Input Overdrive = 20 mV Load = 50 pF//5 kΩ		1100		ns
		Input Overdrive = 50 mV Load = 50 pF//5 kΩ		800		ns

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.

6.7 2.7-V Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 2.7 V, V^- = 0 V.

PARAMETER		CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
V_{OS}	Input Offset Voltage				0.3	4	mV
		At the temperature extremes				6	
TC V_{OS}	Input Offset Temperature Drift	V_{CM} = 1.35 V(3)			20		µV/°C
I_B	Input Bias Current				10		nA
I_{OS}	Input offset Current				200		pA
I_S	Supply Current	LMV7271/LMV7275			9	13	µA
			At the temperature extremes			15	
		LMV7272			18	25	µA
			At the temperature extremes			28	
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 1.35 V (LMV7271/LMV7272 only)		10	15		mA
		Sinking, V_O = 1.35 V		10	15		
V_{OH}	Output Voltage High (LMV7271/LMV7272 only)	I_O = 0.5 mA		2.63	2.66		V
		I_O = 2.0 mA		2.48	2.55		
V_{OL}	Output Voltage Low	I_O = −0.5 mA			50	70	mV
		I_O = −2 mA			155	220	
V_{CM}	Input Common Voltage Range	CMRR > 45 dB				2.8	V
				−0.1			V
CMRR	Common-Mode Rejection Ratio	0 < V_{CM} < 2.7 V		46	78		dB
PSRR	Power Supply Rejection Ratio	V^+ = 1.8 V to 5 V		55	80		dB
$I_{LEAKAGE}$	Output Leakage Current	V_O = 2.7 V (LMV7275 only)			2		pA

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Offset Voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

6.8 2.7-V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 2.7 V, V^- = 0 V, V_{CM} = 0.5 V, V_O = V^+/2 and R_L > 1 MΩ to V^-.

PARAMETER		CONDITION	MIN(1)	TYP(2)	MAX(1)	UNIT
t_{PHL}	Propagation Delay (High to Low)	Input Overdrive = 20 mV Load = 50 pF//5 kΩ		1200		ns
		Input Overdrive = 50 mV Load = 50 pF//5 kΩ		810		ns
t_{PLH}	Propagation Delay (Low to High)	Input Overdrive = 20 mV Load = 50 pF//5 kΩ		1300		ns
		Input Overdrive = 50 mV Load = 50 pF//5 kΩ		860		ns

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.

6.9 5-V Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 5 V, V^- = 0 V.

PARAMETER		CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
V_{OS}	Input Offset Voltage				0.3	4	mV
		At the temperature extremes				6	
TC V_{OS}	Input Offset Temperature Drift	V_{CM} = 2.5 V(3)			20		µV/°C
I_B	Input Bias Current				10		nA
I_{OS}	Input Offset Current				200		pA
I_S	Supply Current	LMV7271/LMV7275			10	14	µA
			At the temperature extremes			16	
		LMV7272			20	27	µA
			At the temperature extremes			30	
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 2.5 V (LMV7271/LMV7272 only)		18	34		mA
		Sinking, V_O = 2.5 V		18	34		
V_{OH}	Output Voltage High (LMV7271/LMV7272 only)	I_O = 0.5 mA		4.93	4.96		V
		I_O = 4.0 mA		4.675	4.77		
V_{OL}	Output Voltage Low	I_O = −0.5 mA			27	70	mV
		I_O = −4.0 mA			225	315	
V_{CM}	Input Common Voltage Range	CMRR > 45 dB				5.1	V
				−0.1			
CMRR	Common-Mode Rejection Ratio	0 < V_{CM} < 5.0 V		46	78		dB
PRSS	Power Supply Rejection Ratio	V^+ = 1.8 V to 5 V		55	80		dB
$I_{LEAKAGE}$	Output Leakage Current	V_O = 5 V (LMV7275 only)			2		pA

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Offset Voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

6.10 5-V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 5.0 V, V^- = 0 V, V_{CM} = 0.5 V, V_O = V^+/2 and R_L > 1 MΩ to V^-.

PARAMETER		CONDITION	MIN(1)	TYP(2)	MAX(1)	UNIT
t_{PHL}	Propagation Delay (High to Low)	Input Overdrive = 20 mV Load = 50 pF//5 kΩ		2100		ns
		Input Overdrive = 50 mV Load = 50 pF//5 kΩ		1380		ns
t_{PLH}	Propagation Delay (Low to High)	Input Overdrive = 20 mV Load = 50 pF//5 kΩ		1800		ns
		Input Overdrive = 50 mV Load = 50 pF//5 kΩ		1100		ns

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.

6.11 Typical Characteristics

T_A = 25°C, Unless otherwise specified.

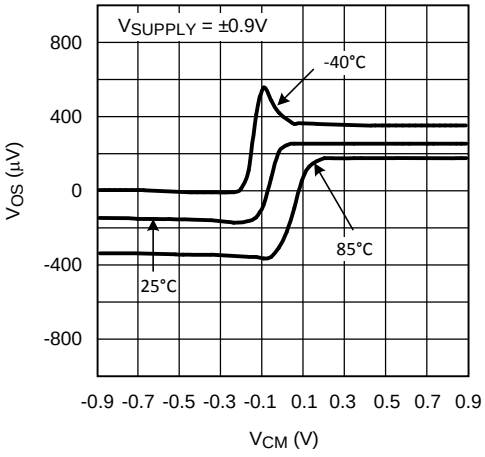


Figure 1. V_{OS} vs. V_{CM}

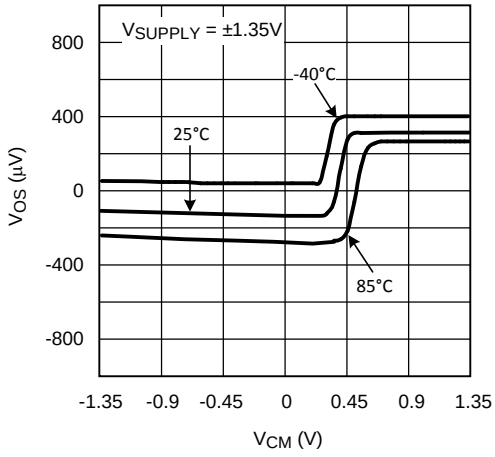


Figure 2. V_{OS} vs. V_{CM}

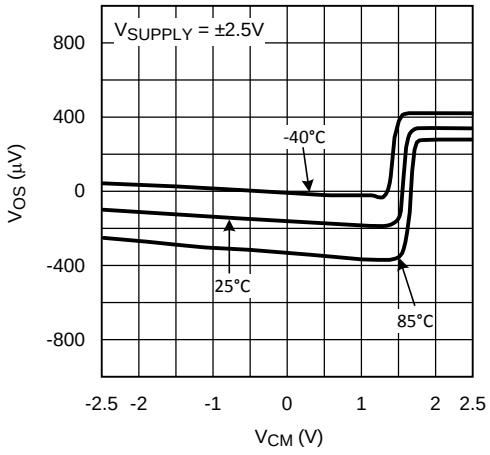


Figure 3. V_{OS} vs. V_{CM}

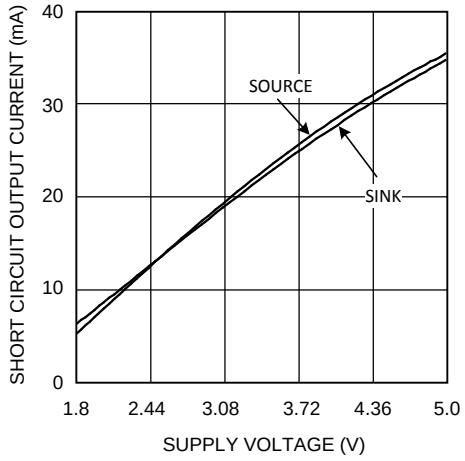


Figure 4. Short Circuit vs. Supply Voltage

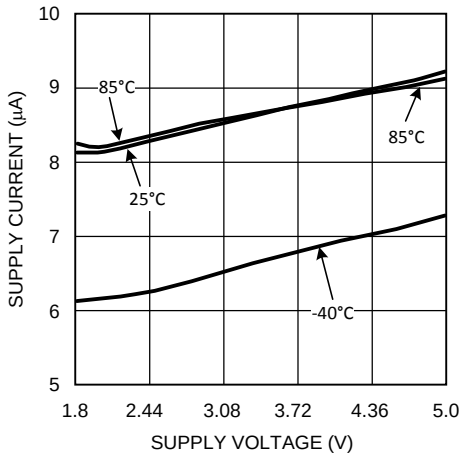


Figure 5. Supply Current vs. Supply Voltage (LMV7271)

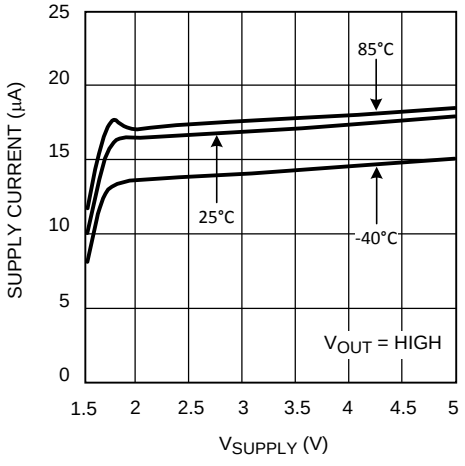


Figure 6. Supply Current vs. Supply Voltage (LMV7272)

Typical Characteristics (continued)

T_A = 25°C, Unless otherwise specified.

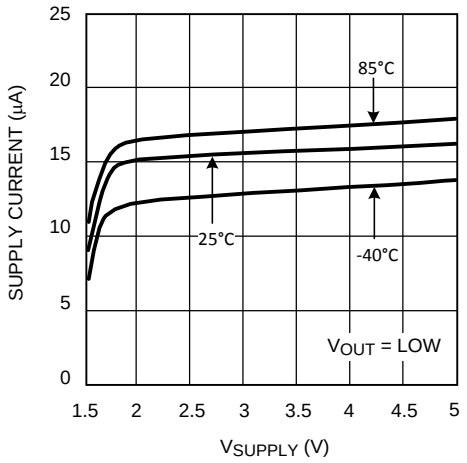


Figure 7. Supply Current vs. Supply Voltage (LMV7272)

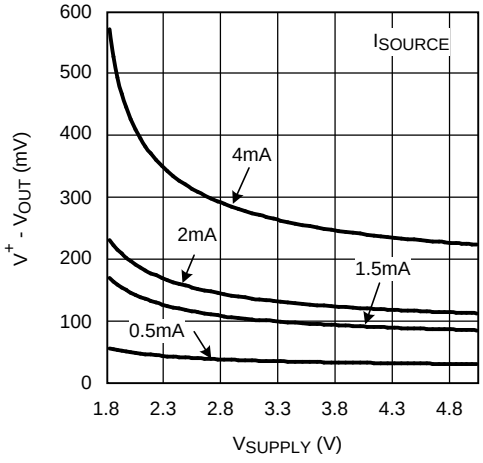


Figure 8. Output Positive Swing vs. V_{SUPPLY}

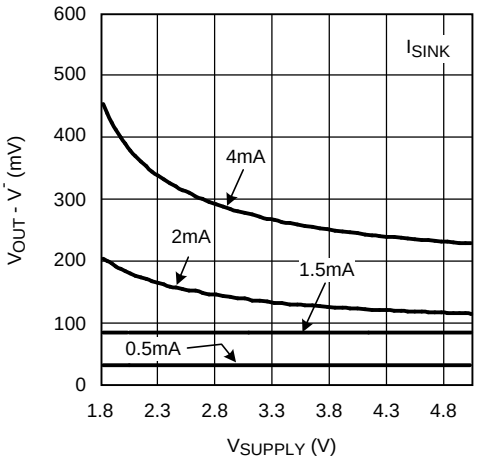


Figure 9. Output Negative Swing vs. V_{SUPPLY}

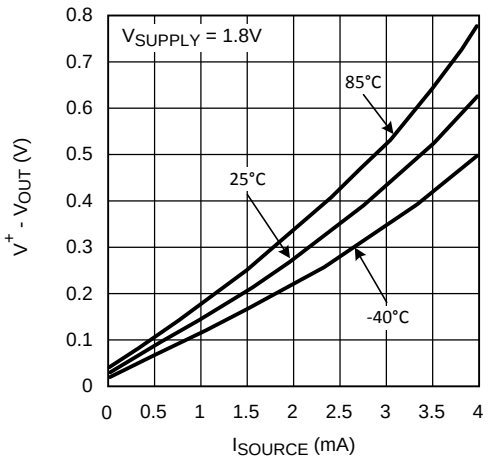


Figure 10. Output Positive Swing vs. I_{SOURCE}

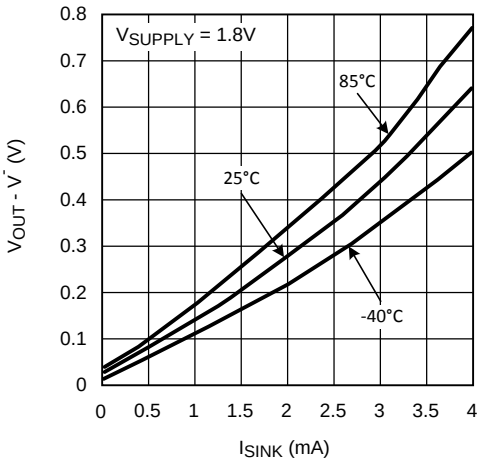


Figure 11. Output Negative Swing vs. I_{SINK}

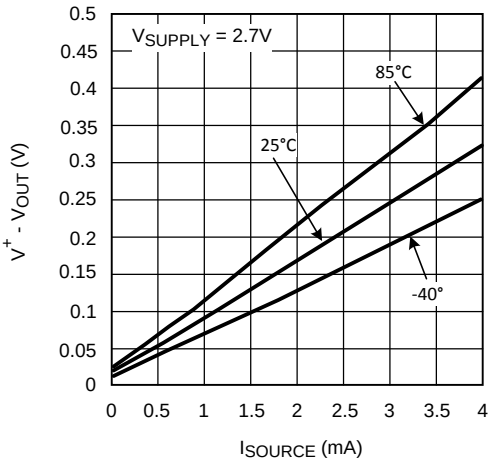


Figure 12. Output Positive Swing vs. I_{SOURCE}

Typical Characteristics (continued)

T_A = 25°C, Unless otherwise specified.

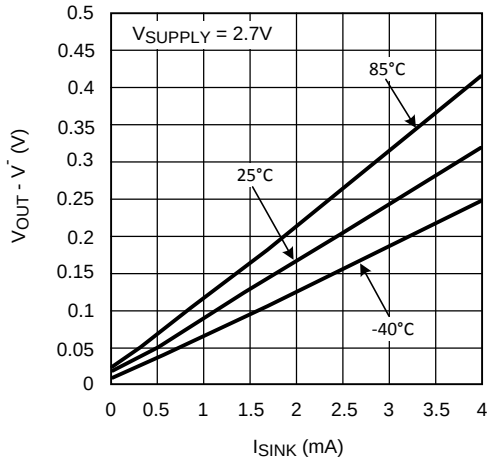


Figure 13. Output Negative Swing vs. I_{SINK}

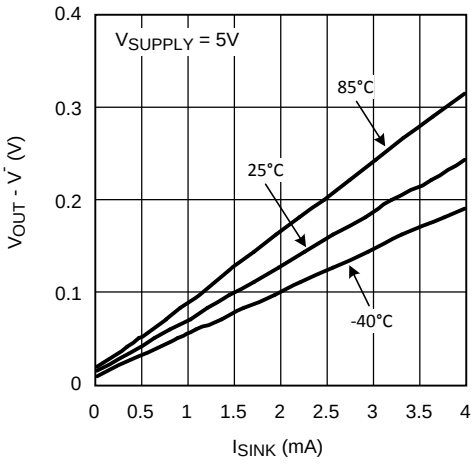


Figure 14. Output Negative Swing vs. I_{SINK}

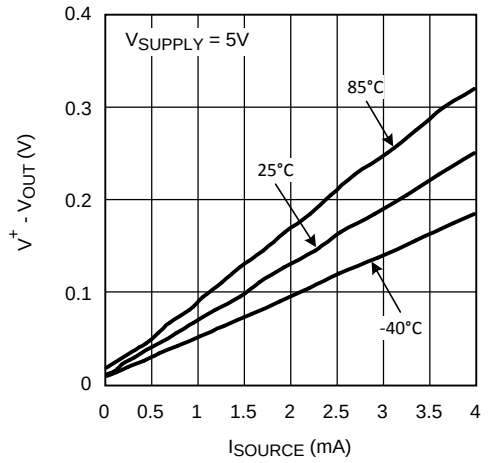


Figure 15. Output Positive Swing vs. I_{SOURCE}

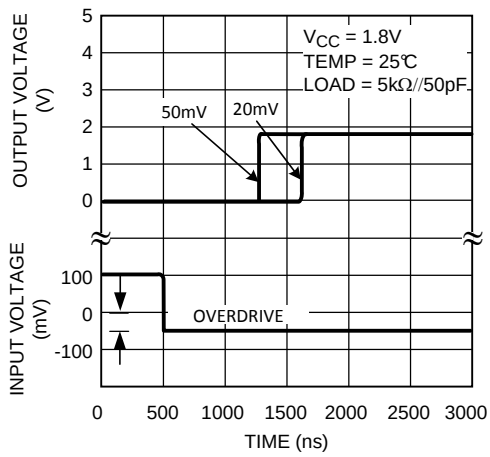


Figure 16. Propagation Delay (t_{PLH})

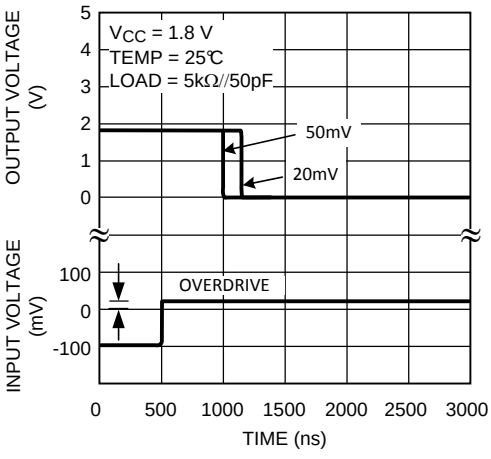


Figure 17. Propagation Delay (t_{PHL})

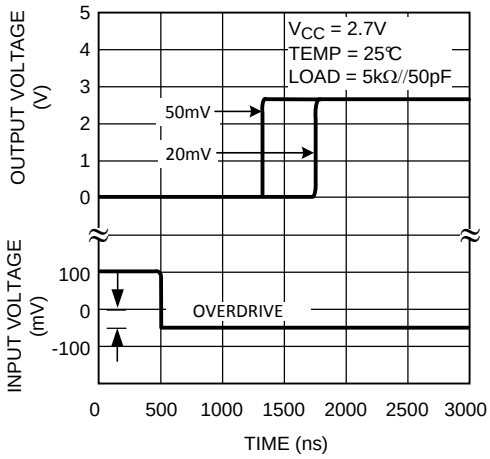


Figure 18. Propagation Delay (t_{PLH})

Typical Characteristics (continued)

T_A = 25°C, Unless otherwise specified.

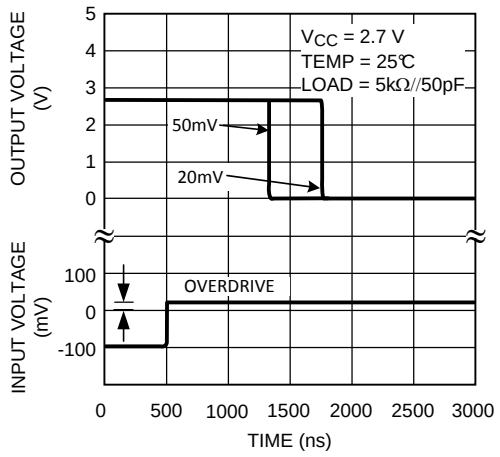


Figure 19. Propagation Delay (t_{PHL})

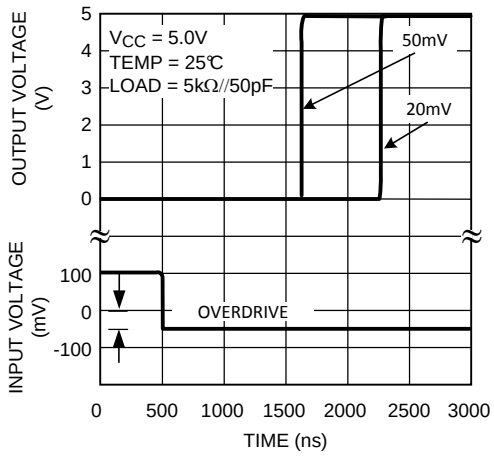


Figure 20. Propagation Delay (t_{PLH})

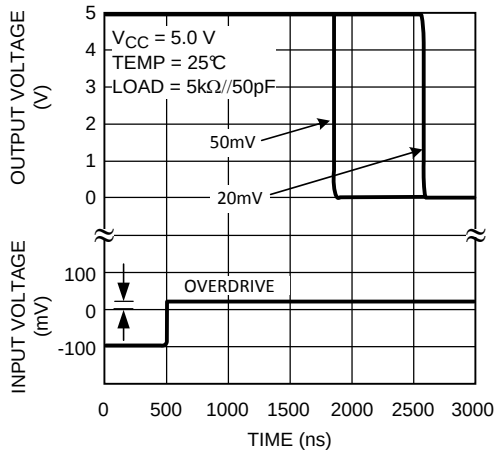


Figure 21. Propagation Delay (t_{PHL})

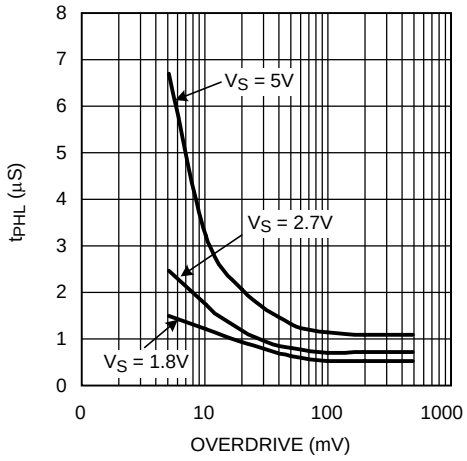


Figure 22. t_{PHL} vs. Overdrive

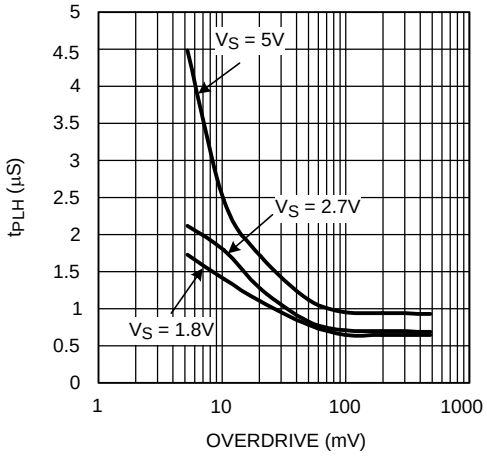


Figure 23. t_{PLH} vs. Overdrive

7 Detailed Description

7.1 Overview

A comparator is often used to convert an analog signal to a digital signal. As shown in Figure 24, the comparator compares an input voltage (V_{IN}) to a reference voltage (V_{REF}). If V_{IN} is less than V_{REF}, the output (V_O) is low. However, if V_{IN} is greater than V_{REF}, the output voltage (V_O) is high.

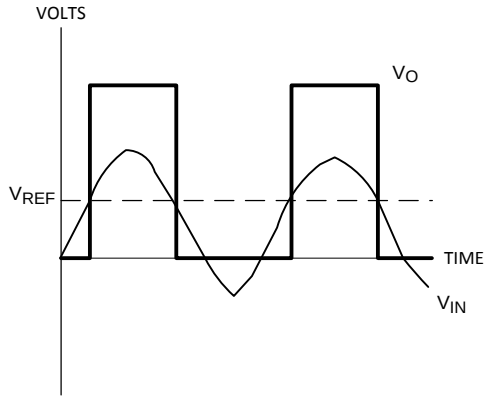
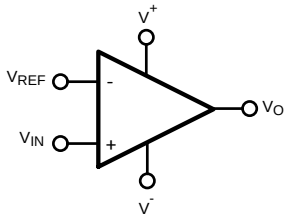


Figure 24. LMV7271 Basic Comparator

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Rail-to-Rail Input Stage

The LMV727X has an input common mode voltage range (V_{CM}) of −0.1V below the V^- to 0.1 V above V^+. This is achieved by using paralleled PNP and NPN differential input pairs. When the V_{CM} is near V^+, the NPN pair is on and the PNP pair is off. When the V_{CM} is near V^-, the NPN pair is off and the PNP pair is on. The crossover point between the NPN and PNP input stages is around 950mV from V^+. Because each input stage has its own offset voltage (V_{OS}), the V_{OS} of the comparator becomes a function of the V_{CM}. See curves for V_{OS} vs. V_{CM} in the *Typical Characteristics* section. In application design, it is recommended to keep the V_{CM} away from the crossover point to avoid problems. The wide input voltage range makes LMV727X ideal in power supply monitoring circuits, where the comparators are used to sense signals close to ground and power supplies.

Feature Description (continued)

7.3.2 Output Stage, LMV7271 and LMV7272

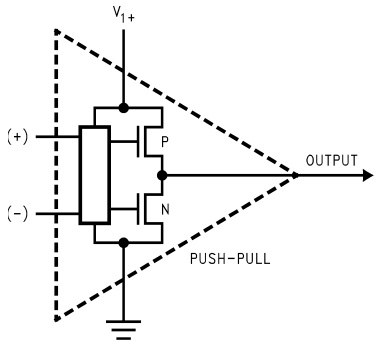


Figure 25. LMV7271 and LMV7272 Push-Pull Output Stage

The LMV7271 and LMV7272 have a push-pull output stage. This output stage keeps the total system power consumption to the absolute minimum by eliminating the need for a pullup resistor. The only current consumed is the low supply current and the current going directly into the load.

When the output switches, both PMOS and NMOS at the output stage are on at the same time for a very short time. This allows current to flow directly between V^+ and V^- through output transistors. The result is a short spike of current (called *shoot-through* current) drawn from the supply and glitches in the supply voltages. The glitches can spread to other parts of the board as noise. To prevent the glitches in supply lines, power supply bypass capacitors must be installed. See *Circuit Techniques for Avoiding Oscillations in Comparator Applications* for supply bypassing for details.

7.3.3 Output Stage, LMV7275

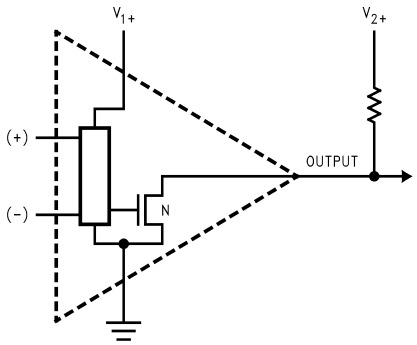


Figure 26. LMV7275 Open-Drain Output

The LMV7275 has an open-drain output that requires a pullup resistor to a positive supply voltage for the output to operate properly. The internal circuitry is identical to the LMV7271 except that the upper P-channel output device is absent. When the internal output transistor is off, the output voltage will be pulled up to the external positive voltage by the external pullup resistor. This allows the output to be OR'ed with other open-drain outputs on the same bus. The output pullup resistor may be connected to any voltage level between V- and V+ for level shifting applications.

7.4 Device Functional Modes

7.4.1 Capacitive and Resistive Loads

The propagation delay is not affected by capacitive loads at the output of the LMV7271 or LMV7272. However, resistive loads slightly effect the propagation delay on the falling edge depending on the load resistance value.

The propagation delay on the rising edge of the LMV7275 depends on the load resistance and capacitance values.

Device Functional Modes (continued)

7.4.2 Noise

Most comparators have rather low gain. This allows the output to alternate between high and low when the input signal changes slowly. The result is the output may oscillate between high and low when the differential input is near zero and triggers on noise. The high gain of this comparator eliminates this problem. Less than 1 μV of change on the input will drive the output from one rail to the other rail. If the input signal is noisy, the output cannot ignore the noise unless some hysteresis is provided by positive feedback. (See *Hysteresis*.)

7.4.3 Hysteresis

It is a standard procedure to use hysteresis (positive feedback) around a comparator to prevent oscillation due to the comparator triggering its own noise on slowly ramping signals. The following sections will describe various ways to apply hysteresis.

7.4.3.1 Noninverting Comparator With Hysteresis

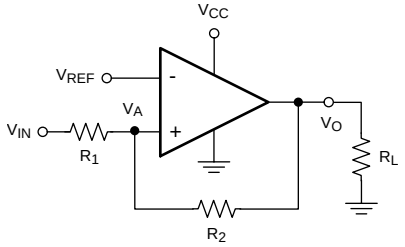


Figure 27. Noninverting Comparator With Hysteresis

A noninverting comparator with hysteresis requires a two resistor network, and a voltage reference (V_{REF}) at the inverting input. When V_{IN} is low, the output is also low. For the output to switch from low to high, V_{IN} must rise up to V_{IN1} where V_{IN1} is calculated by:

$$\Delta V_{IN1} = \frac{V_{REF}(R_1 + R_2)}{R_2} \quad (1)$$

As soon as V_O switches to V_{CC}, V_A steps to a value greater than V_{REF} which is given by:

$$V_A = V_{IN} + \frac{(V_{CC} - V_{IN1})R_1}{R_1 + R_2} \quad (2)$$

To make the comparator switch back to its low state, V_{IN} must equal V_{REF} before V_A will again equal V_{REF}. V_{IN2} can be calculated by:

$$V_{IN2} = \frac{V_{REF}(R_1 + R_2) - V_{CC} R_1}{R_2} \quad (3)$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}.

$$\Delta V_{IN} = V_{CC} R_1 / R_2 \quad (4)$$

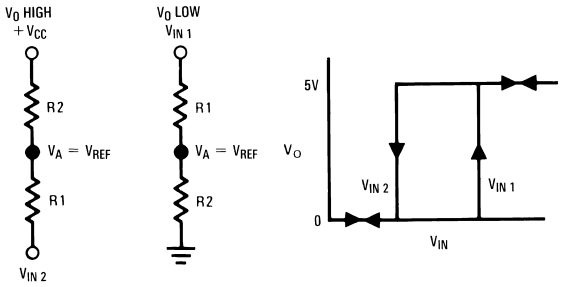


Figure 28. Noninverting Comparator Thresholds

Device Functional Modes (continued)

7.4.3.2 Inverting Comparator With Hysteresis

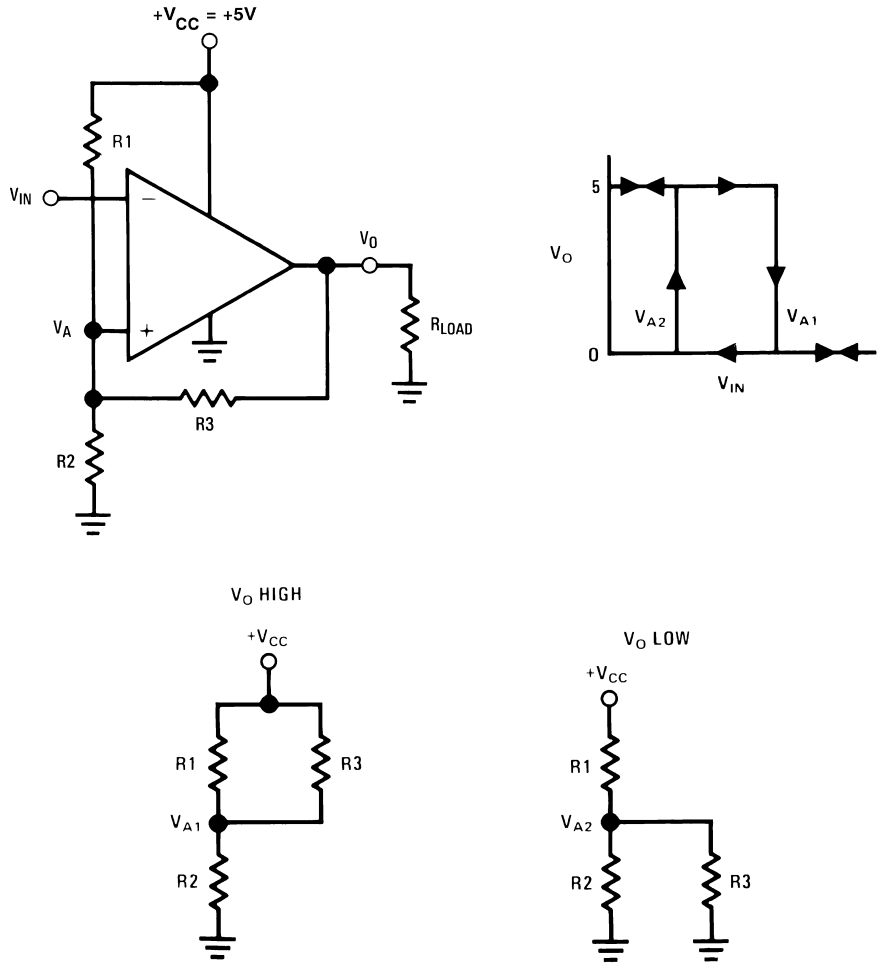


Figure 29. Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three resistor network that is referenced to the supply voltage V_{CC} of the comparator (Figure 29). When V_{IN} at the inverting input is less than V_A, the voltage at the noninverting node of the comparator ($V_{IN} < V_A$), the output voltage is high (for simplicity assume V_O switches as high as V_{CC}). The three network resistors can be represented as $R_1||R_3$ in series with R_2. The lower input trip voltage V_{A1} is defined as

$$V_{A1} = \frac{V_{CC}\, R_2}{(R_1||R_3) + R_2} \tag{5}$$

When V_{IN} is greater than V_A ($V_{IN} > V_A$), the output voltage is low and very close to ground. In this case the three network resistors can be presented as $R_2//R_3$ in series with R_1. The upper trip voltage V_{A2} is defined as

$$V_{A2} = \frac{V_{CC}\,(R_2||R_3)}{R_1 + (R_2||R_3)} \tag{6}$$

The total hysteresis provided by the network is defined as

$$\Delta V_A = V_{A1} - V_{A2} \tag{7}$$

A good typical value of ΔV_A would be in the range of 5 to 50 mV. This is easily obtained by choosing R_3 as 1000 to 100 times ($R_1||R_2$) for 5-V operation, or as 300 to 30 times ($R_1||R_2$) for 1.8-V operation.

Device Functional Modes (continued)

7.4.4 Zero Crossing Detector

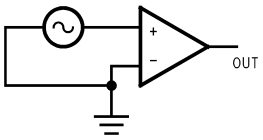


Figure 30. Simple Zero Crossing Detector

In a zero crossing detector circuit, the inverting input is connected to ground and the noninverting input is connected to a 100 mV_{PP} AC signal. As the signal at the noninverting input crosses 0 V, the output of the comparator changes state.

7.4.4.1 Zero Crossing Detector With Hysteresis

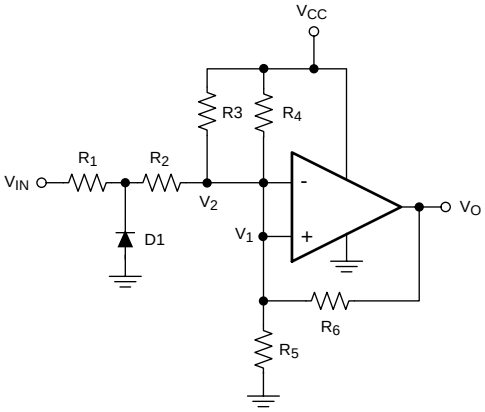


Figure 31. Zero Crossing Detector With Hysteresis

To improve switching times and centering the input threshold to ground a small amount of positive feedback is added to the circuit. Voltage divider R_4 and R_5 establishes a reference voltage, V_1, at the positive input. By making the series resistance, R_1 plus R_2 equal to R_5, the switching condition, $V_1 = V_2$, will be satisfied when $V_{IN} = 0$.

The positive feedback resistor, R_6, is made very large with respect to $R_5 \parallel R_6 = 2000\ R_5$). The resultant hysteresis established by this network is very small ($\Delta V_1 < 10$ mV) but it is sufficient to insure rapid output voltage transitions.

Diode D_1 is used to insure that the inverting input terminal of the comparator never goes below approximately −100 mV. As the input terminal goes negative, D_1 will forward bias, clamping the node between R_1 and R_2 to approximately −700 mV. This sets up a voltage divider with R_2 and R_3 preventing V_2 from going below ground. The maximum negative input overdrive is limited by the current handling ability of D_1.

7.4.5 Threshold Detector

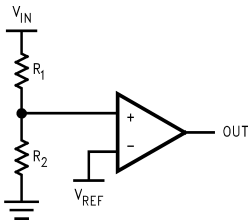


Figure 32. Threshold Detector

Device Functional Modes (continued)

Instead of tying the inverting input to 0 V, the inverting input can be tied to a reference voltage. As the input on the noninverting input passes the V_{REF} threshold, the output of the comparator changes state. It is important to use a stable reference voltage to ensure a consistent switching point.

7.4.6 Universal Logic Level Shifter (LMV7275 only)

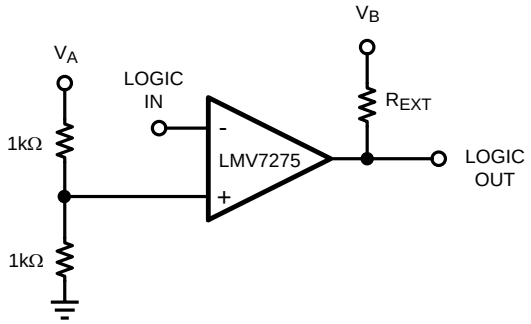


Figure 33. Logic Level Shifter

The output of LMV7275 is an unconnected drain of an NMOS device, which can be pulled up, through a resistor, to any desired output level within the permitted power supply range. Hence, the following simple circuit works as a universal logic level shifter, pulling up the signal to the desired level.

For example, V_A could be the 5-V analog supply voltage, where V_B could be the 3.3-V supply of the processor. The output will now be compatable with the 3.3-V logic.

7.4.7 OR'ING the Output (LMV7275 only)

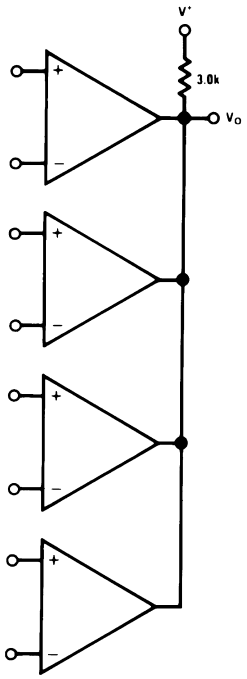


Figure 34. OR'ing the Outputs

Because the LMV7275 output is an unconnected NMOS drain, many open-drain outputs can be tied together, pulled up to V^+ by a common resistor to provide an output OR'ing function. If any of the comparator outputs goes low, the output V_O goes low.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMV727x devices are single-supply comparators with 880 ns of propagation delay and only 12 µA of supply current.

8.2 Typical Applications

8.2.1 Square Wave Oscillator

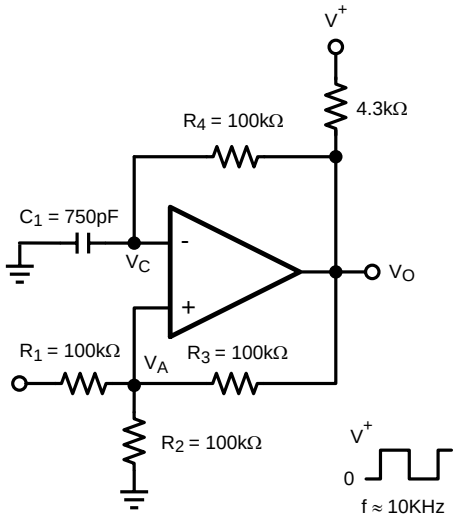


Figure 35. Square Wave Oscillator Application

8.2.1.1 Design Requirements

A typical application for a comparator is as a square wave oscillator. Figure 35 generates a square wave whose period is set by the RC time constant of the capacitor $C_1$and resistor R_4. The maximum frequency is limited by the large signal propagation delay of the comparator, and by the capacitive loading at the output, which limits the output slew rate.

8.2.1.2 Detailed Design Procedure

To analyze the circuit, consider it when the output is high. That implies that the inverted input (V_C) is lower than the noninverting input (V_A).

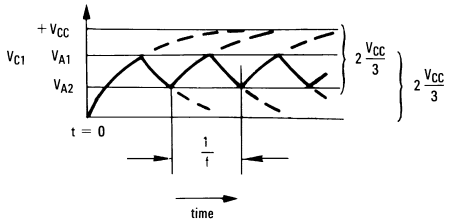


Figure 36. Squarewave Oscillator Timing Thresholds

Typical Applications (continued)

This causes the C_1 to get charged through R_4, and the voltage V_C increases till it is equal to the noninverting input. The value of V_A at this point is

$$V_{A1} = \frac{V_{CC} \cdot R_2}{R_2 + R_1 \| R_3} \tag{8}$$

If $R_1 = R_2 = R_3$, then $V_{A1} = 2V_{CC}/3$

At this point the comparator switches pulling down the output to the negative rail. The value of V_A at this point is

$$V_{A2} = \frac{V_{CC} (R_2 \| R_3)}{R_1 + (R_2 \| R_3)} \tag{9}$$

If $R_1 = R_2 = R_3$, then $V_{A2} = V_{CC}/3$

The capacitor C_1 now discharges through R_4, and the voltage V_C decreases till it is equal to V_{A2}, at which point the comparator switches again, bringing it back to the initial stage. The time period is equal to twice the time it takes to discharge C_1 from $2V_{CC}/3$ to $V_{CC}/3$, which is given by $R_4C_1.\ln 2$. Hence the formula for the frequency is:

$F = 1/(2 \cdot R_4 \cdot C_1 \cdot \ln 2)$

8.2.1.3 Application Curve

Figure Figure 37 shows the simulated results of an oscillator using the following values:

1. $R_1 = R_2 = R_3 = R_4 = 100\ k\Omega$
2. $C_1 = 750$ pF, $C_L = 20$ pF
3. V+ = 5 V, V- = GND
4. C_{STRAY} (not shown) from Va to GND = 10 pF

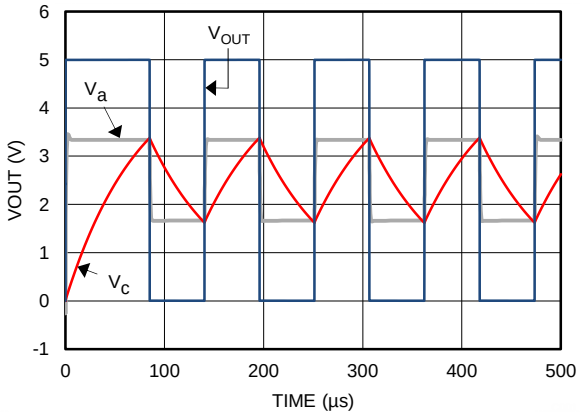


Figure 37. Square Wave Oscillator Output Waveforms

Typical Applications (continued)

8.2.2 Positive Peak Detector

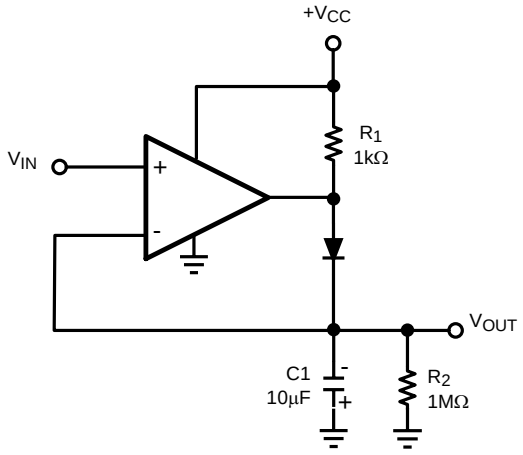


Figure 38. Positive Peak Detector

The positive peak detect circuit is basically a comparator operated in a unity gain follower configuration, with a capacitor as a load to store the highest voltage. A diode is added at the output to prevent the capacitor from discharging through the pullup resistor. When the input V_{IN} increases, the inverting input of the comparator follows it, thus charging the capacitor. When the input voltage decreases, the cap discharges through the 1-MΩ resistor.

The decay time can be modified by changing R2. The output should be accessed through a high-impedance input follower circuit to prevent loading. Upper output swing headroom is determined by the forward voltage of the diode ($V_{MAX} = V_{CC} – V_F$). A Shottky signal diode can be used to reduce the required headroom to around 300 mV.

This circuit can use any of the LMV727x devices, but R1 is not required for the LMV7271 or LMV7272.

8.2.3 Negative Peak Detector

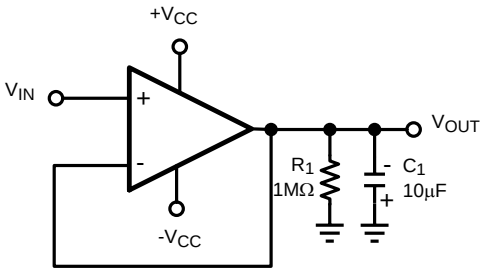


Figure 39. Negative Peak Detector (LMV7275 Only)

The Negative Peak Detector circuit will store the peak negative voltage below ground (0 V to $–V_{CC}$). For the negative detector, the LMV7275 must be used because the output transistor acts as a low-impedance current sink. Because there is no pullup resistor, the only discharge path will be the 1-MΩ resistor and any load impedance used. Decay time is changed by varying the 1-MΩ resistor.

NOTE

The negative peak detector does require a negative supply voltage! $+_{VCC}$ can be grounded to save dynamic range because the output does not swing above ground

Typical Applications (continued)

8.2.4 Window Detector

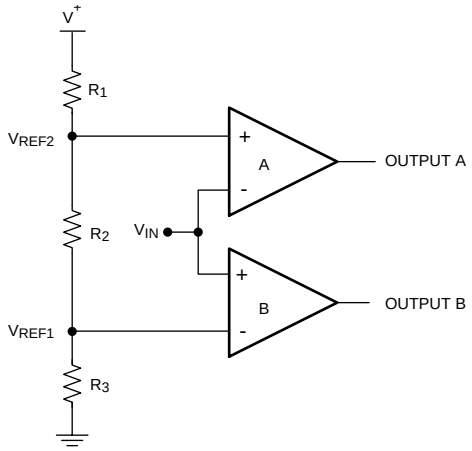


Figure 40. Window Detector

A window detector monitors the input signal to determine if it falls between two voltage levels. Both outputs are true (high) when $V_{REF1} < V_{IN} < V_{REF2}$

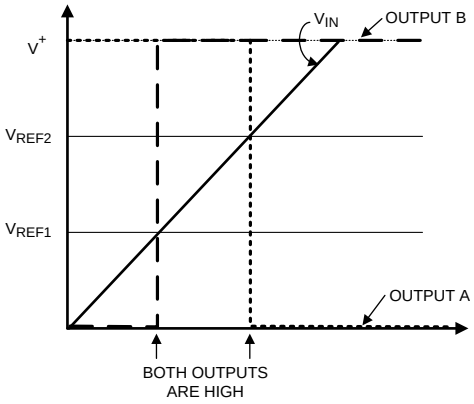


Figure 41. Window Detector Output Signal

The comparator outputs A and B are high only when $V_{REF1} < V_{IN} < V_{REF2}$, or *within the window*, where these are defined as:

$$V_{REF1} = R_3 / R_1 + R_2 + R_3) \times V+ \quad (10)$$

$$V_{REF2} = R_2 + R_3) / R_1 + R_2 + R_3) \times V+ \quad (11)$$

To determine if the input signal falls outside of the two voltage levels, both inputs on each comparators can be reversed to invert the logic.

The LMV7275 with an open-drain output should be used if the outputs are to be tied together for a common logic output.

Other names for window detectors are: threshold detector, level detector, and amplitude trigger or detector.

9 Power Supply Recommendations

To minimize supply noise, power supplies should be decoupled by a 0.01-µF ceramic capacitor in parallel with a 10-µF capacitor.

Due to the nanosecond edges on the output transition, peak supply currents will be drawn during the time the output is transitioning. Peak current depends on the capacitive loading on the output. The output transition can cause transients on poorly bypassed power supplies. These transients can cause a poorly bypassed power supply to *ring* due to trace inductance and low self-resonance frequency of high ESR bypass capacitors.

Treat the LMV727x as a high-speed device. Keep the ground paths short and place small (low-ESR ceramic) bypass capacitors directly between the V+ and V– pins.

Output capacitive loading and output toggle rate will cause the average supply current to rise over the quiescent current.

10 Layout

10.1 Layout Guidelines

10.1.1 Circuit Techniques for Avoiding Oscillations in Comparator Applications

Feedback to almost any pin of a comparator can result in oscillation. In addition, when the input signal is a slow voltage ramp or sine wave, the comparator may also burst into oscillation near the crossing point. To avoid oscillation or instability, PCB layout should be engineered thoughtfully. Several precautions are recommended:

1. Power supply bypassing is critical, and will improve stability and transient response. Resistance and inductance from power supply wires and board traces increase power supply line impedance. When supply current changes, the power supply line will move due to its impedance. Large enough supply line shift will cause the comparator to mis-operate. To avoid problems, a small bypass capacitor, such as 0.1-µF ceramic, should be placed immediately adjacent to the supply pins. An additional 6.8 µF or greater tantalum capacitor should be placed at the point where the power supply for the comparator is introduced onto the board. These capacitors act as an energy reservoir and keep the supply impedance low. In a dual-supply application, a 0.1-µF capacitor is recommended to be placed across V^+ and V^- pins.
2. Keep all leads short to reduce stray capacitance and lead inductance. It will also minimize any unwanted coupling from any high-level signals (such as the output). The comparators can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs through stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Try to avoid a long loop which could act as an inductor (coil).
3. It is a good practice to use an unbroken ground plane on a printed-circuit-board to provide all components with a low inductive ground connection. Make sure ground paths are low-impedance where heavier currents are flowing to avoid ground level shift. Preferably there should be a ground plane under the component.
4. The output trace should be routed away from inputs. The ground plane should extend between the output and inputs to act as a guard. This can be achieved by running a topside ground plane between the output and inputs. A typical PCB layout is shown in Figure 43.
5. When the signal source is applied through a resistive network to one input of the comparator, it is usually advantageous to connect the other input with a resistor with the same value, for both DC and AC consideration. Input traces should be laid out symmetrically if possible.
6. All pins of any unused comparators should be tied to the negative supply.

10.1.2 DSBGA Light Sensitivity

Exposing the DSBGA device to direct sunlight will cause mis-operation of the device. Light sources such as Halogen lamps can also affect electrical performance if brought near to the device. The wavelengths, which have the most detrimental effect, are reds and infrareds. Be aware of internal light sources, such as keyboard or display backlights, that may pass through a PCB. A copper plane should be placed on a lower layer under the DSBGA to block light. Be careful using vias under the device, as they may pass light.

Layout Guidelines (continued)

10.1.3 DSBGA Mounting

The DSBGA package requires specific mounting techniques, which are detailed in Application Note AN-1112 (SNVA009).

10.1.4 LMV7272 DSBGA to DIP Conversion Board

To facilitate characterization and testing, a DSBGA to DIP conversion board, LMV7272TLCONV, is available. It is a 2-layer board, with the LMV7272 mounted on the bottom layer, and a capacitor (C1, between the positive and negative supplies) added to the top layer.

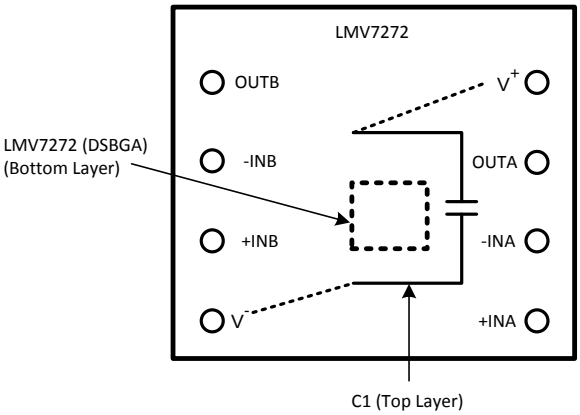


Figure 42. LMV7272TLCONV Diagram

10.2 Layout Example

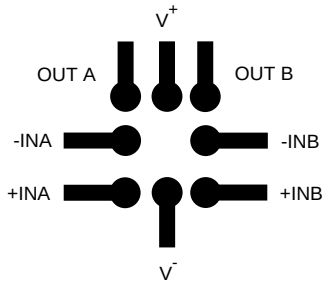


Figure 43. Typical PCB Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

For developmental support, see the following:

- LMV7271 PSPICE Model (can also be used for LMV7272), SNOM052
- LMV7275 PSPICE Model, SNOM555
- TINA-TI SPICE-Based Analog Simulation Program, http://www.ti.com/tool/tina-ti
- DIP Adapter Evaluation Module, http://www.ti.com/tool/dip-adapter-evm
- TI Universal Operational Amplifier Evaluation Module, http://www.ti.com/tool/opampevm

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- AN-74 *A Quad of Independently Functioning Comparators*, SNOA654
- AN-1112 *Micro SMD Wafer Level Chip Scale Package*, SNVA009

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMV7271	Click here	Click here	Click here	Click here	Click here
LMV7272	Click here	Click here	Click here	Click here	Click here
LMV7275	Click here	Click here	Click here	Click here	Click here

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV7271MF	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	C25A	
LMV7271MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C25A	Samples
LMV7271MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C25A	Samples
LMV7271MG	NRND	SC70	DCK	5	1000	TBD	Call TI	Call TI	-40 to 85	C34	
LMV7271MG/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C34	Samples
LMV7271MGX/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C34	Samples
LMV7272TL/NOPB	ACTIVE	DSBGA	YZR	8	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C 01	Samples
LMV7272TLX/NOPB	ACTIVE	DSBGA	YZR	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C 01	Samples
LMV7275MF	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	C26A	
LMV7275MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C26A	Samples
LMV7275MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C26A	Samples
LMV7275MG	NRND	SC70	DCK	5	1000	TBD	Call TI	Call TI	-40 to 85	C35	
LMV7275MG/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C35	Samples
LMV7275MGX/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C35	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

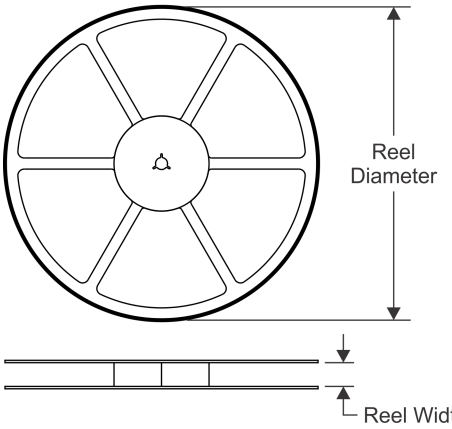
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

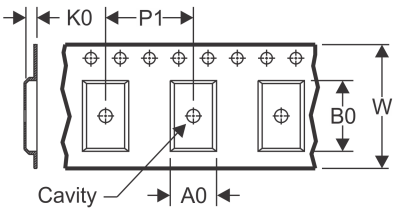
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

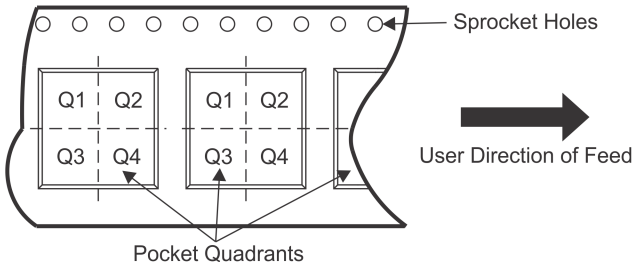


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

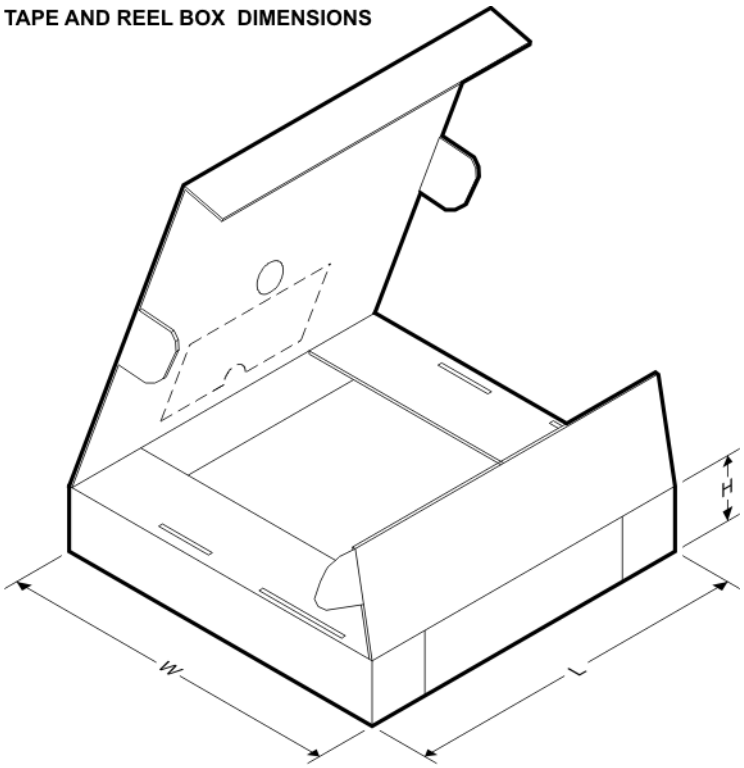
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV7271MF	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7271MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7271MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7271MG	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7271MG/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7271MGX/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7272TL/NOPB	DSBGA	YZR	8	250	178.0	8.4	1.7	1.7	0.76	4.0	8.0	Q1
LMV7272TLX/NOPB	DSBGA	YZR	8	3000	178.0	8.4	1.7	1.7	0.76	4.0	8.0	Q1
LMV7275MF	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7275MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7275MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7275MG	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7275MG/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7275MGX/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

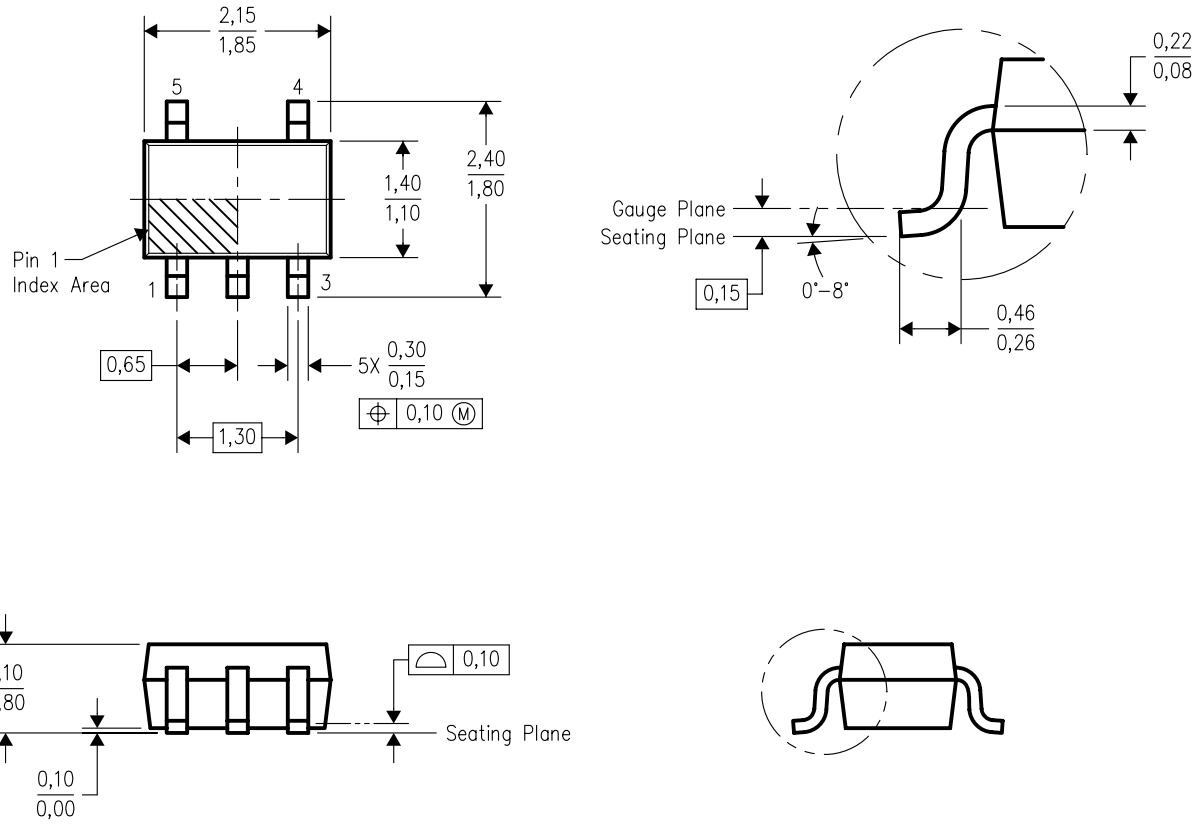
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV7271MF	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV7271MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV7271MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV7271MG	SC70	DCK	5	1000	210.0	185.0	35.0
LMV7271MG/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LMV7271MGX/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0
LMV7272TL/NOPB	DSBGA	YZR	8	250	210.0	185.0	35.0
LMV7272TLX/NOPB	DSBGA	YZR	8	3000	210.0	185.0	35.0
LMV7275MF	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV7275MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV7275MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV7275MG	SC70	DCK	5	1000	210.0	185.0	35.0
LMV7275MG/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LMV7275MGX/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0

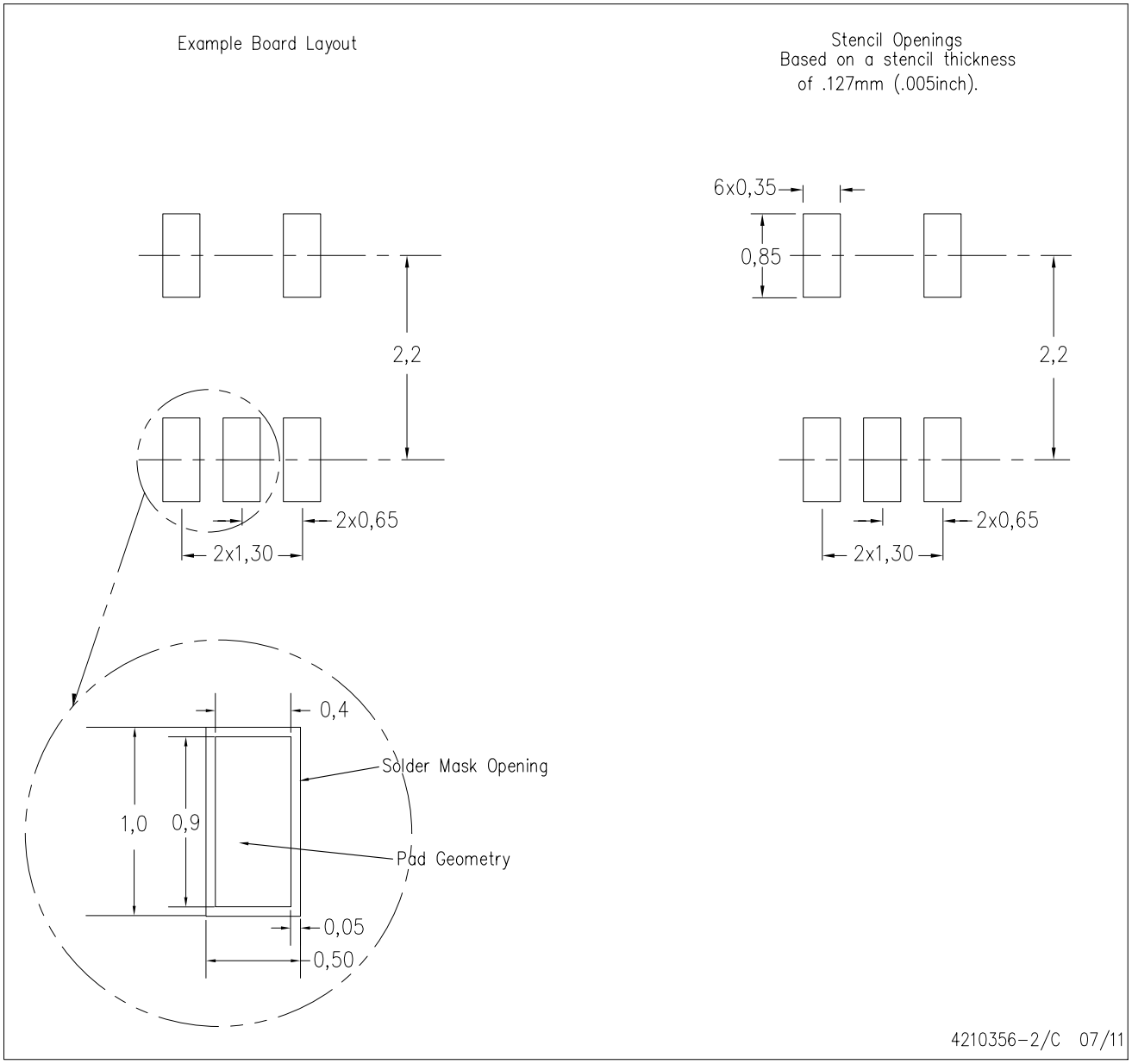
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

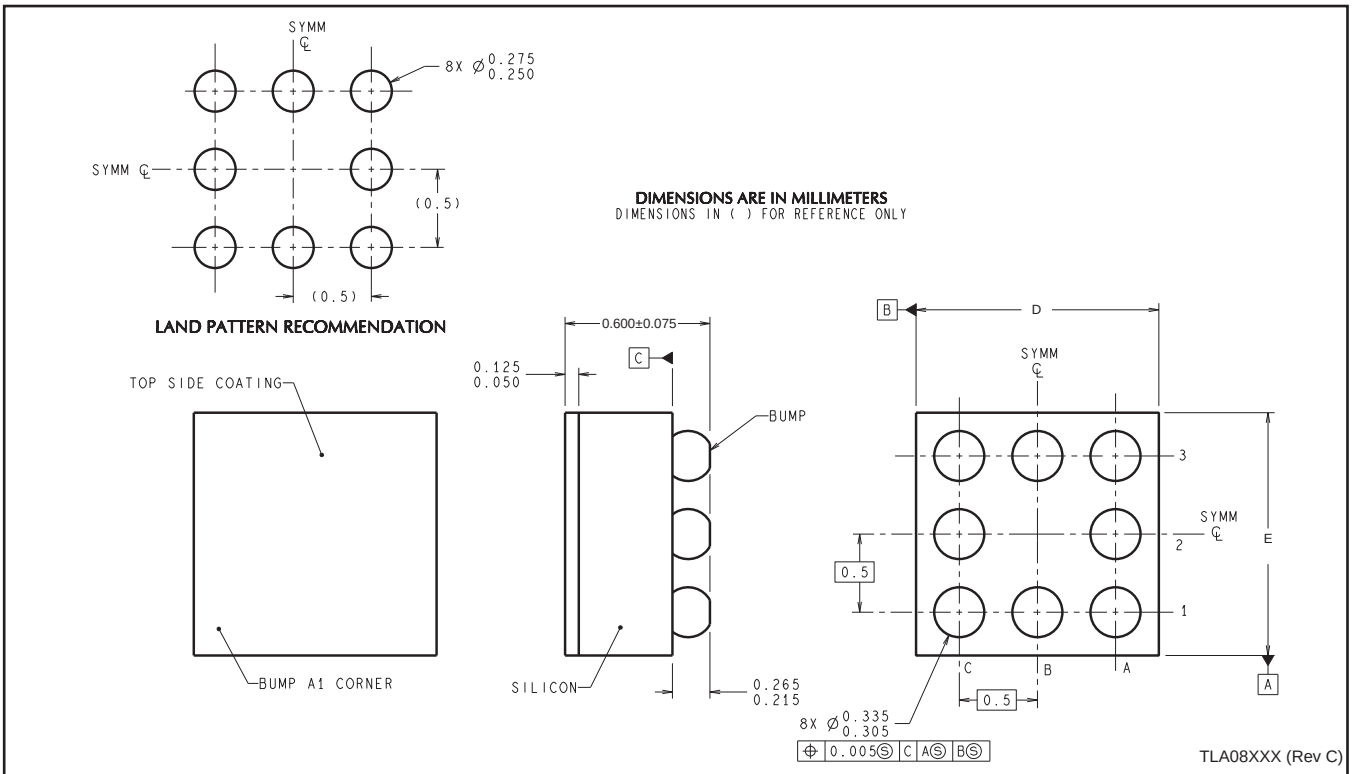
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

YZR0008



D: Max = 1.55 mm, Min = 1.489 mm

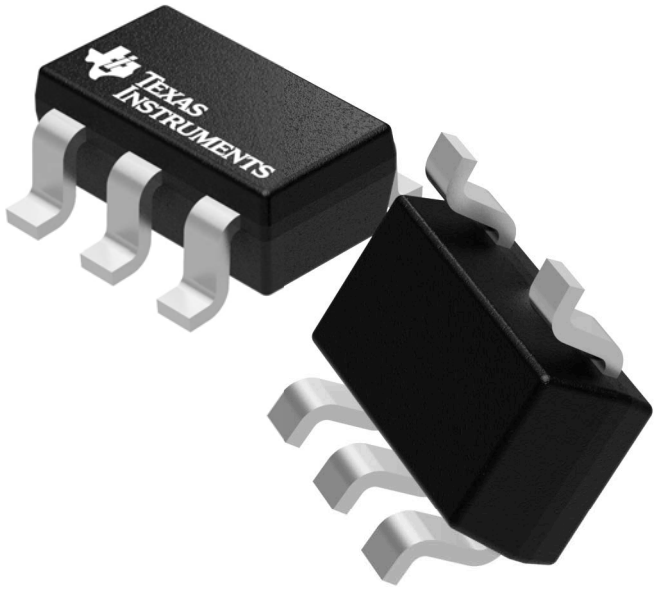
E: Max = 1.55 mm, Min = 1.489 mm

4215045/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

DBV 5 SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



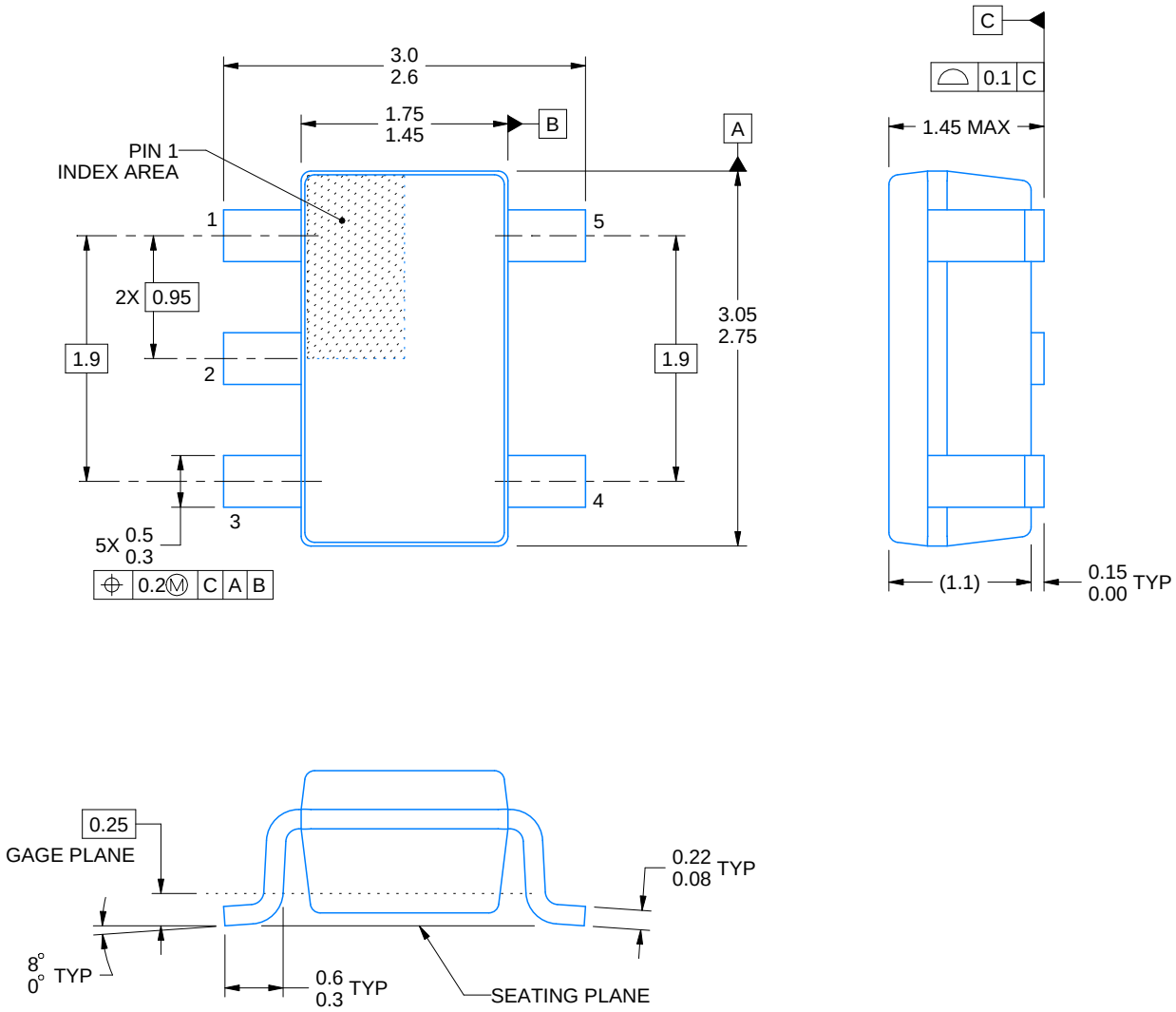
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

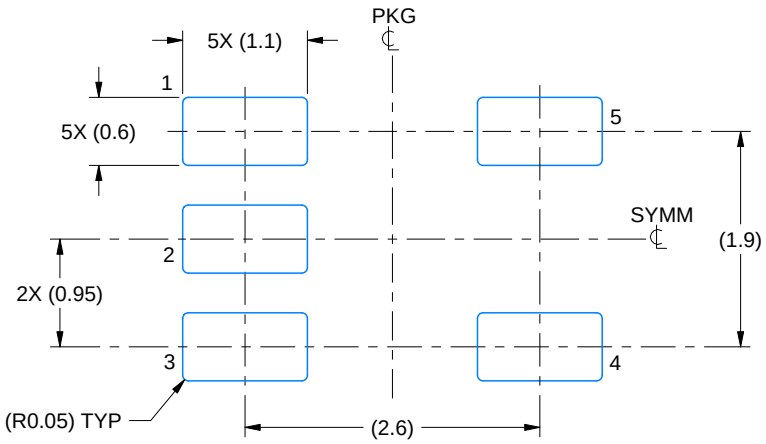
SMALL OUTLINE TRANSISTOR



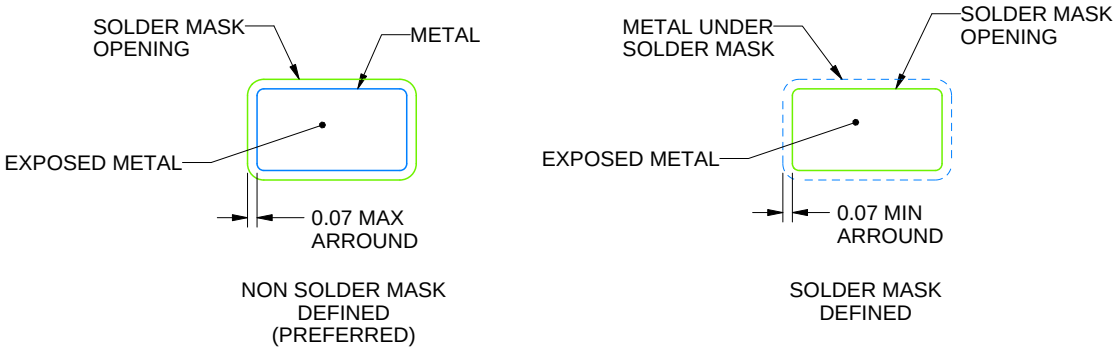
4214839/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

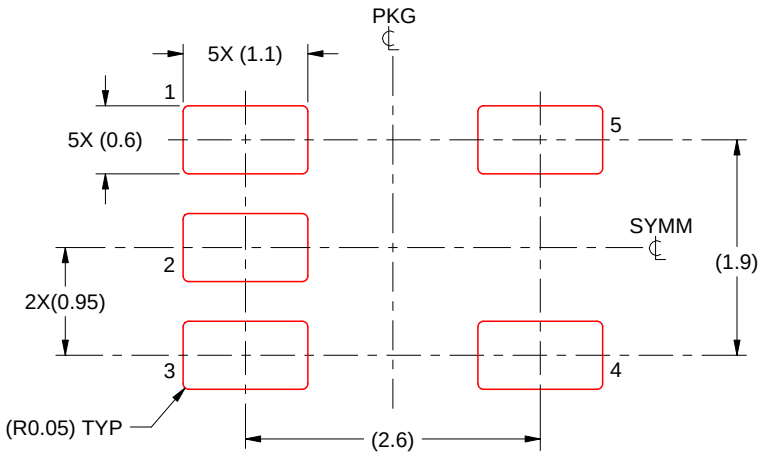


SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

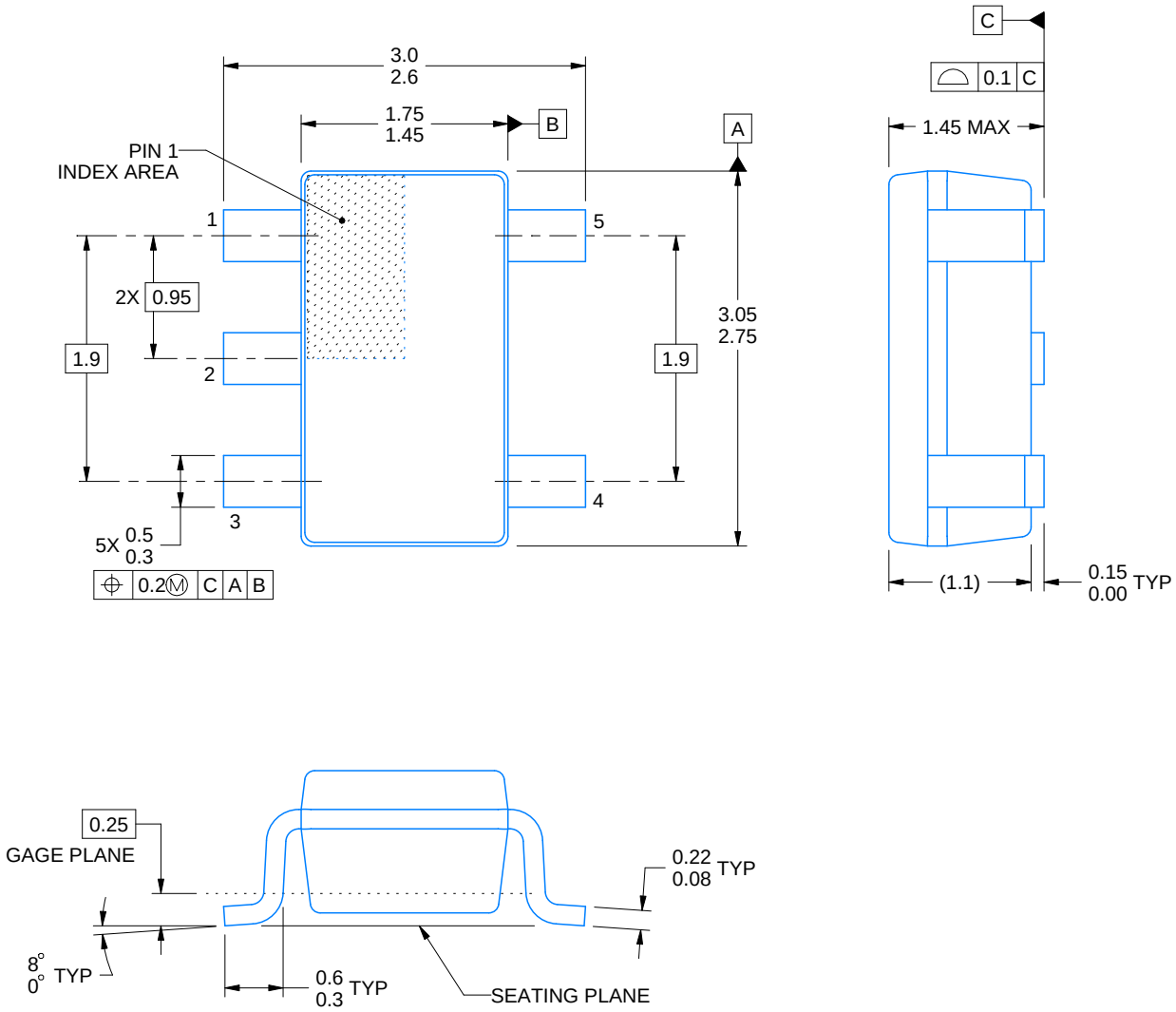
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

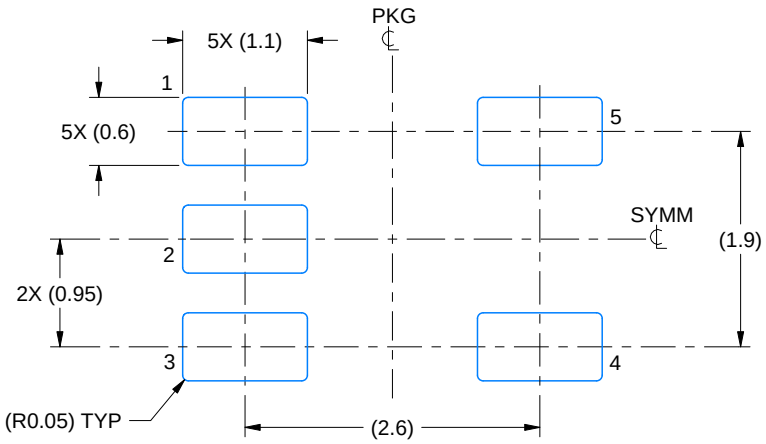
SMALL OUTLINE TRANSISTOR



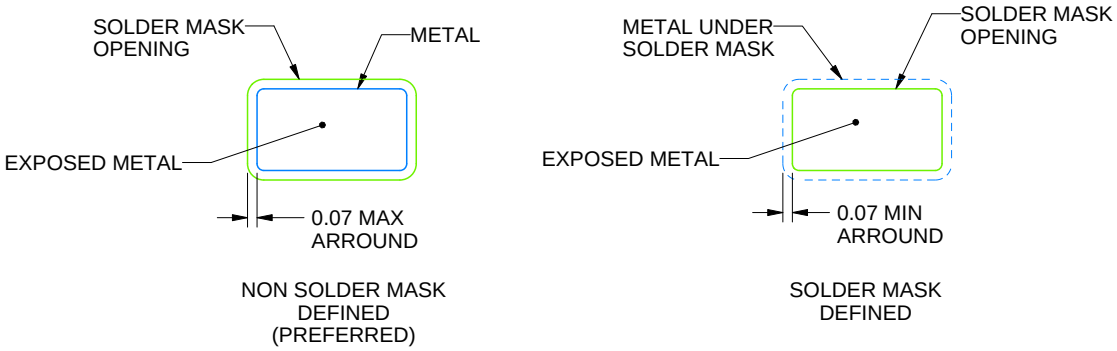
4214839/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

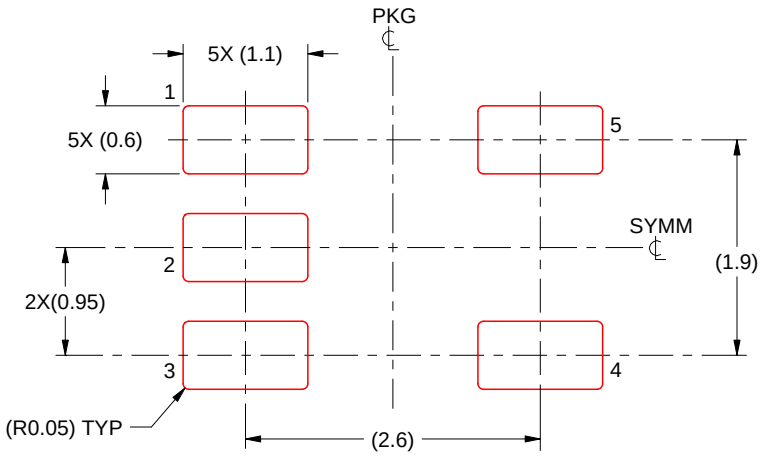


SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

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