TEXAS INSTRUMENTS

TPS74901

SBVS082I – JUNE 2007 – REVISED MAY 2016

TPS74901 3-A Low Dropout Linear Regulator With Programmable Soft-Start

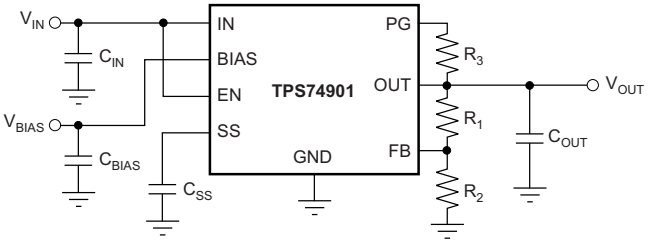
1 Features

- V_{OUT} Range: 0.8 V to 3.6 V
- Ultralow V_{IN} Range: 0.8 V to 5.5 V
- V_{BIAS} Range: 2.7 V to 5.5 V
- Low Dropout: 120 mV (Typical) at 3 A
- Power-Good (PG) Output Allows Supply Monitoring or Provides a Sequencing Signal for Other Supplies
- 2% Accuracy Over Line, Load, and Temperature
- Adjustable Start-Up In-Rush Control
- V_{BIAS} Permits Low V_{IN} Operation With Good Transient Response
- Stable with Any Output Capacitor ≥ 2.2 µF
- Packages:
  - Small, 3-mm × 3-mm × 1-mm VSON
  - 5-mm × 5-mm × 1-mm VQFN and DDPAK-7
- Active High Enable

2 Applications

- FPGA Applications
- DSP Core and I/O Voltages
- Servers
- Post-Regulation Applications
- Applications with Special Start-Up Time or Sequencing Requirements

Typical Application Circuit (Adjustable)



3 Description

The TPS74901 low-dropout (LDO) linear regulator provides an easy-to-use, robust power management solution for a wide variety of applications. User-programmable soft-start minimizes stress on the input power source by reducing capacitive inrush current during start-up. The soft-start is monotonic and well-suited for powering many different types of processors and ASICs. The enable input and power-good output allow easy sequencing with external regulators. This complete flexibility permits the user to configure a solution that meets the sequencing requirements of FPGAs, DSPs, and other applications with special start-up requirements.

A precision reference and error amplifier deliver 2% accuracy over load, line, temperature, and process. The device is stable with any type of capacitor ≥ 2.2 µF, and the device is fully specified from –40°C to 125°C. The TPS74901 is offered in a small (3 mm × 3 mm) VSON package and a small (5-mm × 5-mm) VQFN package, yielding a highly compact total solution size. The device is also available in a DDPAK-7 package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS74901	VQFN (20)	5.00 mm × 5.00 mm
	DDPAK/TO-263 (7)	8.89 mm × 10.10 mm
	VSON (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Turnon Response

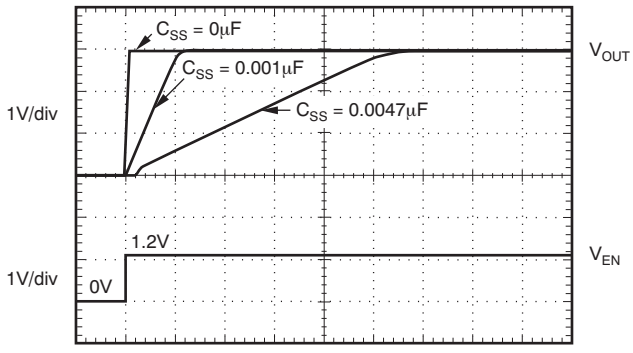


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (November 2015) to Revision I — **Page**

- Added DRC package to document ... 1
- Changed *Packages* Features bullet ... 1
- Added DRC package to *Description* section ... 1
- Added DRC (VSON) package to *Device Information* table ... 1
- Added DRC package to *Pin Configuration and Functions* section ... 3
- Added DRC package to *Thermal Information* table ... 5

Changes from Revision G (November 2010) to Revision H — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Deleted nonimal values from V_{IN}, V_{EN}, and V_{BIAS} rows ... 4
- Changed values in the *Thermal Information* table ... 5
- Changed values for VBIAS column on Normal mode, Dropout mode, and Disabled mode rows ... 13
- Changed $V_{IN(min)}$ to $V_{IN(UVLO)}$ under V_{IN} column in Disabled mode row ... 13

Changes from Revision F (August, 2010) to Revision G — **Page**

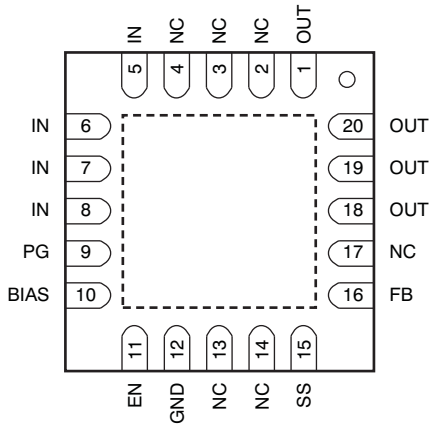
- Corrected equation for and updated values for Table 2 ... 16

Changes from Revision E (January, 2010) to Revision F — **Page**

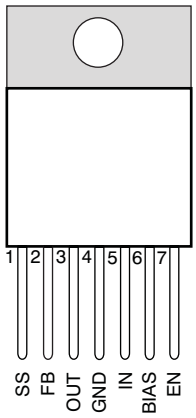
- Revised *Layout Recommendations and Power Dissipation* section ... 20
- Added *Estimating Junction Temperature* ... 21

5 Pin Configuration and Functions

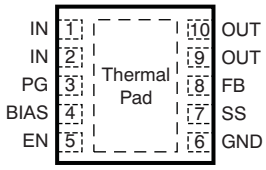
RGW Package
20-Pin VQFN
Top View



KTW Package
7-Pin DDPAK/TO-263
Top View



DRC Package
10-Pin VSON with Thermal Pad
Top View



Pin Functions

PIN				I/O	DESCRIPTION
NAME	DDPAK/TO-263	VQFN	VSON		
BIAS	6	10	4	I	Bias input voltage for error amplifier, reference, and internal control circuits.
EN	7	11	5	I	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode. This pin must not be left floating.
FB	2	16	8	I	This pin is the feedback connection to the center tap of an external resistor divider network that sets the output voltage. This pin must not be left floating.
GND	4	12	6	—	Ground
IN	5	5, 6, 7, 8	1, 2	I	Unregulated input to the device.
NC	—	2, 3, 4, 13, 14, 17	—	—	No connection. This pin can be left floating or connected to GND to allow better thermal contact to the top-side plane.
OUT	3	1, 18, 19, 20	9, 10	O	Regulated output voltage. A small capacitor (total typical capacitance ≥ 2.2 µF, ceramic) is needed from this pin to ground to assure stability.
PG	—	9	3	O	Power-Good (PG) is an open-drain, active-high output that indicates the status of V_{OUT}. When V_{OUT} exceeds the PG trip threshold, the PG pin goes into a high-impedance state. When V_{OUT} is below this threshold the pin is driven to a low-impedance state. A pullup resistor from 10 kΩ to 1 MΩ must be connected from this pin to a supply up to 5.5 V. The supply can be higher than the input voltage. Alternatively, the PG pin can be left floating if output monitoring is not necessary.
SS	1	15	7	—	Soft-Start pin. A capacitor connected on this pin to ground sets the start-up time. If this pin is left floating, the regulator output soft-start ramp time is typically 100 µs.
Thermal Pad				—	Solder to the ground plane for increased thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

At T_J = –40°C to 125°C, unless otherwise noted. All voltages are with respect to GND.(1)

		MIN	MAX	UNIT
V_{IN}, V_{BIAS}	Input voltage	–0.3	6	V
V_{EN}	Enable voltage	–0.3	6	V
V_{PG}	Power-good voltage	–0.3	6	V
I_{PG}	PG sink current	0	1.5	mA
V_{SS}	SS pin voltage	–0.3	6	V
V_{FB}	Feedback pin voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3	V_{IN} + 0.3	V
I_{OUT}	Maximum output current	Internally limited		
	Output short circuit duration	Indefinite		
P_{DISS}	Continuous total power dissipation	See *Thermal Information*		
T_J	Operating junction temperature	–40	125	°C
T_{stg}	Storage junction temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	V_{OUT} + V_{DO} (V_{IN})		5.5	V
V_{EN}	Enable supply voltage	0		5.5	V
V_{BIAS}(1)	BIAS supply voltage	V_{OUT} + V_{DO} (V_{BIAS})(2)		5.5	V
V_{OUT}	Output voltage	0.8		3.3	V
I_{OUT}	Output current	0		3	A
C_{OUT}	Output capacitor	2.2			µF
C_{IN}	Input capacitor(3)	1			µF
C_{BIAS}	Bias capacitor	0.1	1		µF
T_J	Operating junction temperature	–40		125	°C

(1) BIAS supply is required when V_{IN} is below V_{OUT} + 1.62 V.
(2) V_{BIAS} has a minimum voltage of 2.7 V or V_{OUT} + V_{DO} (V_{BIAS}), whichever is higher.
(3) If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for the supply is 4.7 µF.

6.4 Thermal Information

THERMAL METRIC[1]		TPS74901			UNIT
		RGW (VQFN)	KTW (TO-263)	DRC (VSON)	
		20 PINS	7 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.1	33.8	48.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.3	35.9	60.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.5	25	22.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	6	1.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	17.6	23.6	22.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.2	N/A	4.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

At T_J = –40°C to 125°C, V_{EN} = 1.1 V, V_{IN} = V_{OUT} + 0.3 V, C_{BIAS} = 0.1 µF, C_{IN} = C_{OUT} = 10 µF, C_{NR} = 1 nF, I_{OUT} = 50 mA, and V_{BIAS} = 5 V, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		V_{OUT} + V_{DO}		5.5	V
V_{BIAS}	Bias pin voltage		2.7		5.5	V
V_{REF}	Internal reference (Adj.)	T_J = 25°C	0.798	0.802	0.806	V
V_{OUT}	Output voltage	V_{IN} = 5 V, I_{OUT} = 3 V	V_{REF}		3.6	V
	Accuracy (RGW package)(1)	V_{OUT} + 2.2 V ≤ V_{BIAS} ≤ 5.5 V, 50 mA ≤ I_{OUT} ≤ 3 A	–2%	±0.5%	2%	
	Accuracy (KTW package)(1)	V_{OUT} + 2.4 V ≤ V_{BIAS} ≤ 5.5 V, 50 mA ≤ I_{OUT} ≤ 3 A	–2%	±0.5%	2%	
V_{OUT}/V_{IN}	Line regulation	$V_{OUT\ (NOM)}$ + 0.3 ≤ V_{IN} ≤ 5.5 V		0.03		%/V
V_{OUT}/I_{OUT}	Load regulation	50 mA ≤ I_{OUT} ≤ 3 A		0.09		%/A
V_{DO}	V_{IN} dropout voltage(2)	I_{OUT} = 3 A, V_{BIAS} – $V_{OUT\ (NOM)}$ ≥ 3.25 V(3)		120	280	mV
	V_{BIAS} dropout voltage(2)	I_{OUT} = 3 A, V_{IN} = V_{BIAS}		1.31	1.75	V
I_{CL}	Current limit	V_{OUT} = 80% × $V_{OUT\ (NOM)}$, RGW Package	3.9	4.6	5.5	A
		V_{OUT} = 80% × $V_{OUT\ (NOM)}$, KTW Package	3.8	4.6	5.5	
I_{BIAS}	Bias pin current			1	2	mA
I_{SHDN}	Shutdown supply current (I_{GND})	V_{EN} ≤ 0.4 V		1	50	µA
I_{FB}	Feedback pin current		–1	0.150	1	µA
PSRR	Power-supply rejection (V_{IN} to V_{OUT})	1 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		60		dB
		300 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		30		
	Power-supply rejection (V_{BIAS} to V_{OUT})	1 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		50		dB
		300 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		30		
Noise	Output noise voltage	100 Hz to 100 kHz, I_{OUT} = 3 A, C_{SS} = 0.001 µF		25 × V_{OUT}		μV_{RMS}
t_{STR}	Minimum start-up time	R_{LOAD} for I_{OUT} = 1 A, C_{SS} = open		200		µs
I_{SS}	Soft-start charging current	V_{SS} = 0.4 V		440		nA
$V_{EN,\ HI}$	Enable input high level		1.1		5.5	V
$V_{EN,\ LO}$	Enable input low level		0		0.4	V
$V_{EN,\ HYS}$	Enable pin hysteresis			50		mV
$V_{EN,\ DG}$	Enable pin deglitch time			20		µs
I_{EN}	Enable pin current	V_{EN} = 5 V		0.1	1	µA
V_{IT}	PG trip threshold	V_{OUT} decreasing	85	90	94	$\%V_{OUT}$
V_{HYS}	PG trip hysteresis			3		$\%V_{OUT}$
$V_{PG,\ LO}$	PG output low voltage	I_{PG} = 1 mA (sinking), V_{OUT} < V_{IT}			0.3	V
$I_{PG,\ LKG}$	PG leakage current	V_{PG} = 5.25 V, V_{OUT} > V_{IT}		0.1	1	µA
T_J	Operating junction temperature		–40		125	°C
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		165		°C
		Reset, temperature decreasing		140		

(1) Adjustable devices tested at 0.8 V; resistor tolerance is not considered.
(2) Dropout is defined as the voltage from V_{IN} to V_{OUT} when V_{OUT} is 3% below nominal.
(3) *3.25 V* is a test condition of this device and can be adjusted by referring to Figure 6.

6.6 Typical Characteristics: I_{OUT} = 50 mA

At T_J = 25°C, V_{IN} = $V_{OUT(TYP)}$ + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 50 mA, V_{EN} = V_{IN}, C_{IN} = 1 µF, C_{BIAS} = 4.7 µF, and C_{OUT} = 10 µF, unless otherwise noted.

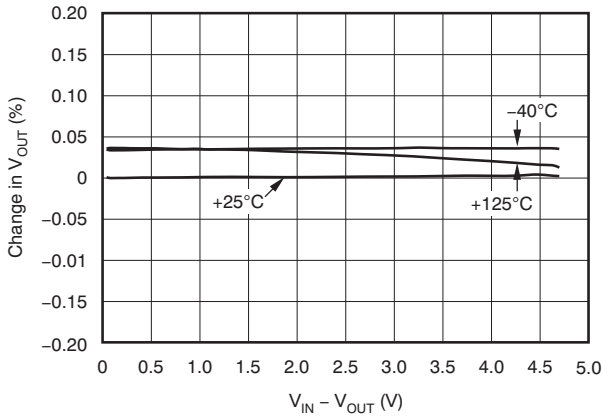


Figure 1. V_{IN} Line Regulation

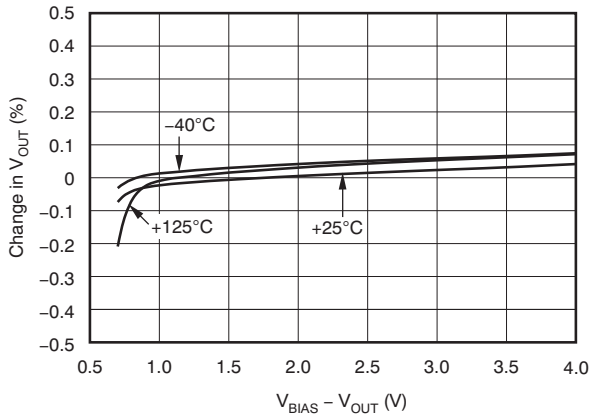


Figure 2. V_{BIAS} Line Regulation

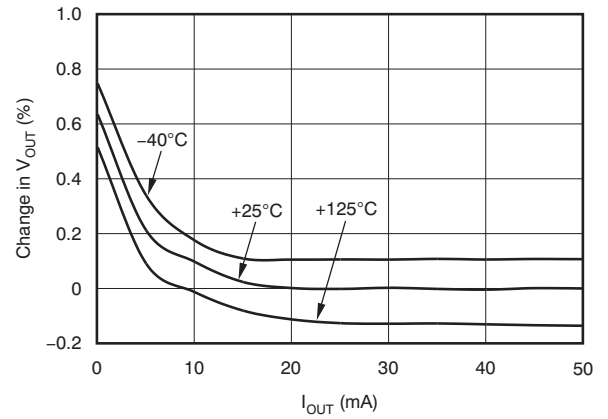


Figure 3. Load Regulation

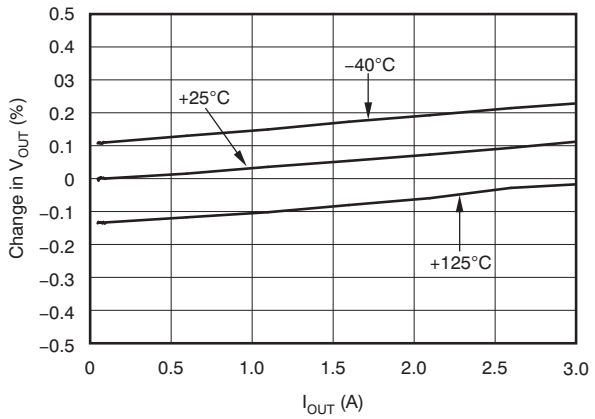


Figure 4. Load Regulation

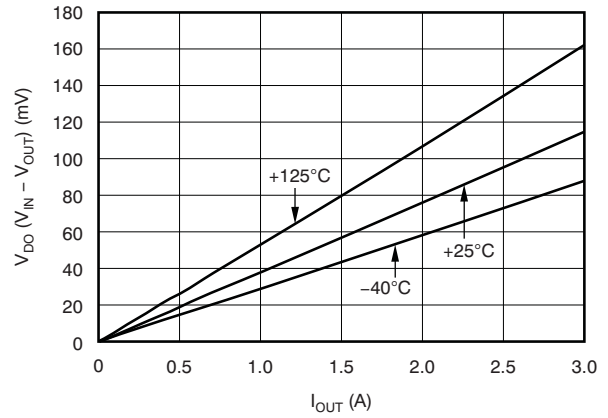


Figure 5. V_{IN} Dropout Voltage vs I_{OUT} and Temperature (T_J)

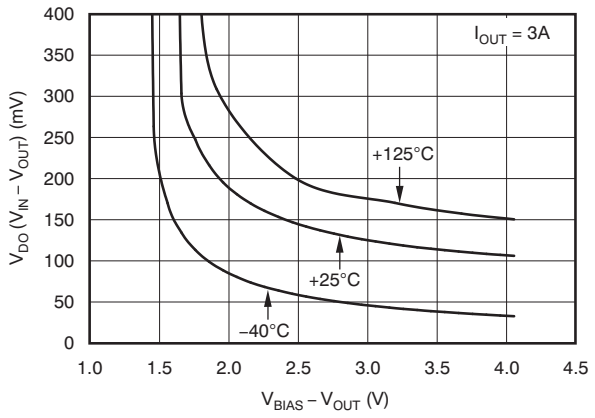


Figure 6. V_{IN} Dropout Voltage vs V_{IN} Dropout Voltage vs I_{OUT} and Temperature (T_J)

Typical Characteristics: I_{OUT} = 50 mA (continued)

At T_J = 25°C, V_{IN} = $V_{OUT(TYP)}$ + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 50 mA, V_{EN} = V_{IN}, C_{IN} = 1 µF, C_{BIAS} = 4.7 µF, and C_{OUT} = 10 µF, unless otherwise noted.

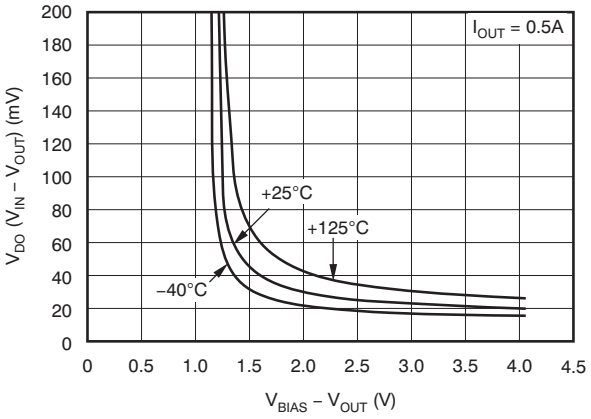


Figure 7. V_{IN} Dropout Voltage vs (V_{BIAS} – V_{OUT}) and Temperature (T_J)

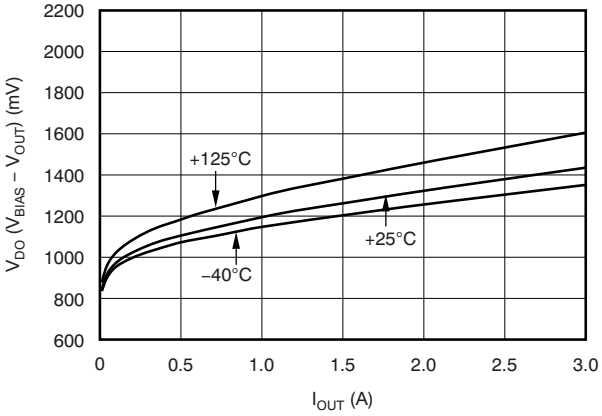


Figure 8. V_{BIAS} Dropout Voltage vs I_{OUT} and Temperature (T_J)

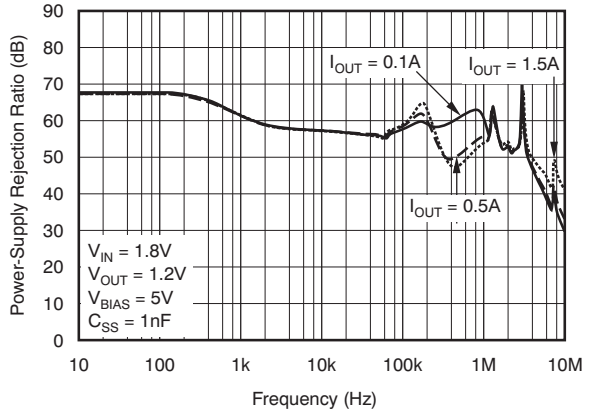


Figure 9. V_{BIAS} PSRR vs Frequency

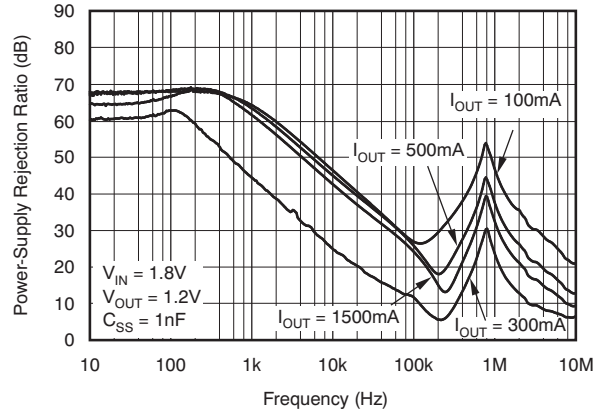


Figure 10. V_{IN} PSRR vs Frequency

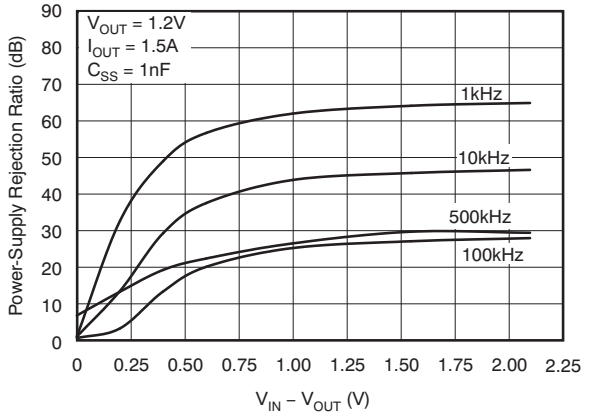


Figure 11. V_{IN} PSRR vs (V_{IN} – V_{OUT})

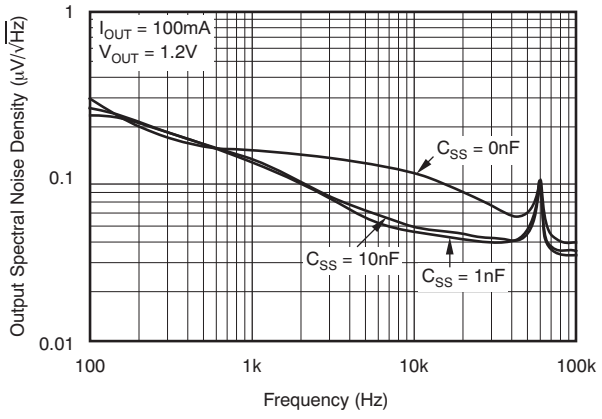


Figure 12. Noise Spectral Density

Typical Characteristics: I_{OUT} = 50 mA (continued)

At T_J = 25°C, V_{IN} = $V_{OUT(TYP)}$ + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 50 mA, V_{EN} = V_{IN}, C_{IN} = 1 µF, C_{BIAS} = 4.7 µF, and C_{OUT} = 10 µF, unless otherwise noted.

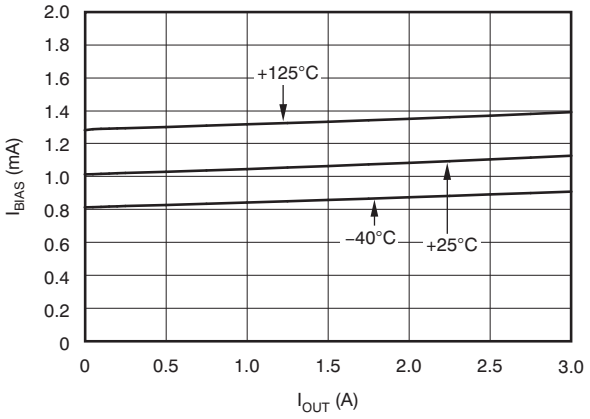


Figure 13. BIAS Pin Current vs I_{OUT} and Temperature (T_J)

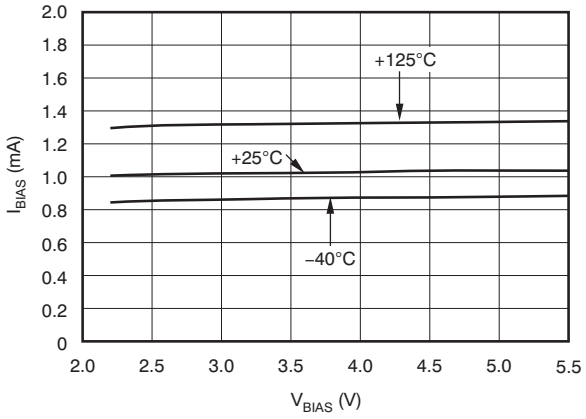


Figure 14. BIAS Pin Current vs V_{BIAS} and Temperature (T_J)

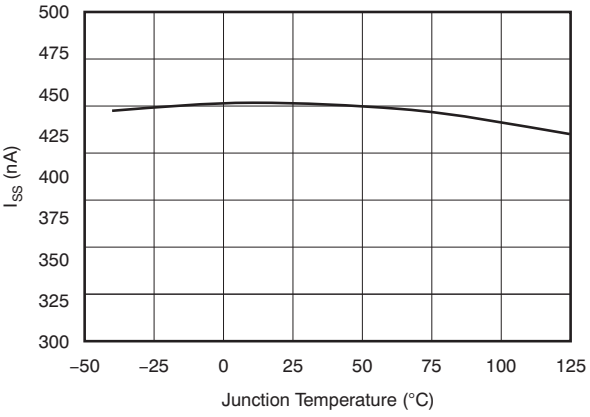


Figure 15. Soft-Start Charging Current (I_{SS}) vs Temperature (T_J)

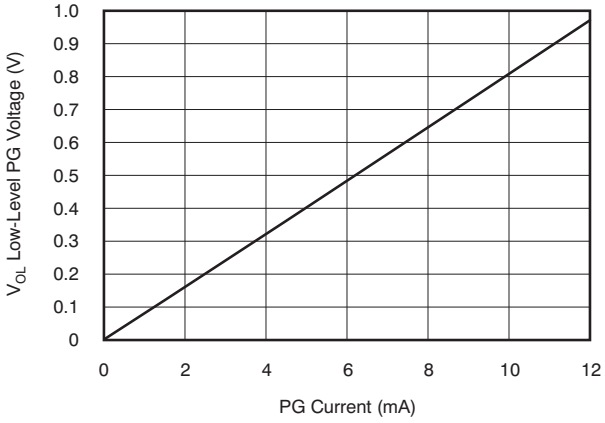


Figure 16. Low-Level PG Voltage vs Current

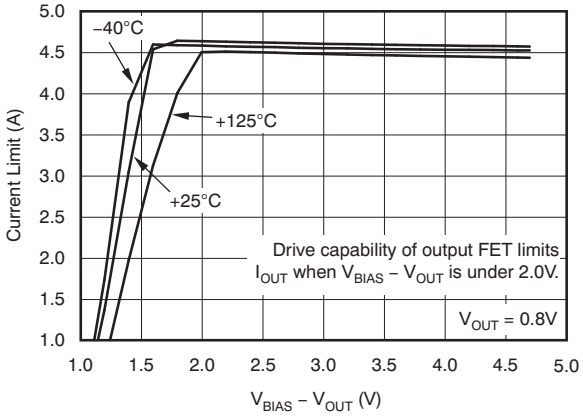


Figure 17. Current Limit vs (V_{BIAS} – V_{OUT})

6.7 Typical Characteristics: I_{OUT} = 1 A

At T_J = 25°C, V_{IN} = $V_{OUT(TYP)}$ + 0.3 V, V_{BIAS} = 5 V, I_{OUT} = 1 A, V_{EN} = V_{IN} = 1.8 V, V_{OUT} = 1.5 V, C_{IN} = 1 µF, C_{BIAS} = 4.7 µF, and C_{OUT} = 10 µF, unless otherwise noted.

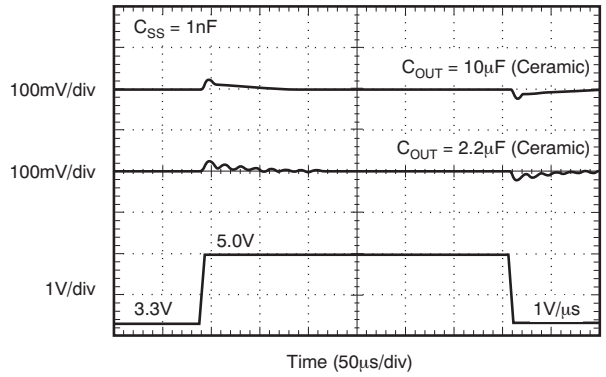


Figure 18. V_{BIAS} Line Transient

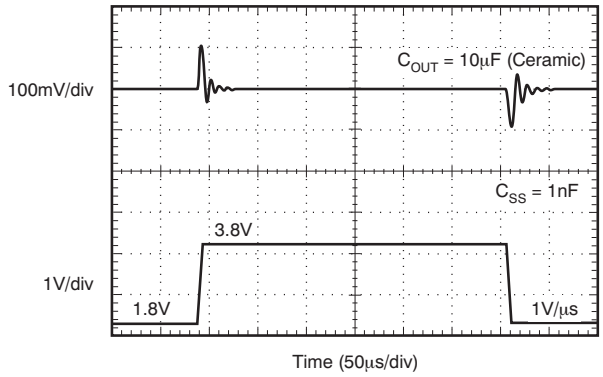


Figure 19. V_{IN} Line Transient

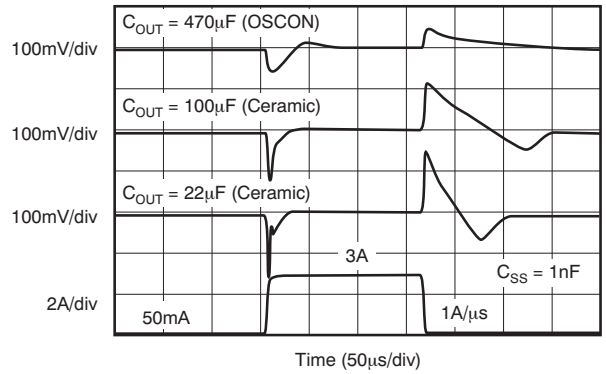


Figure 20. Output Load Transient Response

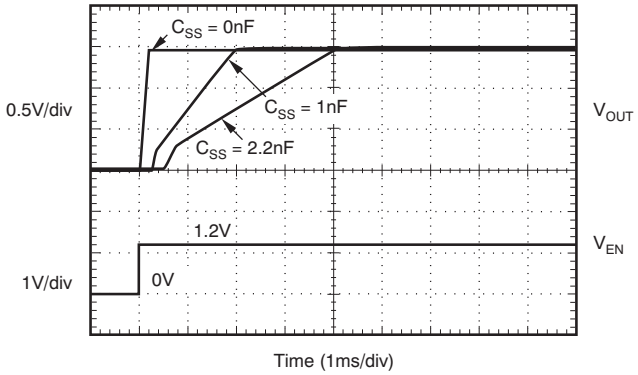


Figure 21. Turnon Response

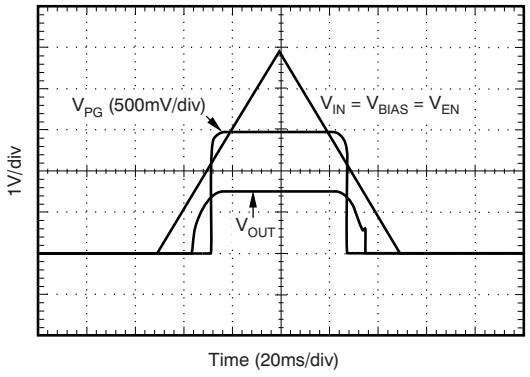


Figure 22. Power Up and Power Down

7 Detailed Description

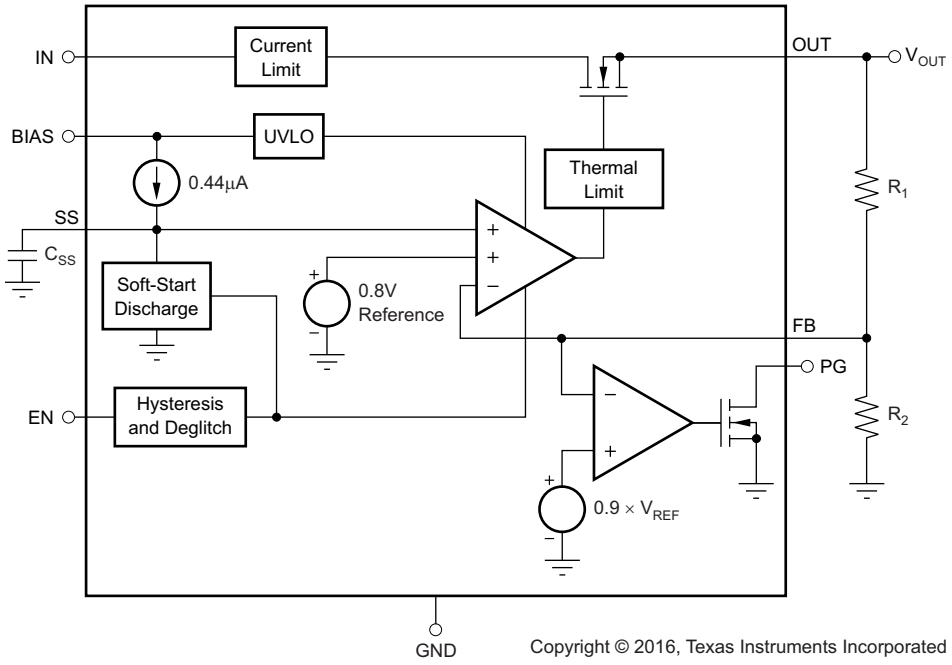
7.1 Overview

The TPS74901 belongs to a family of low-dropout regulators that feature soft-start capabilities. These regulators use a low-current bias input to power all internal control circuitry, allowing the NMOS pass transistor to regulate very-low input and output voltages.

The use of an NMOS-pass FET offers several critical advantages for many applications. Unlike a PMOS topology device, the output capacitor has little effect on loop stability. This architecture allows the TPS74901 to be stable with any capacitor with a value of 2.2 µF or greater. Transient response is also superior to PMOS topologies, particularly for low V_{IN} applications.

The TPS74901 features a programmable voltage-controlled soft-start circuit that provides a smooth, monotonic start-up and limits start-up inrush currents that may be caused by large capacitive loads. A power-good (PG) output is available to allow supply monitoring and sequencing of other supplies. An enable (EN) pin with hysteresis and deglitch allows slow-ramping signals to be used for sequencing the device. The low V_{IN} and V_{OUT} capability allows for inexpensive, easy-to-design, and efficient linear regulation between the multiple supply voltages often present in processor-intensive systems.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable and Shutdown

The enable (EN) pin is active high and is compatible with standard digital-signaling levels. V_{EN} below 0.4 V turns the regulator off and V_{EN} above 1.1 V turns the regulator on. Unlike many regulators, the enable circuitry has hysteresis and deglitching for use with relatively slowly ramping analog signals. This configuration allows the TPS74901 to be enabled by connecting the output of another supply to the EN pin. The enable circuitry typically has 50 mV of hysteresis and a deglitch circuit to help avoid ON-OFF cycling because of small glitches in the V_{EN} signal.

The enable threshold is typically 0.8 V and varies with temperature and process variations. Temperature variation is approximately –1 mV/°C; process variation accounts for most of the rest of the variation to the 0.4-V and 1.1-V limits. If precise turnon timing is required, a fast rise-time signal must be used to enable the TPS74901.

Feature Description (continued)

If not used, EN can be connected to either IN or BIAS. If EN is connected to IN, then connect EN as close as possible to the largest capacitance on the input to prevent voltage droops on that line from triggering the enable circuit.

7.3.2 Power-Good

The power-good (PG) pin is an open-drain output and can be connected to any 5.5 V or lower rail through an external pullup resistor. This pin requires at least 1.1 V on V_{BIAS} to have a valid output. The PG output is high-impedance when V_{OUT} is greater than $V_{IT} + V_{HYS}$. If V_{OUT} drops below V_{IT} or if V_{BIAS} drops below 1.9 V, the open-drain output turns on and pulls the PG output low. The PG pin also asserts when the device is disabled. The recommended operating condition of PG pin sink current is up to 1 mA, so the pullup resistor for PG must be in the range of 10 kΩ to 1 MΩ. PG is only provided on the VQFN package. If output voltage monitoring is not needed, the PG pin can be left floating.

7.3.3 Internal Current Limit

The TPS74901 features a factory-trimmed, accurate current limit that is flat over temperature and supply voltage. The current limit allows the device to supply surges of up to 4 A and maintain regulation. The current limit responds in about 10 µs to reduce the current during a short circuit fault.

The internal current limit protection circuitry of the TPS74901 is designed to protect against overload conditions. This circuitry is not intended to allow operation above the rated current of the device. Continuously running the TPS74901 above the rated current degrades device reliability.

7.3.4 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature the thermal protection circuit may cycle ON and OFF. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Activation of the thermal protection circuit indicates excessive power dissipation or inadequate heatsinking. For reliable operation, junction temperature must be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection must trigger at least 40°C above the maximum expected ambient condition of the application. This condition produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS74901 is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the TPS74901 into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage and bias voltage are both at least at the respective minimum specifications.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

Device Functional Modes (continued)

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The input or bias voltages are below the respective minimum specifications.
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

Table 1 lists the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER				
	V_{IN}	V_{EN}	V_{BIAS}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}(V_{IN})$	$V_{EN} > V_{EN(high)}$	$V_{BIAS} \geq V_{OUT} + V_{DO}(V_{BIAS})$	$I_{OUT} < I_{CL}$	$T_J < 125°C$
Dropout mode	$V_{IN} < V_{OUT(nom)} + V_{DO}(V_{IN})$	$V_{EN} > V_{EN(high)}$	$V_{BIAS} < V_{OUT} + V_{DO}(V_{BIAS})$	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)		$V_{EN} < V_{EN(low)}$	$V_{BIAS} < V_{BIAS(UVLO)}$	—	$T_J > 165°C$

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Input, Output, and BIAS Capacitor Requirements

The device is designed to be stable for all available types of and values of output capacitors ≥ 2.2 µF. The device is also stable with multiple capacitors in parallel, which can be of any type or value.

The capacitance required on the IN and BIAS pin strongly depends on the input supply source impedance. To counteract any inductance in the input, the minimum recommended capacitor for V_{IN} and V_{BIAS} is 1 µF. If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for V_{BIAS} is 4.7 µF. Good quality, low-ESR capacitors must be used on the input; ceramic X5R and X7R capacitors are preferred. These capacitors must be placed as close as possible to the pins for optimum performance.

8.1.2 Transient Response

The TPS74901 is designed to have excellent transient response for most applications with a small amount of output capacitance. In some cases, the transient response may be limited by the transient response of the input supply. This limitation is especially true in applications where the difference between the input and output is less than 300 mV. In this case, adding additional input capacitance improves the transient response much more than just adding additional output capacitance would do. With a solid input supply, adding additional output capacitance reduces undershoot and overshoot during a transient event; see Figure 20 in the *Typical Characteristics: I_{OUT} = 50 mA* section. Because the TPS74901 is stable with output capacitors as low as 2.2 µF, many applications may need very little capacitance at the LDO output. For these applications, local bypass capacitance for the powered device may be sufficient to meet the transient requirements of the application. This design reduces the total solution cost by avoiding the need to use expensive high-value capacitors at the LDO output.

8.1.3 Dropout Voltage

The TPS74901 offers very low dropout performance, making the device well-suited for high-current low V_{IN} and low V_{OUT} applications. The low dropout of the TPS74901 allows the device to be used in place of a DC-DC converter and still achieve good efficiencies. This provides designers with the power architecture for their applications to achieve the smallest, simplest, and lowest-cost solution.

There are two different specifications for dropout voltage with the TPS74901. The first specification (see Figure 23) is referred to as *V_{IN} Dropout* and is used when an external bias voltage is applied to achieve low dropout. This specification assumes that V_{BIAS} is at least 3.25 V above V_{OUT}, which is the case for V_{BIAS} when powered by a 5-V rail with 5% tolerance and with V_{OUT} = 1.5 V (*3.25 V* is a test condition of this device and can be adjusted by referring to Figure 6). If V_{BIAS} is higher than V_{OUT} + 3.25 V, V_{IN} dropout is less than specified.

Application Information (continued)

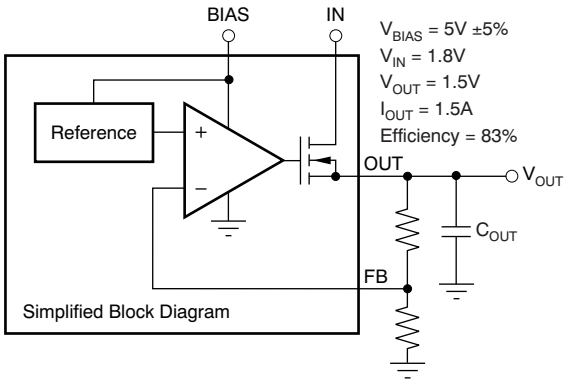


Figure 23. Typical Application of the TPS74901 Using an Auxiliary Bias Rail

The second specification (shown in Figure 24) is referred to as *V_{BIAS} Dropout* and applied to applications where IN and BIAS are tied together. This option allows the device to be used in applications where an auxiliary bias voltage is not available or low dropout is not required. Dropout is limited by BIAS in these applications because V_{BIAS} provides the gate drive to the pass FET; therefore, V_{BIAS} must be 1.75 V above V_{OUT}. Dropout is limited by BIAS in these applications because V_{BIAS} provides the gate drive to the pass FET; therefore, V_{BIAS} must be 1.75 V above V_{OUT}. Because of this usage, IN and BIAS tied together easily consume huge power. Pay attention not to exceed the power rating of the IC package.

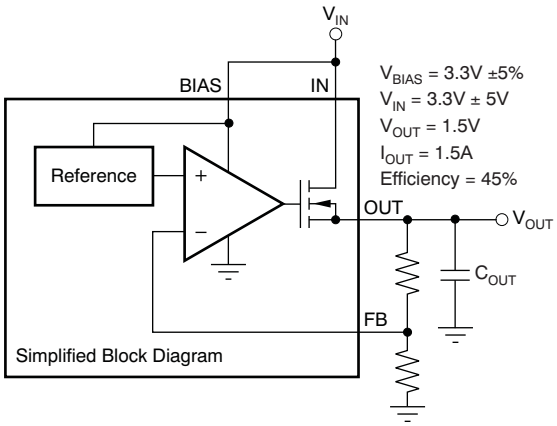


Figure 24. Typical Application of the TPS74901 Without an Auxiliary Bias

8.1.4 Output Noise

The TPS74901 provides low-output noise when a soft start capacitor is used. When the device reaches the end of the soft start cycle, the soft start capacitor serves as a filter for the internal reference. By using a 0.001-µF soft start capacitor, the output noise is reduced by half and is typically 30 μV_{RMS} for a 1.2-V output (10 Hz to 100 kHz). Further increasing C_{SS} has little effect on noise. Because most of the output noise is generated by the internal reference, the noise is a function of the set output voltage. The RMS noise with a 0.001-µF soft-start capacitor is given in Equation 1.

$$V_N(\mu V_{RMS}) = 25 \left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \quad (1)$$

The low-output noise of the TPS74901 makes the device a good choice for powering transceivers, PLLs, or other noise-sensitive circuitry.

Application Information (continued)

8.1.5 Programmable Soft Start

The TPS74901 features a programmable, monotonic, voltage-controlled soft start that is set with an external capacitor (C_{SS}). This feature is important for many applications because power-up initialization problems are eliminated when powering FPGAs, DSPs, or other processors. The controlled voltage ramp of the output also reduces peak inrush current during start-up, minimizing start-up transient events to the input power bus.

To achieve a linear and monotonic soft start, the TPS74901 error amplifier tracks the voltage ramp of the external soft start capacitor until the voltage exceeds the internal reference. The soft start ramp time is dependent on the soft start charging current (I_{SS}), soft start capacitance (C_{SS}), and the internal reference voltage (V_{REF}), and can be calculated using Equation 2.

$$t_{SS} = \frac{(V_{REF} \times C_{SS})}{I_{SS}} \quad (2)$$

If large output capacitors are used, the device current limit (I_{CL}) and the output capacitor may set the start-up time. In this case, the start-up time is given by Equation 3:

$$t_{SSCL} = \frac{(V_{OUT(NOM)} \times C_{OUT})}{I_{CL(MIN)}} \quad (3)$$

where

- $V_{OUT(NOM)}$ is the nominal set output voltage.
- C_{OUT} is the output capacitance.
- $I_{CL(MIN)}$ is the minimum current limit for the device.

In applications where monotonic start-up is required, the soft start time given by Equation 2 must be set to be greater than Equation 3.

The maximum recommended soft start capacitor is 0.015 µF. Larger soft start capacitors can be used and do not damage the device; however, the soft start capacitor discharge circuit may not be able to fully discharge the soft start capacitor when enabled. Soft start capacitors larger than 0.015 µF could be a problem in applications where the user must rapidly pulse the enable pin and still requires the device to soft start from ground. C_{SS} must be low-leakage; X7R, X5R, or C0G dielectric materials are preferred. See Table 2 for suggested soft-start capacitor values.

Table 2. Standard Capacitor Values for Programming the Soft-Start Time(1)

C_{SS}	SOFT START TIME
Open	0.1 ms
270 pF	0.5 ms
560 pF	1 ms
2.7 nF	5 ms
5.6 nF	10 ms
0.01 µF	18 ms

(1) $$t_{SS}(s) = \frac{V_{REF} \times C_{SS}}{I_{SS}} = \frac{0.8V \times C_{SS}(F)}{0.44\mu A}$$ where $t_{SS}(s)$ = soft-start time in seconds.

8.1.6 Sequencing Requirements

V_{IN}, V_{BIAS}, and V_{EN} can be sequenced in any order without causing damage to the device. However, for the soft-start function to work as intended, certain sequencing rules must be applied. Connecting EN to IN is acceptable for most applications as long as V_{IN} is greater than 1.1 V, and the ramp rate of V_{IN} and V_{BIAS} is faster than the set soft start ramp rate. If the ramp rate of the input sources is slower than the set soft start time, the output tracks the slower supply minus the dropout voltage until the set output voltage is reached. If EN is connected to BIAS, the device soft-starts as programmed, provided that V_{IN} is present before V_{BIAS}. If V_{BIAS} and V_{EN} are present before V_{IN} is applied and the set soft start time has expired, then V_{OUT} tracks V_{IN}. If the soft start time has not expired, the output tracks V_{IN} until V_{OUT} reaches the value set by the charging soft start capacitor. Figure 25 shows the use of an RC-delay circuit to hold off V_{EN} until V_{BIAS} has ramped. This technique can also be used to drive EN from V_{IN}. An external control signal can also be used to enable the device after V_{IN} and V_{BIAS} are present.

NOTE

When V_{BIAS} and V_{EN} are present and V_{IN} is not supplied, this device outputs approximately 50 µA of current from OUT. Although this condition will not cause any damage to the device, the output current may charge up the OUT node if total resistance between OUT and GND (including external feedback resistors) is greater than 10 kΩ.

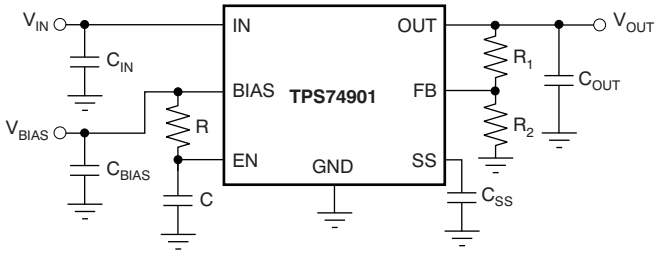


Figure 25. Soft-Start Delay Using an RC Circuit on Enable

8.2 Typical Application

Figure 26 illustrates the typical application circuit for the TPS74901 adjustable output device.

R_1 and R_2 can be calculated for any output voltage using the formula shown in Figure 26. See Table 3 for sample resistor values of common output voltages. To achieve the maximum accuracy specifications, R_2 must be ≤ 4.99 kΩ.

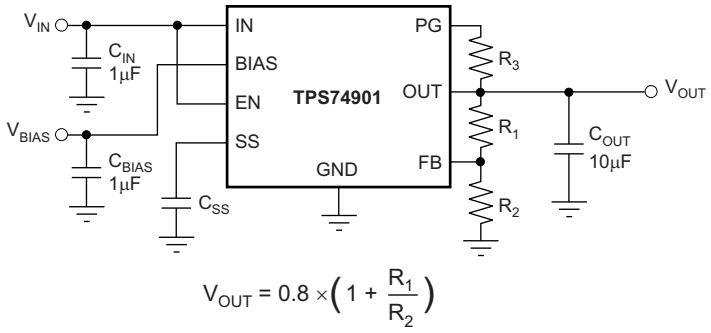


Figure 26. Typical Application Circuit for the TPS74901 (Adjustable)

Table 3. Standard 1% Resistor Values for Programming the Output Voltage(1)

R_1 (kΩ)	R_2 (kΩ)	V_{OUT} (V)
Short	Open	0.8
0.619	4.99	0.9
1.13	4.53	1
1.37	4.42	1.05
1.87	4.99	1.1
2.49	4.99	1.2
4.12	4.75	1.5
3.57	2.87	1.8
3.57	1.69	2.5
3.57	1.15	3.3

(1) $V_{OUT} = 0.8 \times (1 + R_1 / R_2)$

8.2.1 Design Requirements

The goal of this design is to create a 1.2-V rail at 3 A with minimal external components from a 1.5-V rail.

8.2.2 Detailed Design Procedure

First choose the bias, which must be at least 1.75-V above the output voltage. A 3.3-V rail is used to achieve this minimum voltage. For a minimal external component count and size, select the minimum capacitor sizes. C_{IN} = 1 µF, C_{BIAS} = 1 µF, and a C_{OUT} = 10 µF. The C_{OUT} value was chosen to improve transient response. Using Table 3, R1 is set to 2.49 kΩ and R2 is set to 4.99 kΩ to create a 1.2-V rail. The pullup resistor for PG is set to 10 kΩ.

8.2.3 Application Curves

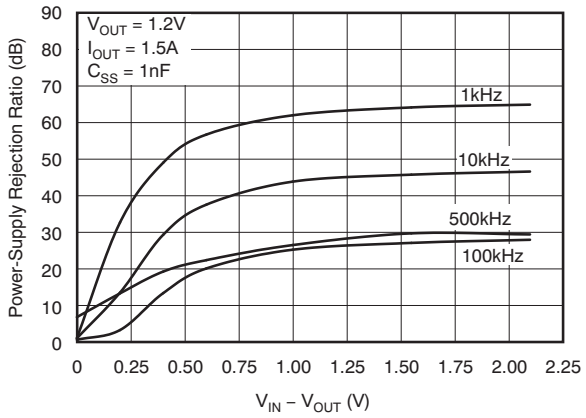


Figure 27. V_{IN} PSRR vs (V_{IN} – V_{OUT})

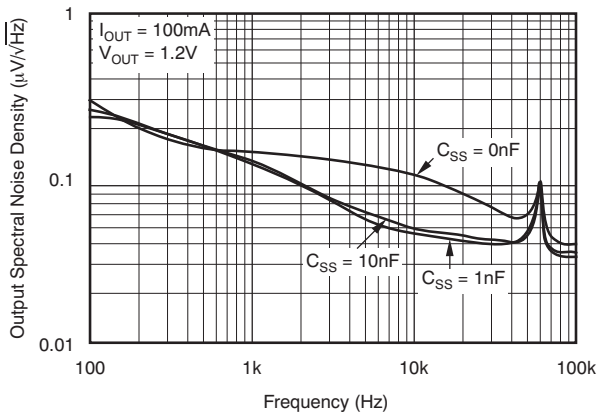


Figure 28. Noise Spectral Density

9 Power Supply Recommendations

The TPS74901 is designed to operate from an input voltage from 1.1 V to 5.5 V, provided the bias rail is at least 1.75-V higher than the input supply. The bias rail and the input supply must both provide adequate headroom and current for the device to operate normally.

Connect a low-output impedance power supply directly to the IN pin of the TPS74901. This supply must have at least 1 µF of capacitance near the IN pin for stability. A supply with similar requirements must also be connected directly to the bias rail with a separate 1-µF or larger capacitor.

If the IN pin is tied to the bias pin, a minimum 4.7 µF of capacitance is needed for stability.

To increase the overall PSRR of the solution at higher frequencies, use a PI-filter or ferrite bead before the input capacitor.

10 Layout

10.1 Layout Guidelines

An optimal layout can greatly improve transient performance, PSRR, and noise. To minimize the voltage droop on the input of the device during load transients, connect the capacitance on IN and BIAS as close as possible to the device. This capacitance also minimizes the effects of parasitic inductance and resistance of the input source and can therefore improve stability. To achieve optimal transient performance and accuracy, connect the top side of R_1 in Figure 26 as close as possible to the load. If BIAS is connected to IN, TI recommends connecting BIAS as close to the sense point of the input supply as possible. This connection minimizes the voltage droop on BIAS during transient conditions and can improve the turnon response.

10.2 Layout Example

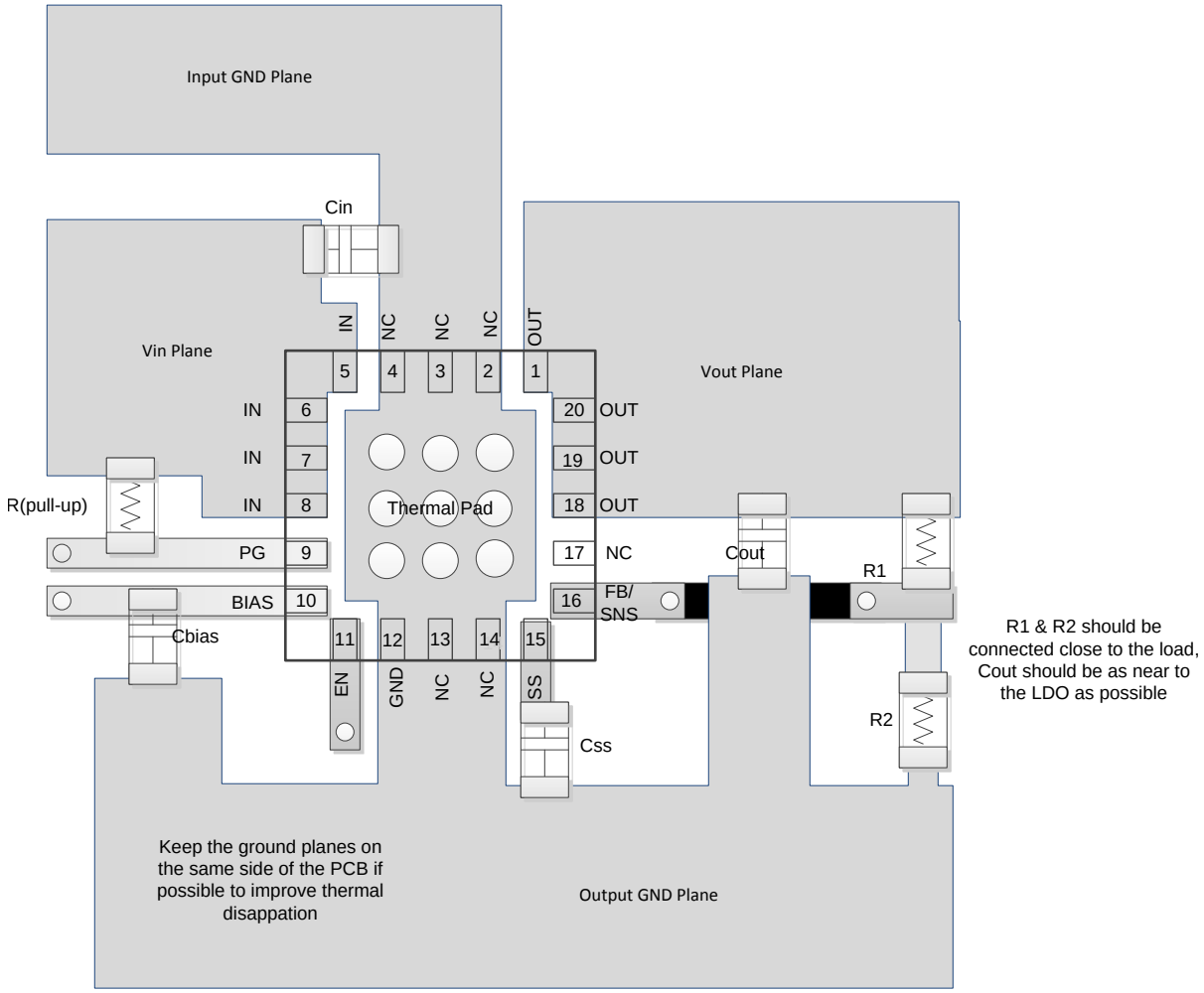


Figure 29. Layout Schematic (RGW Package)

10.3 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the tab or pad is critical to avoiding thermal shutdown and ensuring reliable operation.

Power dissipation of the device depends on input voltage and load conditions, and can be calculated using Equation 4:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (4)$$

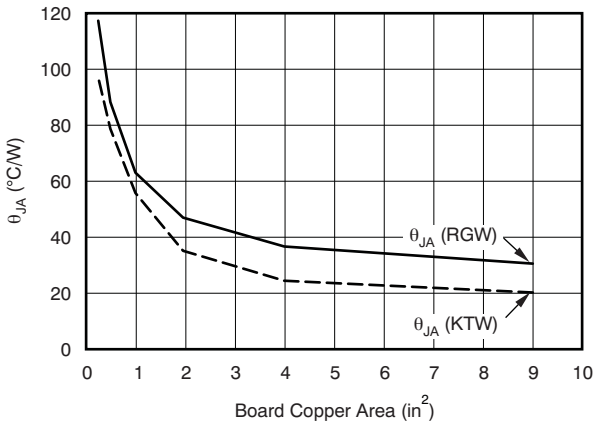
Power Dissipation (continued)

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On the VQFN (RGW) package, the primary conduction path for heat is through the exposed pad to the PCB. The pad can be connected to ground or left floating; however, the pad must be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. On the DDPAK (KTW) package, the primary conduction path for heat is through the tab to the PCB. Connect that tab to ground. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be estimated using Equation 5:

$$R_{\theta JA} = \frac{(+125°C - T_A)}{P_D} \quad (5)$$

Knowing the maximum $R_{\theta JA}$, the minimum amount of PCB copper area needed for appropriate heatsinking can be estimated using Figure 30.



Note: θ_{JA} value at board size of 9 in^2 (that is, 3 inches × 3 innches) is a JEDEC standard.

Figure 30. θ_{JA} versus Board Size

Figure 30 shows the variation of θ_{JA} as a function of ground plane copper area in the board. Figure 30 is intended only as a guideline to demonstrate the affects of heat spreading in the ground plane; do not use Figure 30 to estimate actual thermal performance in real application environments.

NOTE

When the device is mounted on an application PCB, TI strongly recommends using Ψ_{JT} and Ψ_{JB}, as explained in the section.

10.4 Thermal Considerations

A better method of estimating the thermal measure comes from using the thermal metrics Ψ_{JT} and Ψ_{JB}, as shown in Equation 6. These metrics are a more accurate representation of the heat transfer characteristics of the die and the package than $R_{\theta JA}$. The junction temperature can be estimated with the corresponding formulas given in Equation 6.

Ψ_{JT}: $T_J = T_T + \Psi_{JT} \bullet P_D$

Ψ_{JB}: $T_J = T_B + \Psi_{JB} \bullet P_D$

where

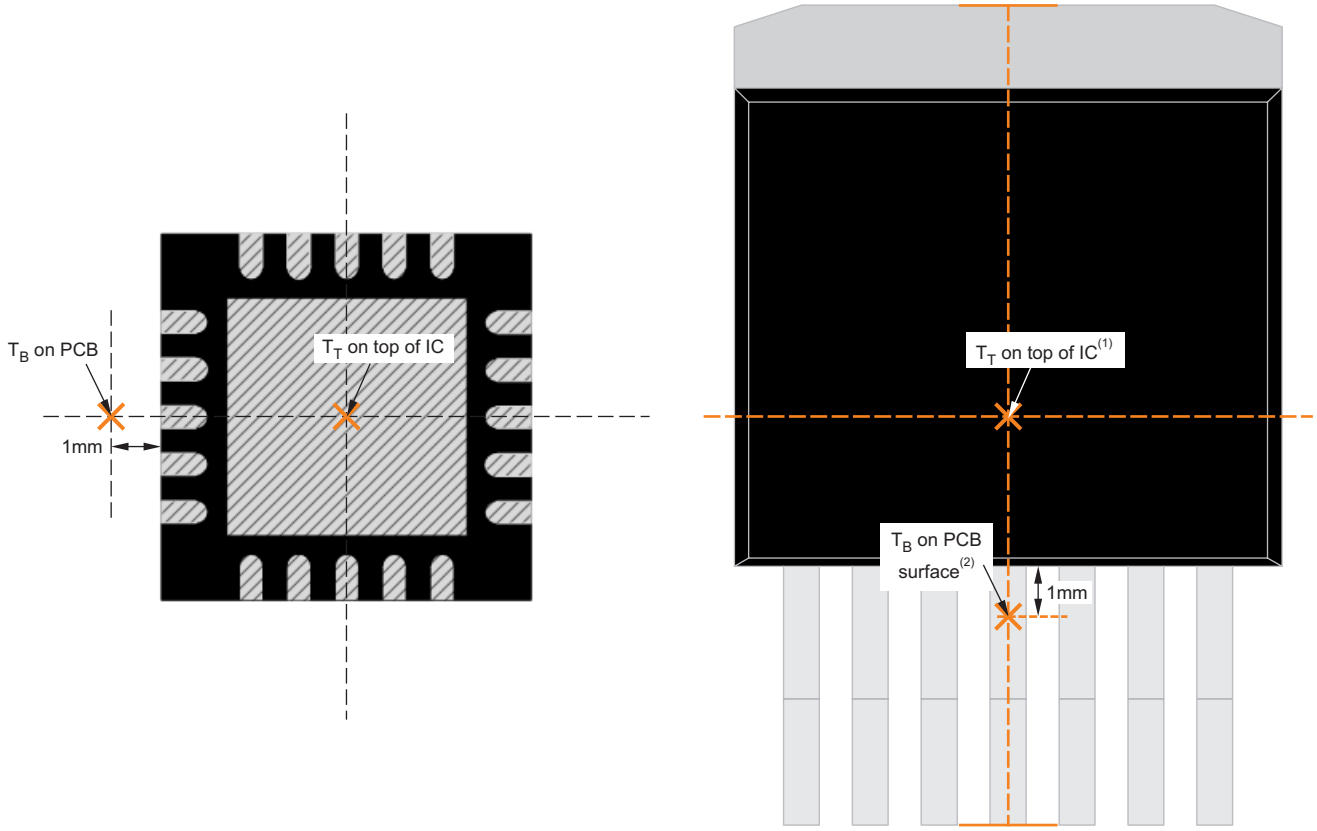
- P_D is the power dissipation shown by Equation 4
- T_T is the temperature at the center-top of the IC package
- T_B is the PCB temperature measured 1 mm away from the IC package *on the PCB surface* (see Figure 31) (6)

Thermal Considerations (continued)

NOTE

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the application note *Using New Thermal Metrics* (SBVA025), available for download at www.ti.com.



(a) Example RGW (VQFN) Package Measurement

(b) Example KTW (DDPAK) Package Measurement

(1) T_T is measured at the center of both the X- and Y-dimensional axes.

(2) T_B is measured below the package lead on the PCB surface.

Figure 31. Measuring Points for T_T and T_B

Compared with θ_{JA}, the thermal metrics Ψ_{JT} and Ψ_{JB} are less independent of board size but do have a small dependency on board size and layout. Figure 32 shows characteristic performance of Ψ_{JT} and Ψ_{JB} versus board size.

Referring to Figure 32, the RGW package thermal performance has negligible dependency on board size. The KTW package, however, does have a measurable dependency on board size. This dependency exists because the package shape is not point symmetric to an IC center. In the KTW package, for example (see Figure 31), silicon is not beneath the measuring point of T_T which is the center of the X and Y dimension, so that Ψ_{JT} has a dependency. Also, because of that non-point symmetry, device heat distribution on the PCB is not point symmetric either, so that Ψ_{JB} has a greater dependency on board size and layout.

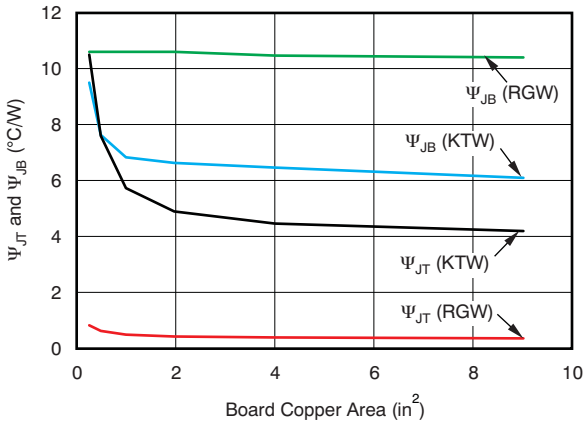


Figure 32. Ψ_{JT} and Ψ_{JB} versus Board Size

For a more detailed discussion of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, see the application note *Using New Thermal Metrics* (SBVA025), available for download at www.ti.com. Also, see the application note *IC Package Thermal Metrics* (SPRA953) (also available on the TI website) for further information.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS48. The TPS74901EVM-210 evaluation module and related user's guide (SLVU190) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS748 is available through the product folders under *Tools & Software*.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- *Using New Thermal Metrics*, SBVA025
- *IC Package Thermal Metrics*, SPRA953
- *Ultimate Regulation of with Fixed Output Versions of the TPS742xx, TPS743xx, and TPS744xx*, SBVA024
- *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator*, SBVA042
- *TPS74901EVM-210 Evaluation Module User Guide*, SLVU190

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS74901DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11S	Samples
TPS74901DRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11S	Samples
TPS74901KTWR	ACTIVE	DDPAK/ TO-263	KTW	7	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TPS74901	Samples
TPS74901KTWRG3	ACTIVE	DDPAK/ TO-263	KTW	7	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TPS74901	Samples
TPS74901KTWT	ACTIVE	DDPAK/ TO-263	KTW	7	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TPS74901	Samples
TPS74901KTWTG3	ACTIVE	DDPAK/ TO-263	KTW	7	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TPS74901	Samples
TPS74901RGWR	ACTIVE	VQFN	RGW	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74901	Samples
TPS74901RGWT	ACTIVE	VQFN	RGW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74901	Samples
TPS74901RGWTG4	ACTIVE	VQFN	RGW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74901	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

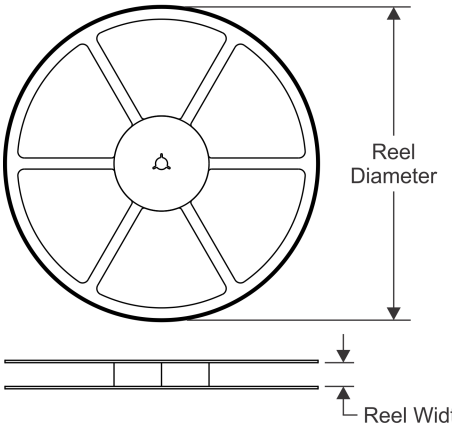
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

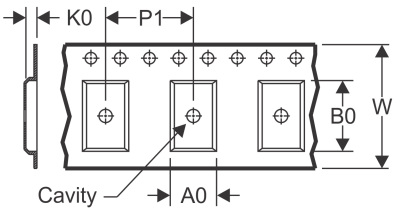
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

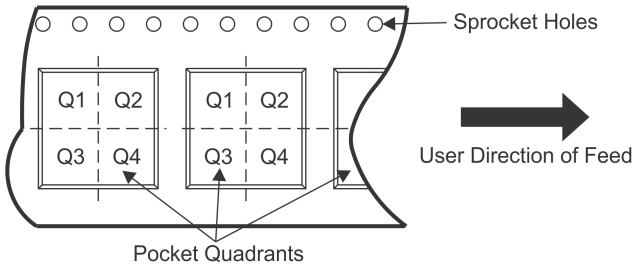


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

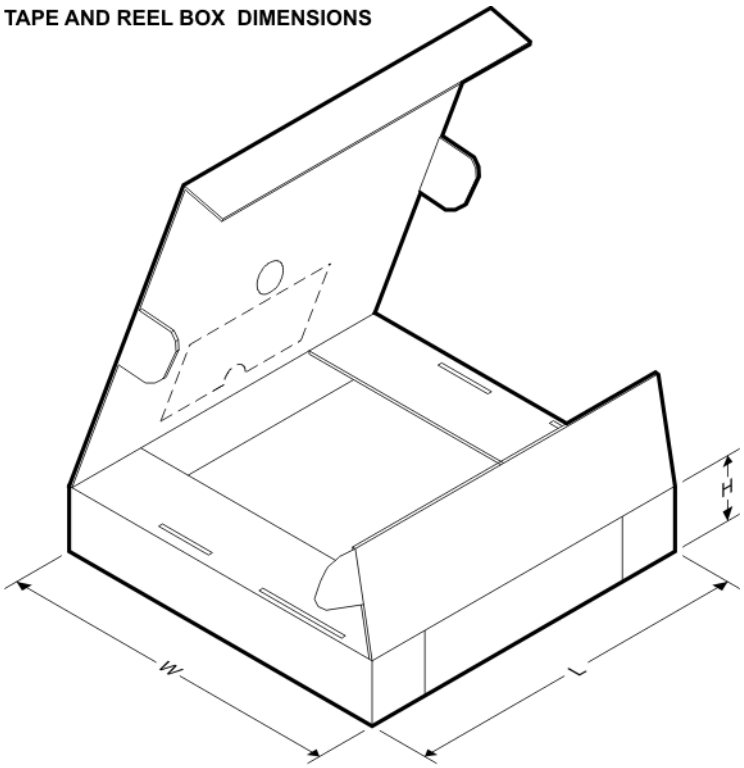
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS74901DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74901DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS74901KTWR	DDPAK/ TO-263	KTW	7	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS74901KTWT	DDPAK/ TO-263	KTW	7	50	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
TPS74901RGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS74901RGWT	VQFN	RGW	20	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

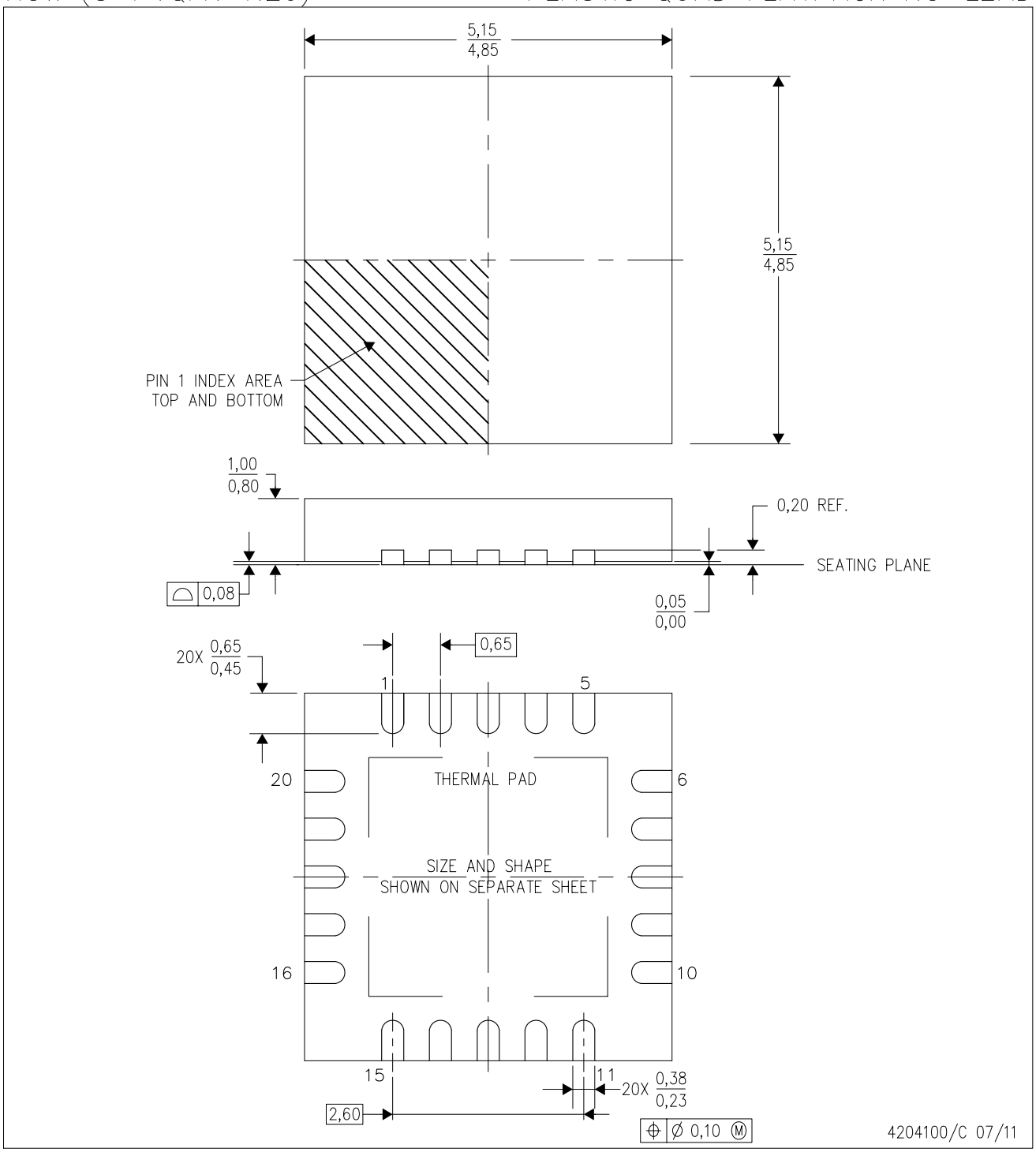
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS74901DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS74901DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS74901KTWR	DDPAK/TO-263	KTW	7	500	367.0	367.0	45.0
TPS74901KTWT	DDPAK/TO-263	KTW	7	50	367.0	367.0	45.0
TPS74901RGWR	VQFN	RGW	20	3000	367.0	367.0	35.0
TPS74901RGWT	VQFN	RGW	20	250	210.0	185.0	35.0

RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flat pack, No–leads (QFN) package configuration
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

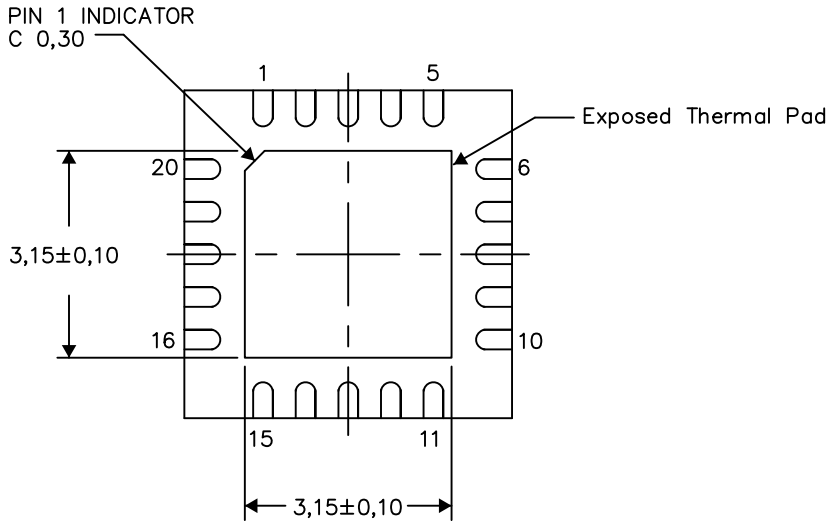
RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



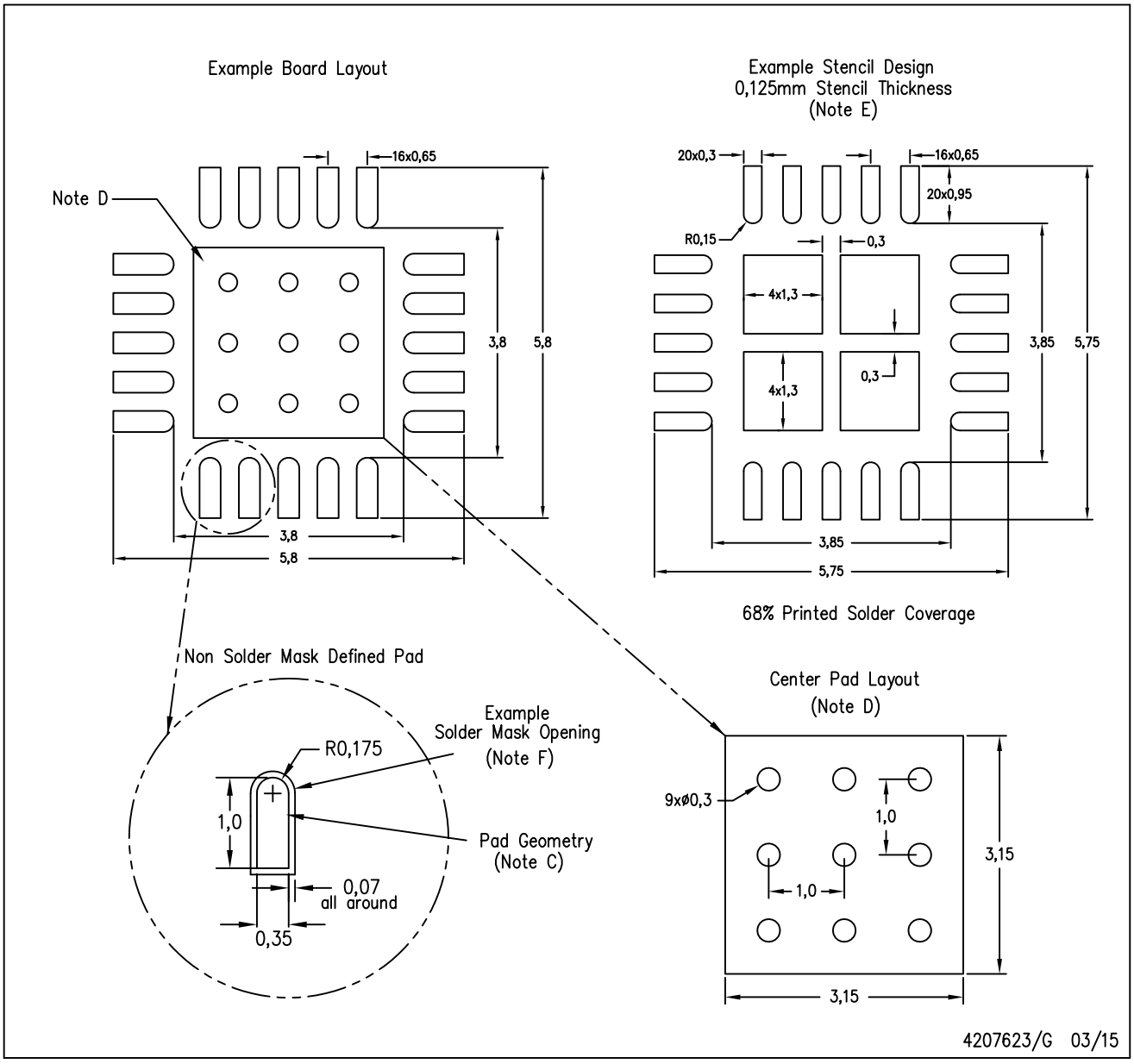
Bottom View

Exposed Thermal Pad Dimensions

4206352–2/M 06/15

NOTE: All linear dimensions are in millimeters

RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

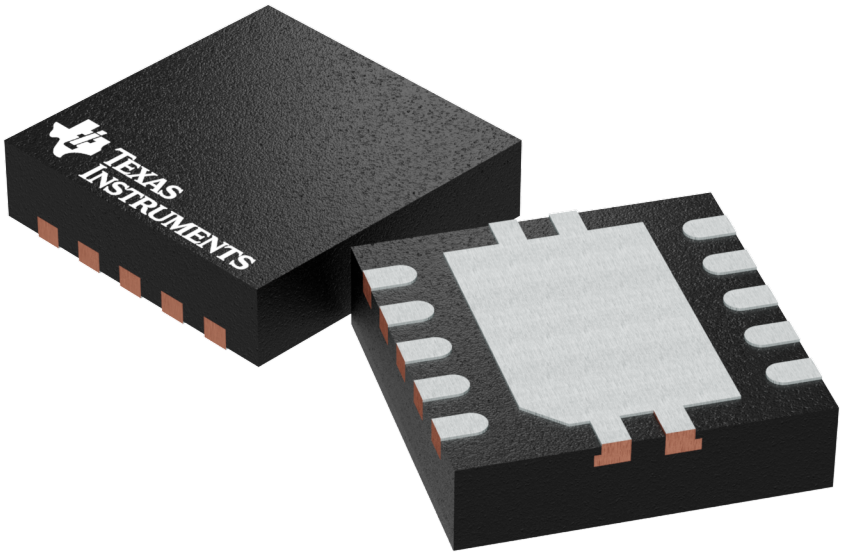


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

DRC 10

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



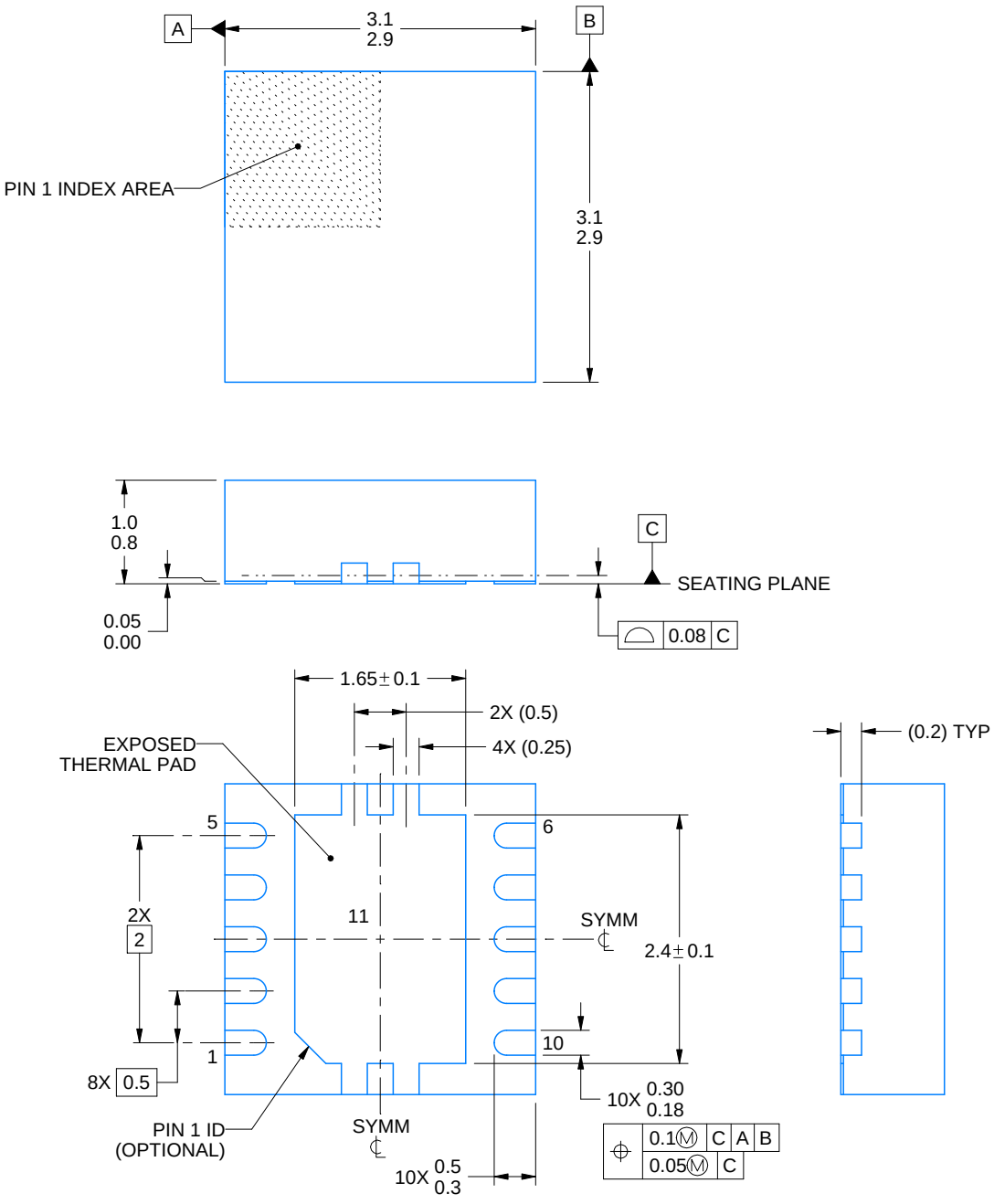
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DRC0010J

PACKAGE OUTLINE

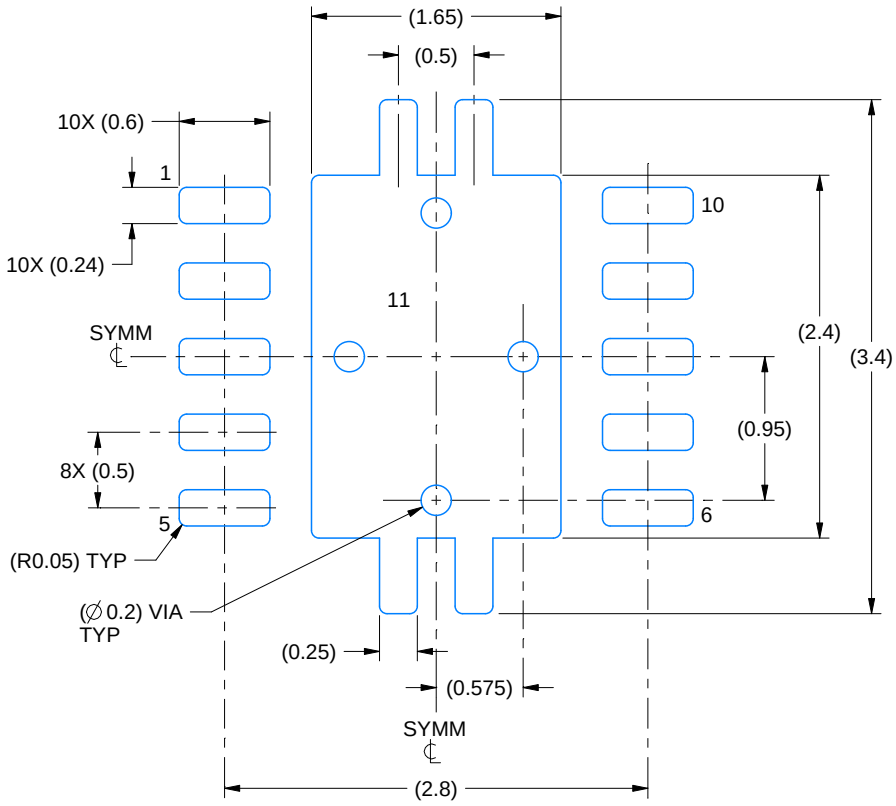
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

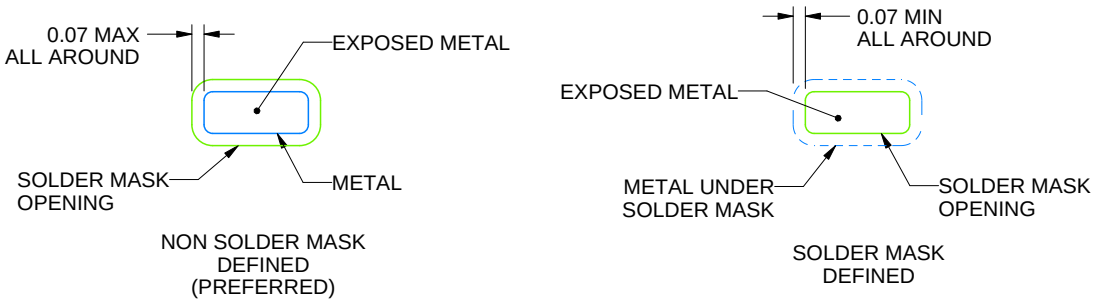


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

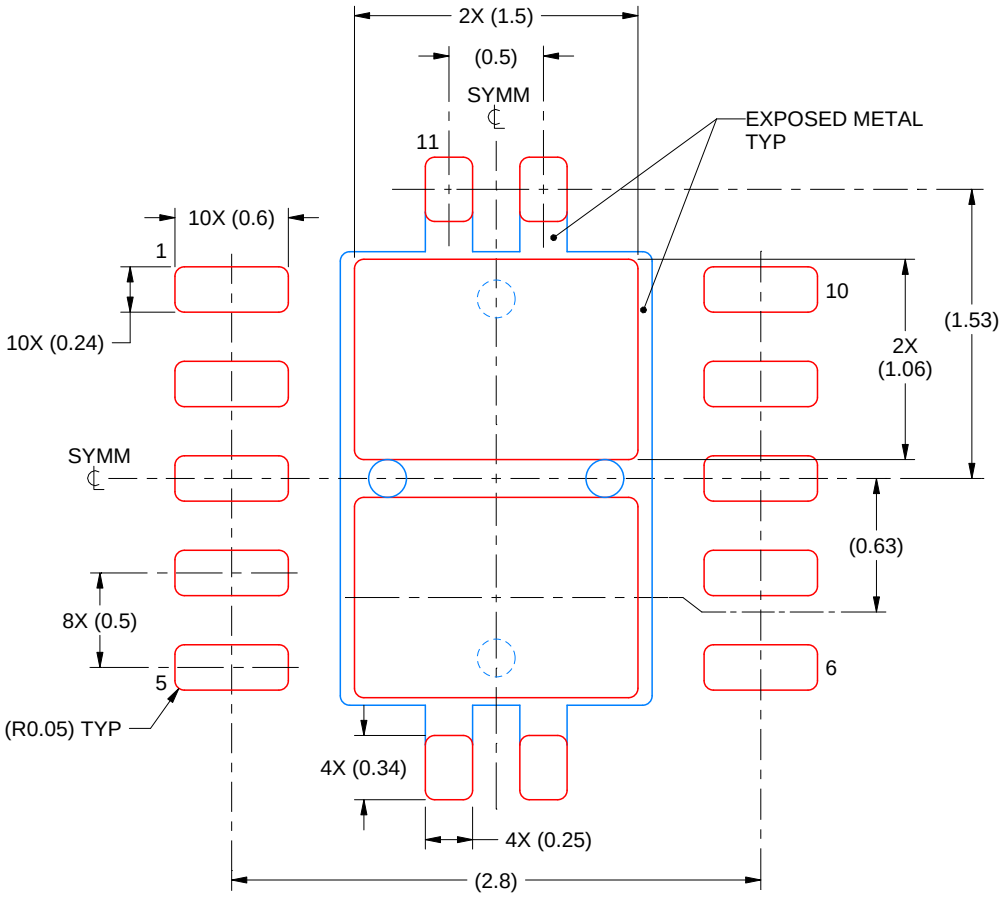
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

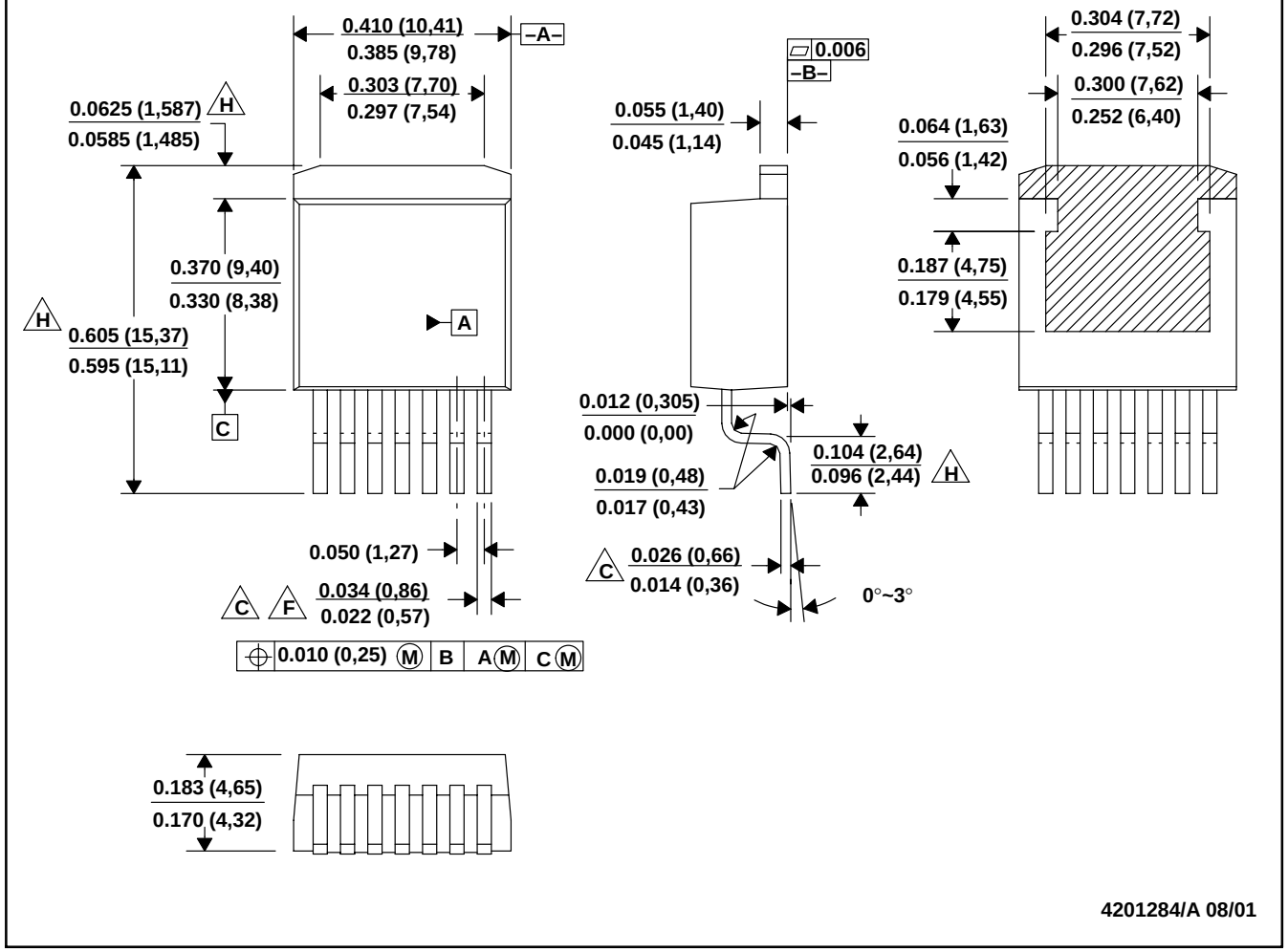
4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MPSF015 – AUGUST 2001

KTW (R-PSFM-G7) **PLASTIC FLANGE-MOUNT**



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead width and height dimensions apply to the plated lead.
D. Leads are not allowed above the Datum B.
E. Stand–off height is measured from lead tip with reference to Datum B.
F. Lead width dimension does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum dimension by more than 0.003”.
G. Cross–hatch indicates exposed metal surface.
H. Falls within JEDEC MO–169 with the exception of the dimensions indicated.

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