LM2731 0.6/1.6-MHz Boost Converters With 22-V Internal FET Switch in SOT-23

1 Features

- 22-V DMOS FET Switch
- 1.6-MHz (X Option), 0.6-MHz (Y Option) Switching Frequency
- Low R_{DS}(ON) DMOS FET
- Switch Current Up to 1.8 A
- Wide Input Voltage Range (2.7 V to 14 V)
- Low Shutdown Current (<1 µA)
- 5-Lead SOT-23 Package
- Uses Tiny Capacitors and Inductors
- Cycle-by-Cycle Current Limiting
- Internally Compensated

2 Applications

- White LED Current Sources
- PDAs and Palm-Top Computers
- Digital Cameras
- Portable Phones and Games
- Local Boost Regulators

3 Description

The LM2731 switching regulators are current-mode boost converters operating at fixed frequencies of 1.6 MHz (X option) and 600 kHz (Y option).

The use of SOT-23 package, made possible by the minimal power loss of the internal 1.8-A switch, and use of small inductors and capacitors result in the highest power density of the industry. The 22-V internal switch makes these solutions perfect for boosting to voltages up to 20 V.

These parts have a logic-level shutdown pin that can reduce quiescent current and extend battery life.

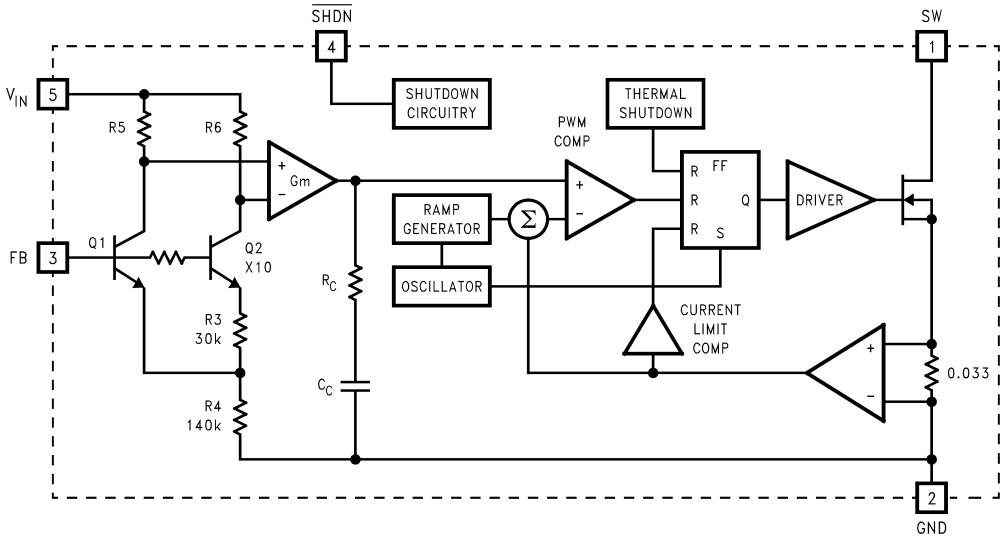
Protection is provided through cycle-by-cycle current limiting and thermal shutdown. Internal compensation simplifies design and reduces component count.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM2731	SOT-23 (5)	1.60 mm × 2.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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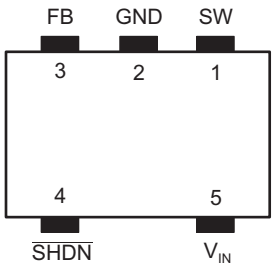
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (November 2012) to Revision G	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
FB	3	I	Feedback point that connects to external resistive divider.
GND	2	PWR	Analog and power ground
$\overline{SHDN}$	4	I	Shutdown control input. Connect to V_{IN} if the feature is not used.
SW	1	O	Drain of the internal FET switch
V_{IN}	5	PWR	Analog and power input

6 Specifications

6.1 Absolute Maximum Ratings(1)

	MIN	MAX	UNIT
Operating Junction Temperature	–40	125	°C
Lead Temperature (Soldering, 5 sec.)		300	°C
Power Dissipation(2)	Internally Limited		
FB Pin Voltage	–0.4	6	V
SW Pin Voltage	–0.4	22	V
Input Supply Voltage	–0.4	14.5	V
$\overline{SHDN}$ Pin Voltage	–0.4	V_{IN} + 0.3	V
Storage Temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The maximum power dissipation which can be safely dissipated for any application is a function of the maximum junction temperature, $T_J(MAX)$ = 125°C, the junction-to-ambient thermal resistance for the SOT-23 package, $R_{\theta JA}$ = 265°C/W, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature for designs using this device can be calculated using the formula: $P(MAX) = \frac{T_J(MAX) - T_A}{\theta_{J-A}} = \frac{125 - T_A}{265}$. If power dissipation exceeds the maximum specified above, the internal thermal protection circuitry will protect the device by reducing the output voltage as required to maintain a safe junction temperature.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)(2)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input Supply Voltage	2.7		14	V
V_{sw}	SW Pin Voltage	3		20	V
V_{shdn}	Shutdown Supply Voltage(1)	0		VIN	V
T_J	Junction Temperature Range	–40		125	ºC

(1) This pin should not be allowed to float or be greater than V_{IN} + 0.3 V.

6.4 Thermal Information

THERMAL METRIC(1)		LM2731 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	209.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	122	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	38.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Limits are for T_J = 25°C. Unless otherwise specified: V_{IN} = 5 V, V_{SHDN} = 5 V, I_L = 0 A.

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
V_{IN}	Input Voltage	−40°C ≤ T_J ≤ 125°C		2.7		14	V
$V_{OUT\ (MIN)}$	Minimum Output Voltage Under Load	R_L = 43 Ω X Option(3)	V_{IN} = 2.7 V		7		V
			−40°C ≤ T_J ≤ 125°C	5.4			
			V_{IN} = 3.3 V		10		
			−40°C ≤ T_J ≤ 125°C	8			
			V_{IN} = 5 V		16		
		R_L = 43 Ω Y Option(3)	V_{IN} = 2.7 V		7.5		
			−40°C ≤ T_J ≤ 125°C	6			
			V_{IN} = 3.3 V		11		
			−40°C ≤ T_J ≤ 125°C	8.75			
			V_{IN} = 5 V		15		
		R_L = 15 Ω X Option(3)	V_{IN} = 2.7 V		5		
			−40°C ≤ T_J ≤ 125°C	3.75			
			V_{IN} = 3.3 V		6.5		
			−40°C ≤ T_J ≤ 125°C	5			
			V_{IN} = 5 V		10		
		R_L = 15 Ω Y Option(3)	V_{IN} = 2.7 V		5		
			−40°C ≤ T_J ≤ 125°C	4			
			V_{IN} = 3.3 V		7		
			−40°C ≤ T_J ≤ 125°C	5.5			
			V_{IN} = 5 V		10		
I_{SW}	Switch Current Limit	See(4)	T_J = 25°C	1.8	2		A
			−40°C ≤ T_J ≤ 125°C	1.4			
$R_{DS}(ON)$	Switch ON-Resistance	I_{SW} = 100 mA Vin = 5 V	T_J = 25°C		260	400	mΩ
			−40°C ≤ T_J ≤ 125°C			500	
		I_{SW} = 100 mA Vin = 3.3 V	T_J = 25°C		300	450	
			−40°C ≤ T_J ≤ 125°C			550	
$SHDN_{TH}$	Shutdown Threshold	Device ON	−40°C ≤ T_J ≤ 125°C	1.5			V
		Device OFF	−40°C ≤ T_J ≤ 125°C			0.5	
I_{SHDN}	Shutdown Pin Bias Current	V_{SHDN} = 0			0		μA
		V_{SHDN} = 5 V	T_J = 25°C		0		
			−40°C ≤ T_J ≤ 125°C			2	
V_{FB}	Feedback Pin Reference Voltage	V_{IN} = 3 V	T_J = 25°C		1.230		V
			−40°C ≤ T_J ≤ 125°C	1.205		1.255	
I_{FB}	Feedback Pin Bias Current	V_{FB} = 1.23 V	T_J = 25°C		60		nA
			−40°C ≤ T_J ≤ 125°C			500	

(1) Limits are ensured by testing, statistical correlation, or design.
(2) Typical values are derived from the mean value of a large quantity of samples tested during characterization and represent the most likely expected value of the parameter at room temperature.
(3) L = 10 μH, C_{OUT} = 4.7 μF, duty cycle = maximum
(4) Switch current limit is dependent on duty cycle (see *Typical Characteristics*).

Electrical Characteristics (continued)

Limits are for T_J = 25°C. Unless otherwise specified: V_{IN} = 5 V, V_{SHDN} = 5 V, I_L = 0 A.

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
I_Q	Quiescent Current	V_{SHDN} = 5 V, Switching "X"	T_J = 25°C		2		mA
			−40°C ≤ T_J ≤ 125°C			3	
		V_{SHDN} = 5 V, Switching "Y"	T_J = 25°C		1		
			−40°C ≤ T_J ≤ 125°C			2	
		V_{SHDN} = 5 V, Not Switching	T_J = 25°C		400		µA
			−40°C ≤ T_J ≤ 125°C			500	
		V_{SHDN} = 0			0.024	1	
$\Delta V_{FB}/\Delta V_{IN}$	FB Voltage Line Regulation	2.7 V ≤ V_{IN} ≤ 14 V			0.02		%/V
F_{SW}	Switching Frequency(5)	"X" Option	T_J = 25°C		1.6		MHz
			−40°C ≤ T_J ≤ 125°C	1		1.85	
		"Y" Option	T_J = 25°C		0.6		
			−40°C ≤ T_J ≤ 125°C	0.4		0.8	
D_{MAX}	Maximum Duty Cycle(5)	"X" Option	T_J = 25°C		86%		
			−40°C ≤ T_J ≤ 125°C	78%			
		"Y" Option	T_J = 25°C		93%		
			−40°C ≤ T_J ≤ 125°C	88%			
I_L	Switch Leakage	Not Switching V_{SW} = 5 V				1	µA

(5) Specified limits are the same for Vin = 3.3 V input.

6.6 Typical Characteristics

Unless otherwise specified: V_{IN} = 5 V, $\overline{SHDN}$ pin tied to V_{IN}.

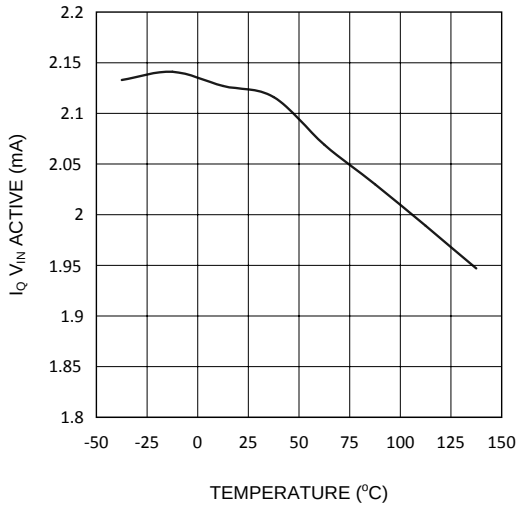


Figure 1. I_q V_{IN} (Active) vs Temperature - X Option

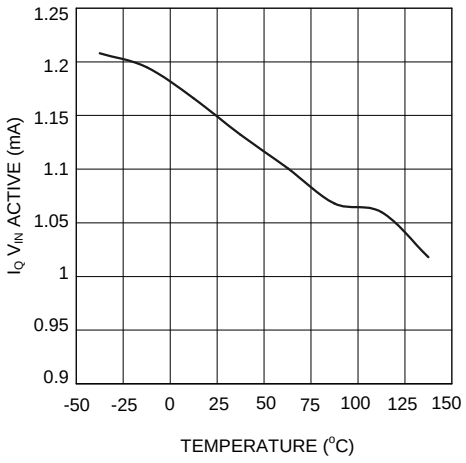


Figure 2. I_q V_{IN} (Active) vs Temperature - Y Option

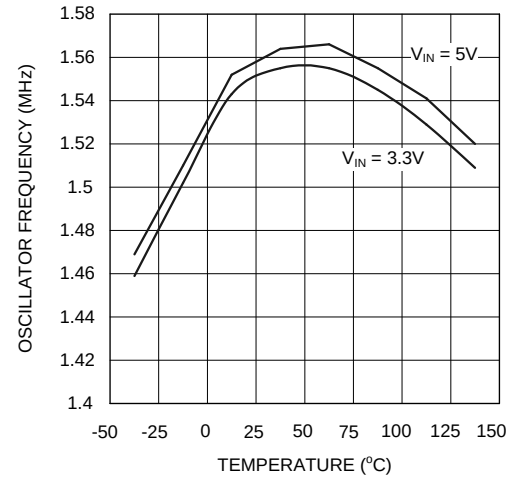


Figure 3. Oscillator Frequency vs Temperature - X Option

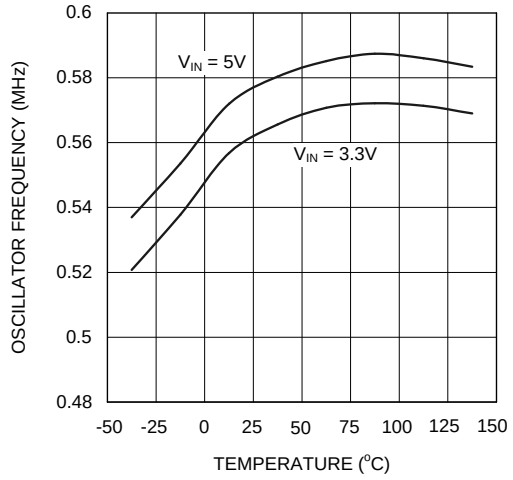


Figure 4. Oscillator Frequency vs Temperature - Y Option

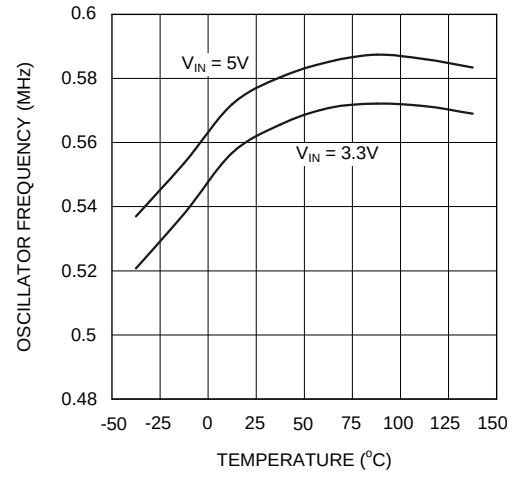


Figure 5. Maximum Duty Cycle vs Temperature - X Option

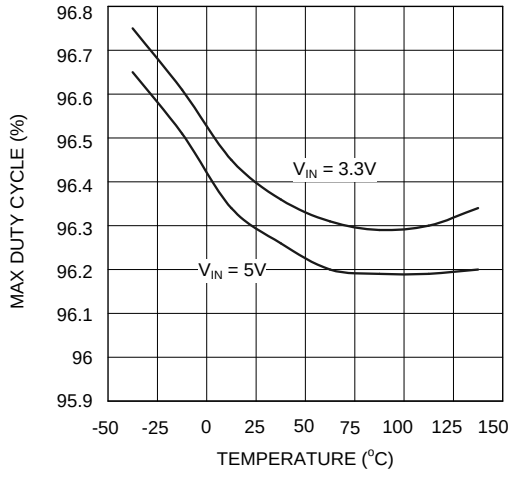


Figure 6. Maximum Duty Cycle vs Temperature - Y Option

Typical Characteristics (continued)

Unless otherwise specified: V_{IN} = 5 V, $\overline{SHDN}$ pin tied to V_{IN}.

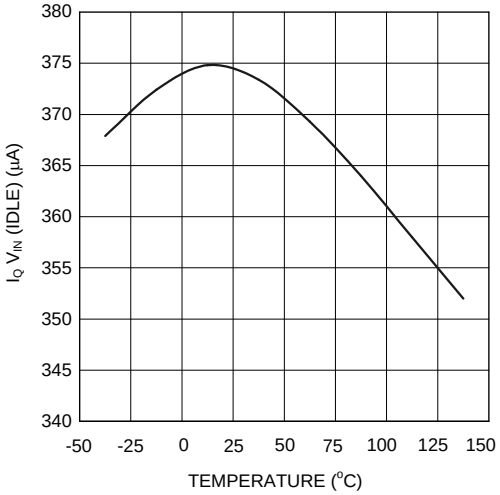


Figure 7. I_q V_{IN} (Idle) vs Temperature

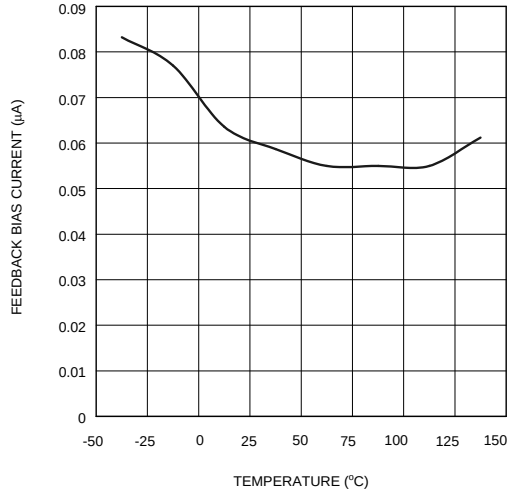


Figure 8. Feedback Bias Current vs Temperature

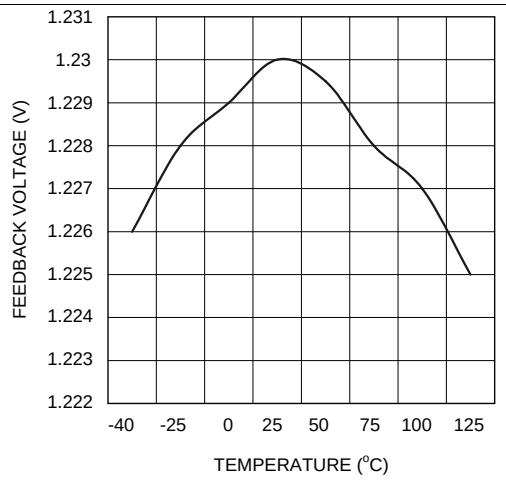


Figure 9. Feedback Voltage vs Temperature

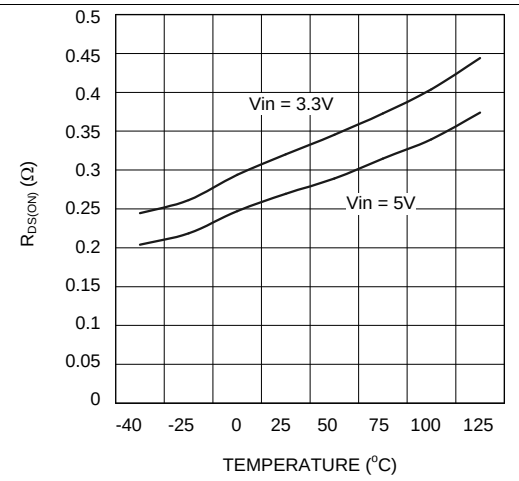


Figure 10. R_{DS}(ON) vs Temperature

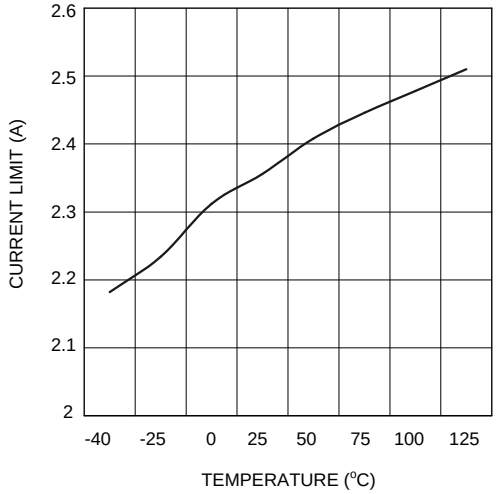


Figure 11. Current Limit vs Temperature

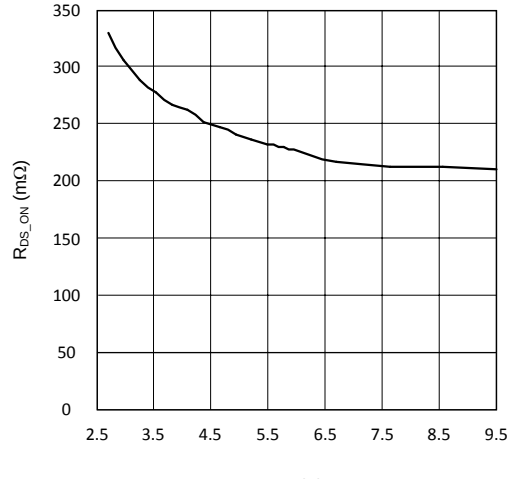
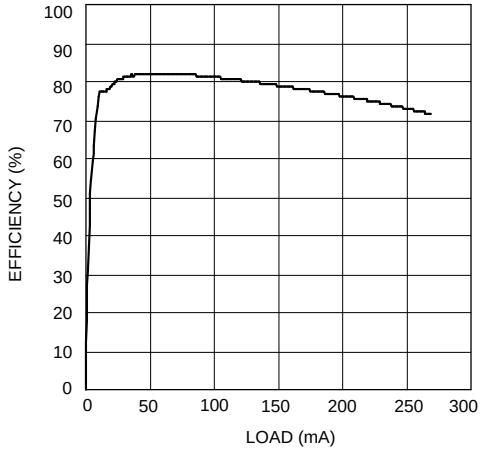


Figure 12. R_{DS}(ON) vs V_{IN}

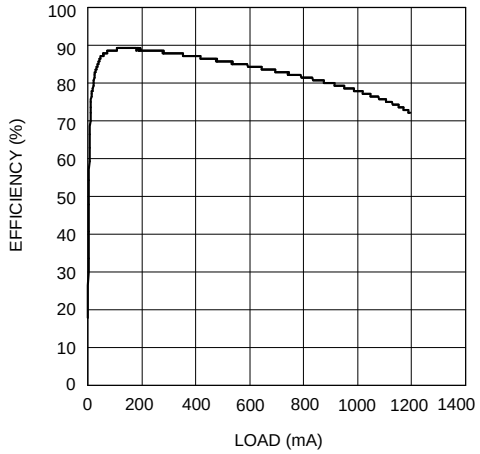
Typical Characteristics (continued)

Unless otherwise specified: V_{IN} = 5 V, $\overline{SHDN}$ pin tied to V_{IN}.



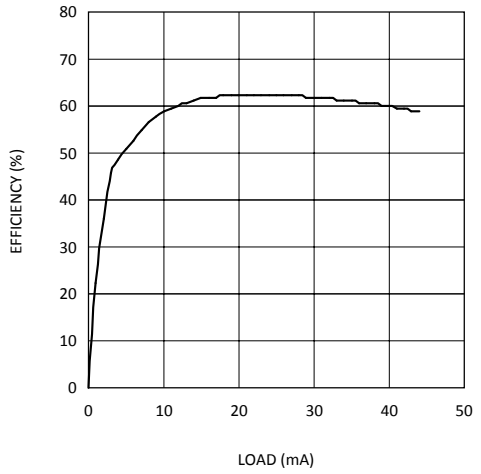
V_{IN} = 2.7 V V_{OUT} = 5 V

Figure 13. Efficiency vs Load Current - X Option



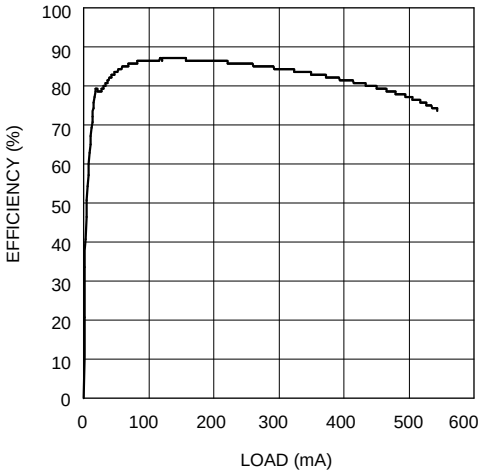
V_{IN} = 4.2 V V_{OUT} = 5 V

Figure 14. Efficiency vs Load Current - X Option



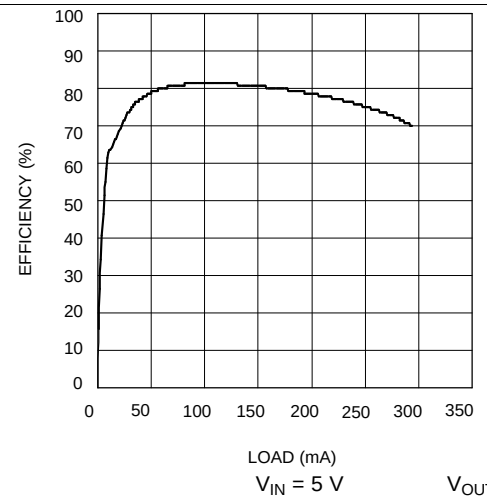
V_{IN} = 2.7 V V_{OUT} = 12 V

Figure 15. Efficiency vs Load Current - X Option



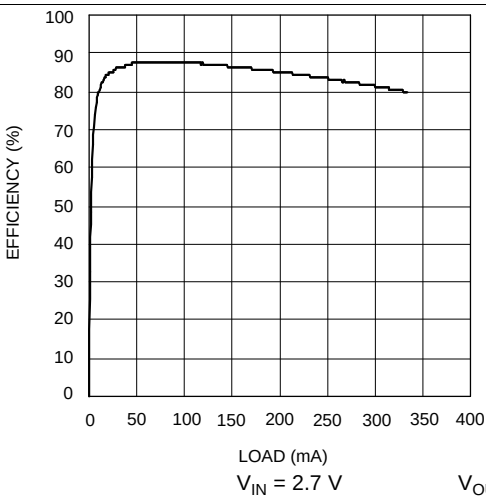
V_{IN} = 5 V V_{OUT} = 12 V

Figure 16. Efficiency vs Load Current - X Option



V_{IN} = 5 V V_{OUT} = 18 V

Figure 17. Efficiency vs Load Current - X Option

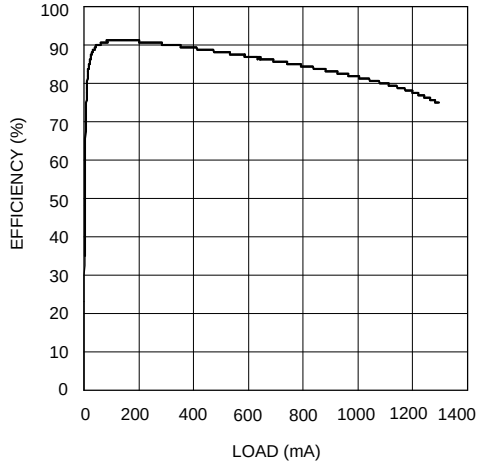


V_{IN} = 2.7 V V_{OUT} = 5 V

Figure 18. Efficiency vs Load Current - Y Option

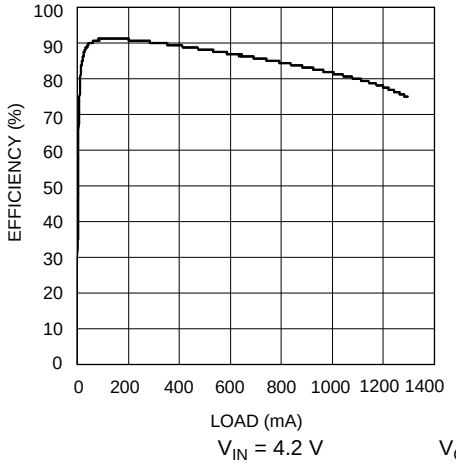
Typical Characteristics (continued)

Unless otherwise specified: V_{IN} = 5 V, $\overline{SHDN}$ pin tied to V_{IN}.



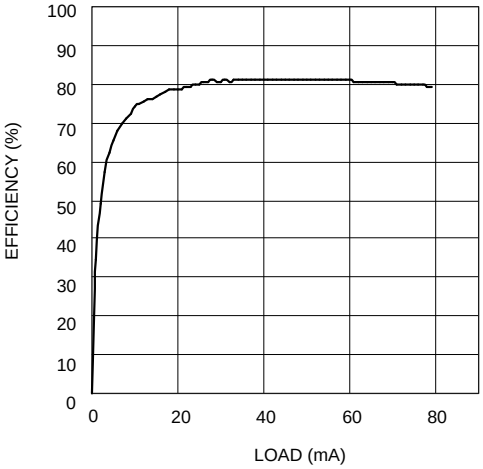
V_{IN} = 3.3 V V_{OUT} = 5 V

Figure 19. Efficiency vs Load Current - Y Option



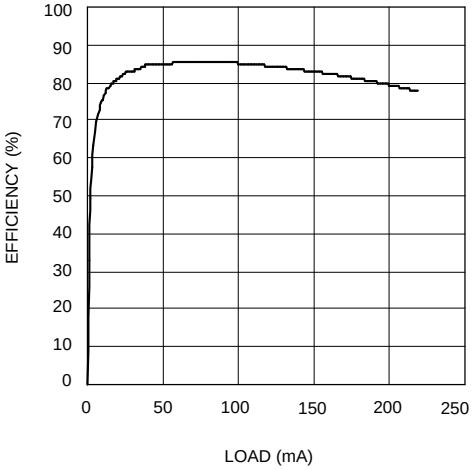
V_{IN} = 4.2 V V_{OUT} = 5 V

Figure 20. Efficiency vs Load Current - Y Option



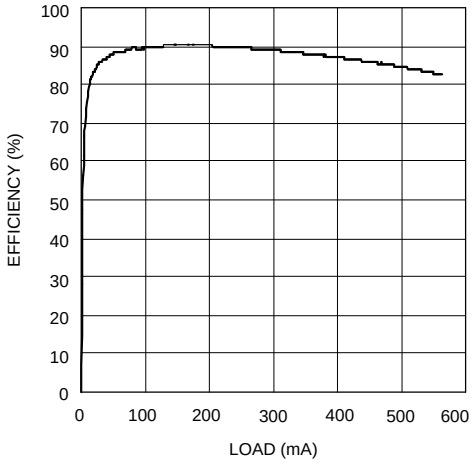
V_{IN} = 2.7 V V_{OUT} = 12 V

Figure 21. Efficiency vs Load Current - Y Option



V_{IN} = 3.3 V V_{OUT} = 12 V

Figure 22. Efficiency vs Load Current - Y Option



V_{IN} = 5 V V_{OUT} = 12 V

Figure 23. Efficiency vs Load Current - Y Option

7 Detailed Description

7.1 Overview

The LM2731 device is a switching converter IC that operates at a fixed frequency (0.6 or 1.6 MHz) for fast transient response over a wide input voltage range and incorporates pulse-by-pulse current limiting protection. Because this is current mode control, a 33-mΩ sense resistor in series with the switch FET is used to provide a voltage (which is proportional to the FET current) to both the input of the pulse width modulation (PWM) comparator and the current limit amplifier.

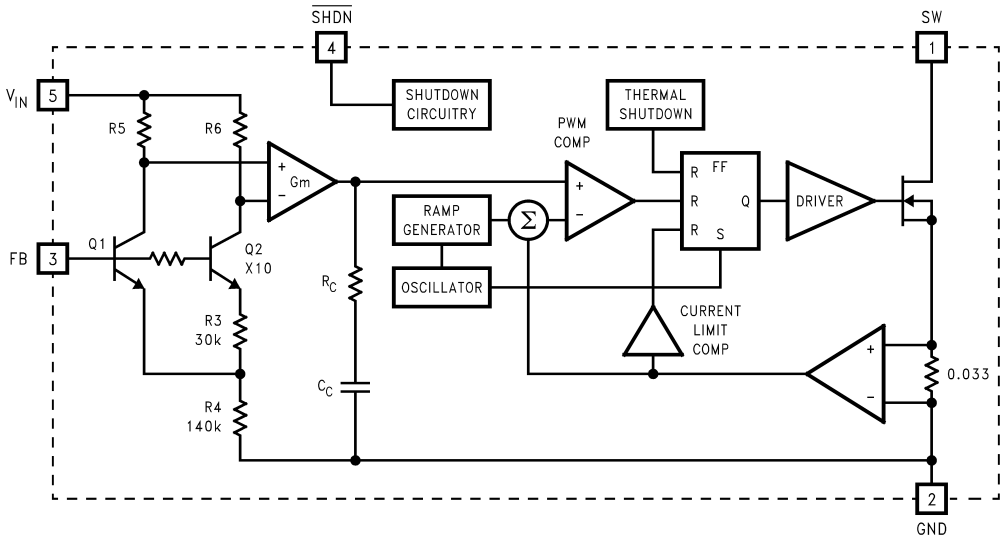
7.1.1 Theory of Operation

At the beginning of each cycle, the S-R latch turns on the FET. As the current through the FET increases, a voltage (proportional to this current) is summed with the ramp coming from the ramp generator and then fed into the input of the PWM comparator. When this voltage exceeds the voltage on the other input (coming from the Gm amplifier), the latch resets and turns the FET off. Because the signal coming from the Gm amplifier is derived from the feedback (which samples the voltage at the output), the action of the PWM comparator constantly sets the correct peak current through the FET to keep the output voltage in regulation.

Q1 and Q2 along with R3 - R6 form a bandgap voltage reference used by the IC to hold the output in regulation. The currents flowing through Q1 and Q2 will be equal, and the feedback loop will adjust the regulated output to maintain this. Because of this, the regulated output is always maintained at a voltage level equal to the voltage at the FB node "multiplied up" by the ratio of the output resistive-divider.

The current limit comparator feeds directly into the flip-flop that drives the switch FET. If the FET current reaches the limit threshold, the FET is turned off and the cycle terminated until the next clock pulse. The current limit input terminates the pulse regardless of the status of the output of the PWM comparator.

7.2 Functional Block Diagram



7.3 Feature Description

The LM2731 is a fixed-frequency boost regulator IC that delivers a minimum 1.8-A peak switch current.

The device provides cycle-by-cycle current limit protection as well as thermal shutdown protection. The device can also be controlled through the shutdown pin.

7.4 Device Functional Modes

7.4.1 Shutdown Pin Operation

The device is turned off by pulling the shutdown pin low. If this function is not going to be used, the pin should be tied directly to V_{IN}. If the SHDN function will be needed, a pullup resistor must be used to V_{IN} (approximately 50 kΩ to 100 kΩ recommended). The SHDN pin must not be left unterminated.

7.4.2 Thermal Shutdown

Thermal shutdown limits total power dissipation by turning off the output switch when the IC junction temperature exceeds 160°C. After thermal shutdown occurs, the output switch doesn't turn on until the junction temperature drops to approximately 150°C.

7.4.3 Current Limit

The LM2731 uses cycle-by-cycle current limiting to protect the internal NMOS switch. It is important to note that this current limit will not protect the output from excessive current during an output short-circuit. The input supply is connected to the output by the series connection of an inductor and a diode. If a short circuit is placed on the output, excessive current can damage both the inductor and diode.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The device will operate with input voltage range from 2.7 V to 14 V and provide a regulated output voltage. This device is optimized for high-efficiency operation with minimum number of external components. For component selection, see *Detailed Design Procedure*.

8.2 Typical Application

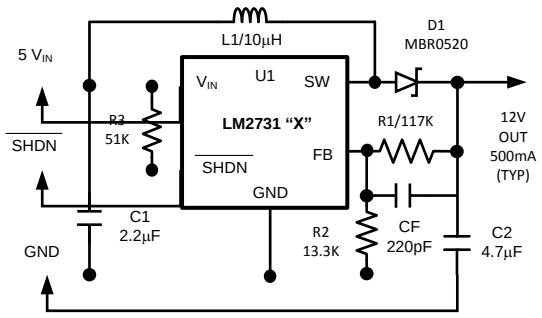


Figure 24. Application Schematic

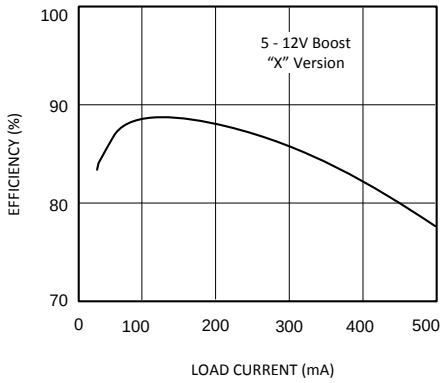


Figure 25. Efficiency vs Load Current

8.2.1 Design Requirements

The device must be able to operate at any voltage within the recommended operating range. The load current must be defined in order to properly size the inductor, input, and output capacitors. The inductor must be able to handle full expected load current as well as the peak current generated during load transients and start-up. Inrush current at start-up will depend on the output capacitor selection. More details are provided in *Detailed Design Procedure*.

The device has a shutdown pin which is used to disable the device. This pin is active-LOW and care must be taken that the voltage on this pin does not exceed VIN + 0.3 V. This pin must also not be left floating.

8.2.2 Detailed Design Procedure

8.2.2.1 Selecting the External Capacitors

The best capacitors for use with the LM2731 are multi-layer ceramic capacitors. These capacitors have the lowest ESR (equivalent series resistance) and highest resonance frequency which makes them optimum for use with high-frequency switching converters.

When selecting a ceramic capacitor, only X5R and X7R dielectric types should be used. Other types such as Z5U and Y5F have such severe loss of capacitance due to effects of temperature variation and applied voltage, they may provide as little as 20% of rated capacitance in many typical applications. Always consult capacitor manufacturer's data curves before selecting a capacitor. High-quality ceramic capacitors can be obtained from Taiyo-Yuden, AVX, and Murata.

8.2.2.2 Selecting the Output Capacitor

A single ceramic capacitor of value 4.7 µF to 10 µF will provide sufficient output capacitance for most applications. If larger amounts of capacitance are desired for improved line support and transient response, tantalum capacitors can be used. Aluminum electrolytics with ultra low ESR such as Sanyo Oscon can be used, but are usually prohibitively expensive. Typical AI electrolytic capacitors are not suitable for switching frequencies above 500 kHz due to significant ringing and temperature rise due to self-heating from ripple current. An output capacitor with excessive ESR can also reduce phase margin and cause instability.

In general, if electrolytics are used, TI recommends that they be paralleled with ceramic capacitors to reduce ringing, switching losses, and output voltage ripple.

8.2.2.3 Selecting the Input Capacitor

An input capacitor is required to serve as an energy reservoir for the current which must flow into the coil each time the switch turns ON. This capacitor must have extremely low ESR, so ceramic is the best choice. TI recommends a nominal value of 2.2 µF, but larger values can be used. Since this capacitor reduces the amount of voltage ripple seen at the input pin, it also reduces the amount of EMI passed back along that line to other circuitry.

8.2.2.4 Feedforward Compensation

Although internally compensated, the feedforward capacitor Cf is required for stability (see Figure 26). Adding this capacitor puts a zero in the loop response of the converter. The recommended frequency for the zero fz should be approximately 6 kHz. Cf can be calculated using the formula:

$$Cf = 1 / (2 \times \pi \times R1 \times fz) \quad (1)$$

8.2.2.5 Selecting Diodes

The external diode used in the typical application should be a Schottky diode. TI recommends a 20-V diode such as the MBR0520.

The MBR05XX series of diodes are designed to handle a maximum average current of 0.5 A. For applications exceeding 0.5-A average but less than 1 A, a Microsemi UPS5817 can be used.

8.2.2.6 Setting the Output Voltage

The output voltage is set using the external resistors R1 and R2 (see Figure 26). A minimum value of 13.3 kΩ is recommended for R2 to establish a divider current of approximately 92 µA. R1 is calculated using the formula:

$$R1 = R2 \times (V_{OUT}/1.23 - 1) \quad (2)$$

8.2.2.7 Switching Frequency

The LM2731 is provided with two switching frequencies: the “X” version is typically 1.6 MHz, while the “Y” version is typically 600 kHz. The best frequency for a specific application must be determined based on the trade-offs involved:

Higher switching frequency means the inductors and capacitors can be made smaller and cheaper for a given output voltage and current. The down side is that efficiency is slightly lower because the fixed switching losses occur more frequently and become a larger percentage of total power loss. EMI is typically worse at higher switching frequencies because more EMI energy will be seen in the higher frequency spectrum where most circuits are more sensitive to such interference.

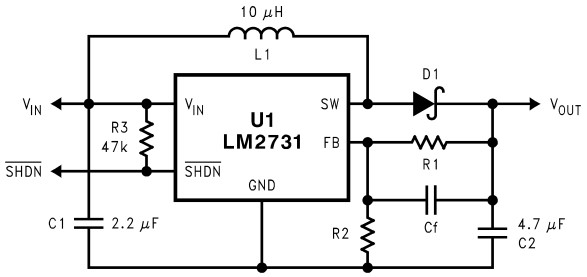


Figure 26. Basic Application Circuit

8.2.2.8 Duty Cycle

The maximum duty cycle of the switching regulator determines the maximum boost ratio of output-to-input voltage that the converter can attain in continuous mode of operation. The duty cycle for a given boost application is defined as:

$$\text{Duty Cycle} = \frac{V_{OUT} + V_{DIODE} - V_{IN}}{V_{OUT} + V_{DIODE} - V_{SW}} \quad (3)$$

This applies for continuous mode operation.

8.2.2.9 Inductance Value

The first question that is usually asked is: "How small can I make the inductor?" (because they are the largest sized component and usually the most costly). The answer is not simple and involves trade-offs in performance. Larger inductors mean less inductor ripple current, which typically means less output voltage ripple (for a given size of output capacitor). Larger inductors also mean more load power can be delivered because the energy stored during each switching cycle is:

$$E = L/2 \times (Ip)^2 \quad (4)$$

Where "Ip" is the peak inductor current. An important point to observe is that the LM2731 will limit its switch current based on peak current. This means that since Ip(max) is fixed, increasing L will increase the maximum amount of power available to the load. Conversely, using too little inductance may limit the amount of load current which can be drawn from the output.

Best performance is usually obtained when the converter is operated in "continuous" mode at the load current range of interest, typically giving better load regulation and less output ripple. Continuous operation is defined as not allowing the inductor current to drop to zero during the cycle. All boost converters shift over to discontinuous operation as the output load is reduced far enough, but a larger inductor stays "continuous" over a wider load current range.

To better understand these trade-offs, a typical application circuit (5-V to 12-V boost with a 10-µH inductor) will be analyzed. We will assume:

$$V_{IN} = 5\ V,\ V_{OUT} = 12\ V,\ V_{DIODE} = 0.5\ V,\ V_{SW} = 0.5\ V \quad (5)$$

Because the frequency is 1.6 MHz (nominal), the period is approximately 0.625 µs. The duty cycle will be 62.5%, which means the ON-time of the switch is 0.390 µs. When the switch is ON, the voltage across the inductor is approximately 4.5 V.

Using the equation:

$$V = L\ (di/dt) \quad (6)$$

The di/dt rate of the inductor can then be calculated, which is found to be 0.45 A/µs during the ON time. Using these facts, what the inductor current will look like during operation can be shown:

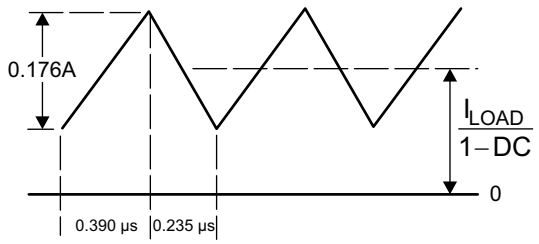


Figure 27. 10 µH Inductor Current, 5 V–12 V Boost (LM2731X)

During the 0.390-µs ON-time, the inductor current ramps up 0.176 A and ramps down an equal amount during the OFF-time. This is defined as the inductor "ripple current". If the load current drops to about 33 mA, the inductor current will begin touching the zero axis which means it will be in discontinuous mode. A similar analysis can be performed on any boost converter, to make sure the ripple current is reasonable and continuous operation will be maintained at the typical load current values.

8.2.2.10 Maximum Switch Current

The maximum FET switch current available before the current limiter cuts in is dependent on duty cycle of the application. This is illustrated in the graphs below which show typical values of switch current for both the "X" and "Y" versions as a function of effective (actual) duty cycle:

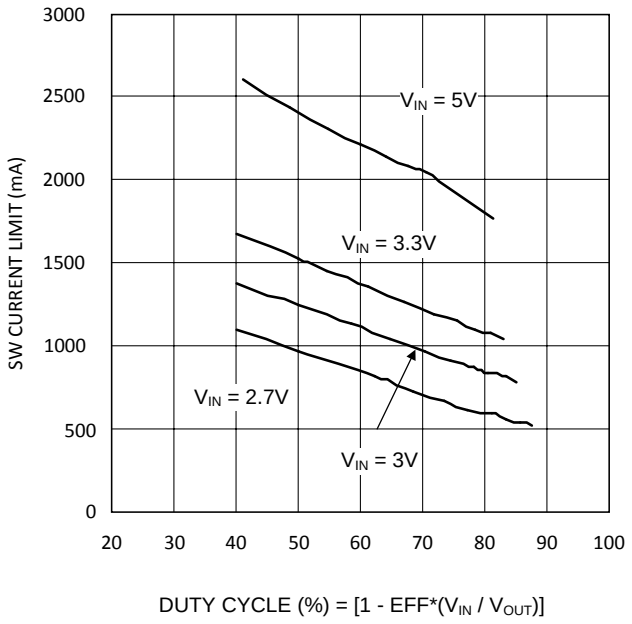


Figure 28. Switch Current Limit vs Duty Cycle - X Option

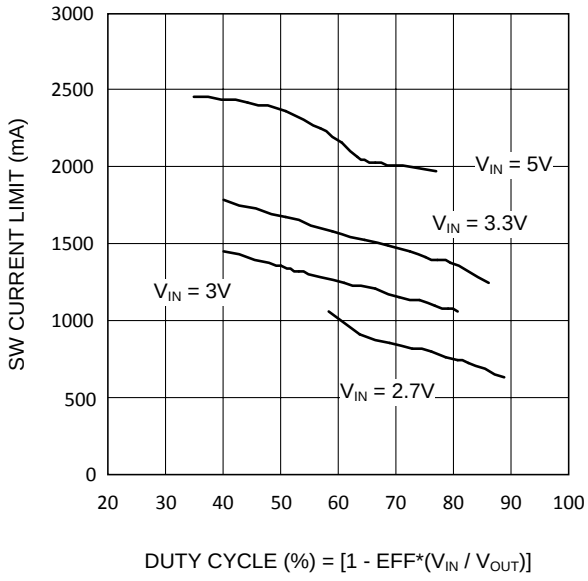


Figure 29. Switch Current Limit vs Duty Cycle - Y Option

8.2.2.11 Calculating Load Current

As shown in the figure which depicts inductor current, the load current is related to the average inductor current by the relation:

$$I_{LOAD} = I_{IND}(AVG) \times (1 - DC) \quad (7)$$

Where "DC" is the duty cycle of the application. The switch current can be found by:

$$I_{SW} = I_{IND}(AVG) + ½ (I_{RIPPLE}) \quad (8)$$

Inductor ripple current is dependent on inductance, duty cycle, input voltage and frequency:

$$I_{RIPPLE} = DC \times (V_{IN}\text{-}V_{SW}) / (f \times L) \quad (9)$$

Combining all terms, an expression can be developed which allows the maximum available load current to be calculated:

$$I_{LOAD}(max) = (1-DC) \times \left(I_{SW}(max) - \frac{DC(V_{IN} - V_{SW})}{2fL} \right) \quad (10)$$

The equation shown to calculate maximum load current takes into account the losses in the inductor or turn-OFF switching losses of the FET and diode. For actual load current in typical applications, we took bench data for various input and output voltages for both the "X" and "Y" versions of the LM2731 and displayed the maximum load current available for a typical device in graph form:

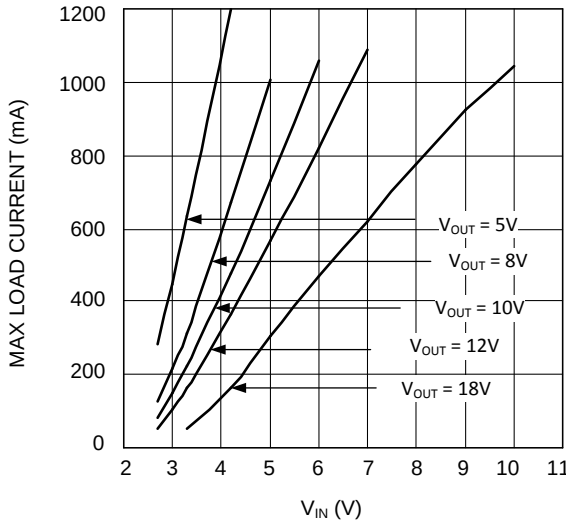


Figure 30. Maximum Load Current (Typical) vs V_{IN} - X Option

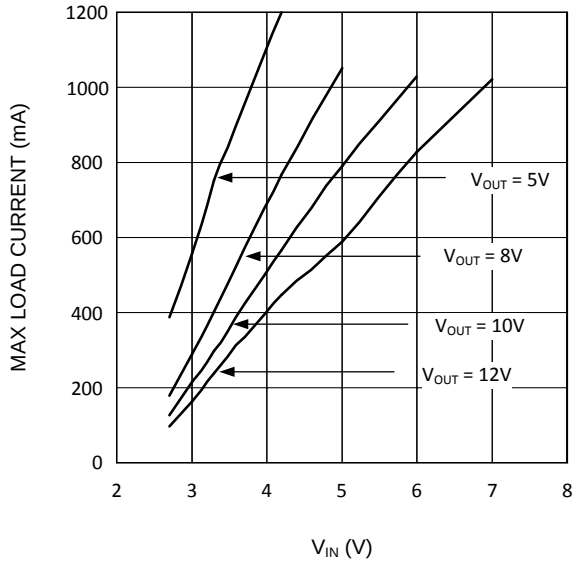


Figure 31. Maximum Load Current (Typical) vs V_{IN} - Y Option

8.2.2.12 Design Parameters V_{SW} and I_{SW}

The value of the FET "ON" voltage (referred to as V_{SW} in the equations) is dependent on load current. A good approximation can be obtained by multiplying the "ON-Resistance" of the FET times the average inductor current.

FET on resistance increases at V_{IN} values less than 5 V, since the internal N-FET has less gate voltage in this input voltage range (see *Typical Characteristics* curves). Above V_{IN} = 5V, the FET gate voltage is internally clamped to 5V.

The maximum peak switch current the device can deliver is dependent on duty cycle. For higher duty cycles, see *Typical Characteristics*.

8.2.2.13 Inductor Suppliers

Recommended suppliers of inductors for this product include, but are not limited to Sumida, Coilcraft, Panasonic, TDK, and Murata. When selecting an inductor, make certain that the continuous current rating is high enough to avoid saturation at peak currents. A suitable core type must be used to minimize core (switching) losses, and wire power losses must be considered when selecting the current rating.

8.2.3 Application Curves

See *Typical Characteristics*.

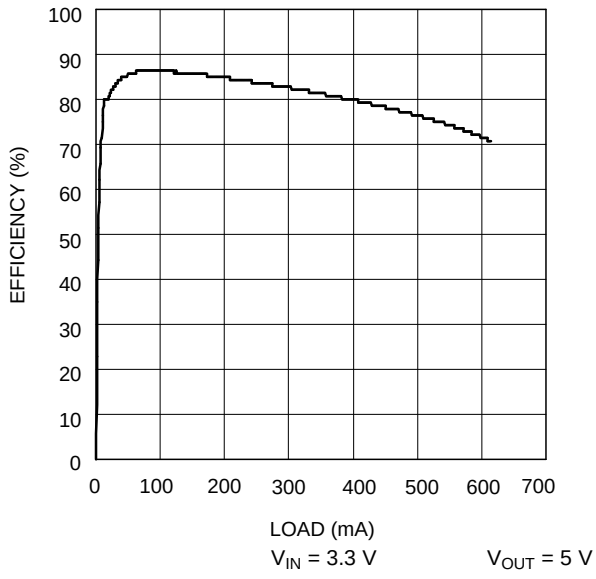


Figure 32. Efficiency vs Load Current - X Option

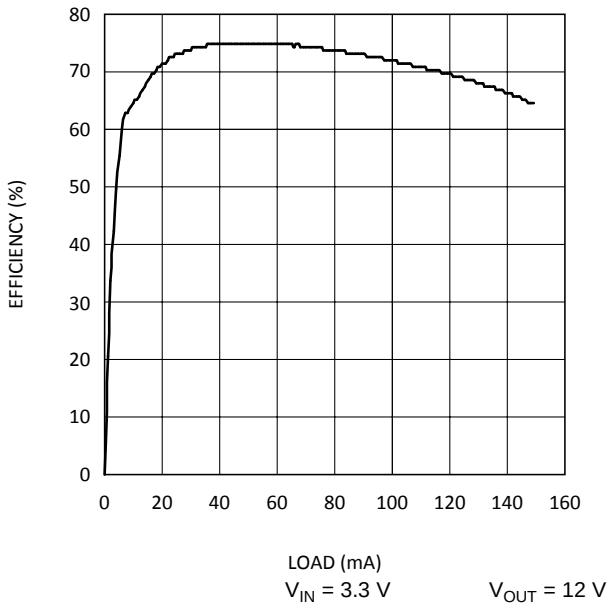


Figure 33. Efficiency vs Load Current - X Option

8.3 System Examples

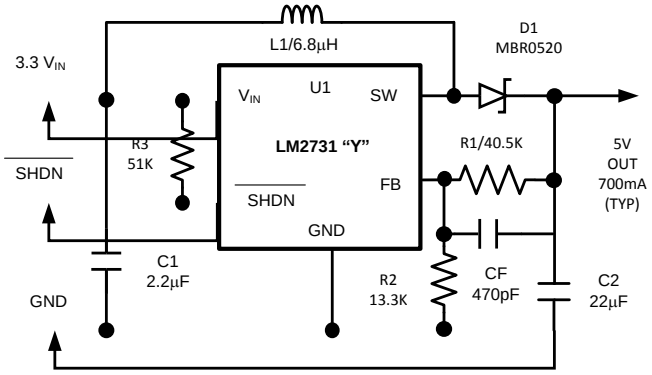


Figure 34. VIN = 3.3 V, VOUT = 5 V at 700 mA

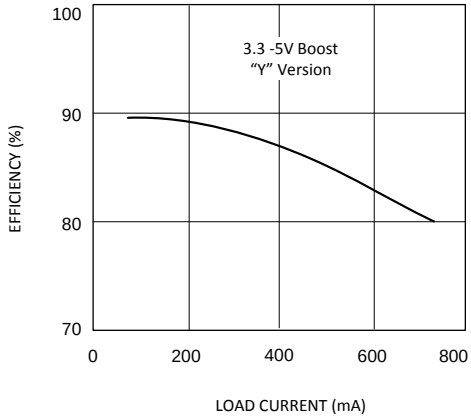


Figure 35. Efficiency vs Load Current

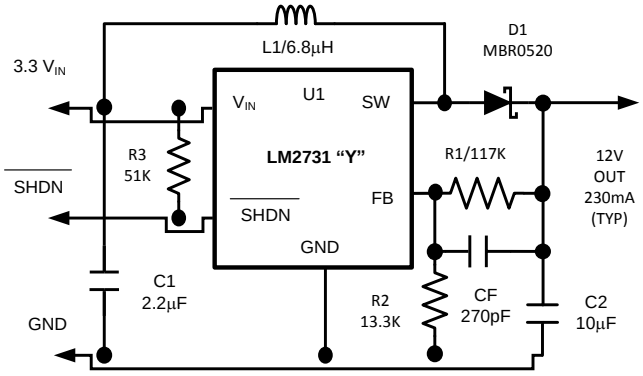


Figure 36. VIN = 3.3 V, VOUT = 12 V at 230 mA

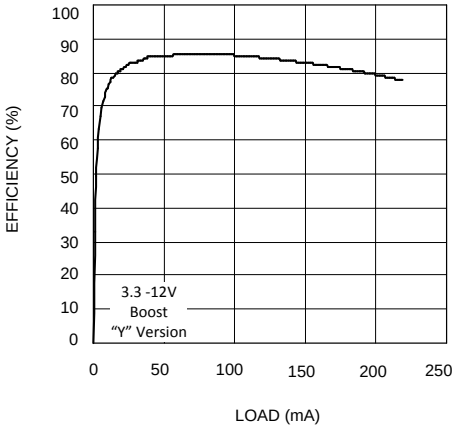


Figure 37. Efficiency vs Load Current

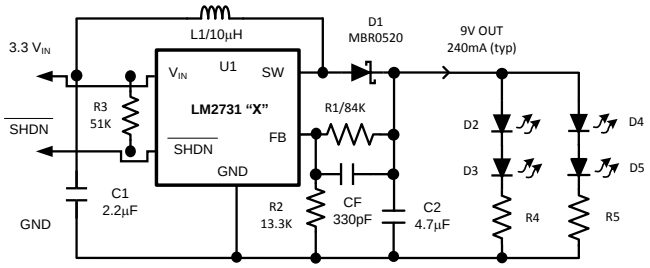


Figure 38. VIN = 3.3 V, VOUT = 9 V at 240 mA

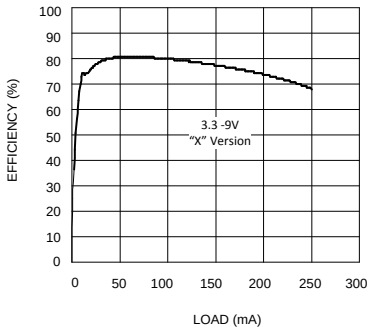


Figure 39. Efficiency vs Load Current

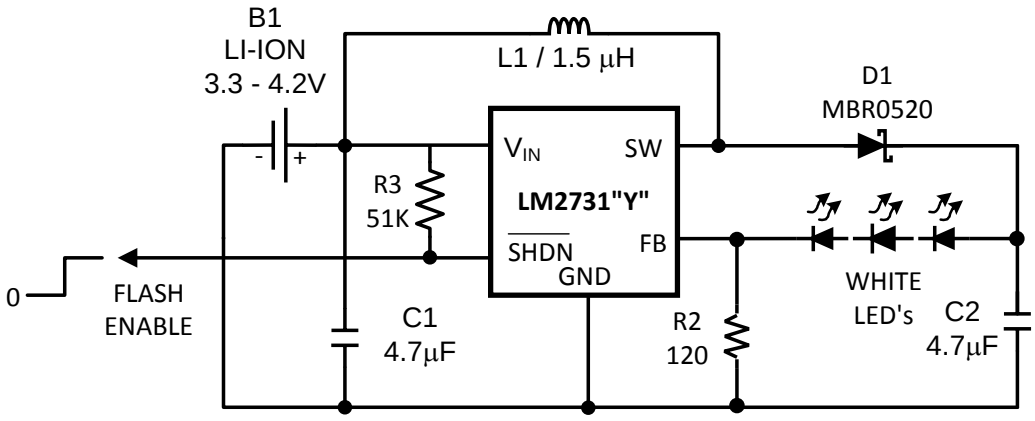


Figure 40. White LED Flash Application

9 Power Supply Recommendations

The LM2731 device is designed to operate from various DC power supplies. The impedance of the input supply rail should be low enough that the input current transient does not cause a drop below SHUTDOWN level. If the input supply is connected by using long wires, additional bulk capacitance may be required in addition to normal input capacitor.

10 Layout

10.1 Layout Guidelines

High-frequency switching regulators require very careful layout of components to get stable operation and low noise. All components must be as close as possible to the LM2731 device. TI recommends that a 4-layer PCB be used so that internal ground planes are available.

As an example, a recommended layout of components is shown in Figure 41.

Some additional guidelines to be observed:

- Keep the path between L1, D1, and C2 extremely short. Parasitic trace inductance in series with D1 and C2 will increase noise and ringing.
- The feedback components R1, R2 and CF must be kept close to the FB pin of U1 to prevent noise injection on the FB pin trace.
- If internal ground planes are available (recommended), use vias to connect directly to ground at pin 2 of U1, as well as the negative sides of capacitors C1 and C2.

10.2 Layout Example

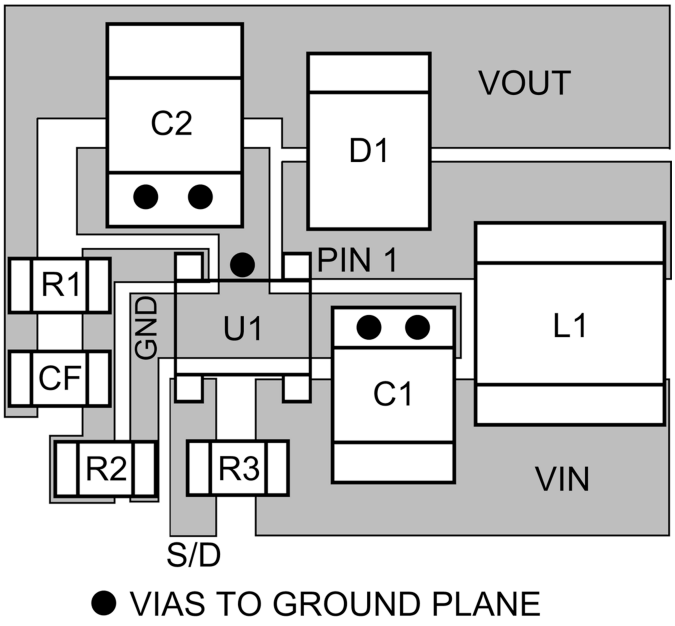


Figure 41. Recommended PCB Component Layout

10.3 Thermal Considerations

At higher duty cycles, the increased ON-time of the FET means the maximum output current will be determined by power dissipation within the LM2731 FET switch. The switch power dissipation from ON-state conduction is calculated by:

$$P_{(SW)} = DC \times I_{IND}(AVE)^2 \times R_{DS}(ON) \quad (11)$$

There will be some switching losses as well, so some derating needs to be applied when calculating IC power dissipation.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2731XMF	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	S51A	
LM2731XMF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	S51A	Samples
LM2731XMFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	S51A	Samples
LM2731YMF	ACTIVE	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	S51B	Samples
LM2731YMF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	S51B	Samples
LM2731YMFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	S51B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

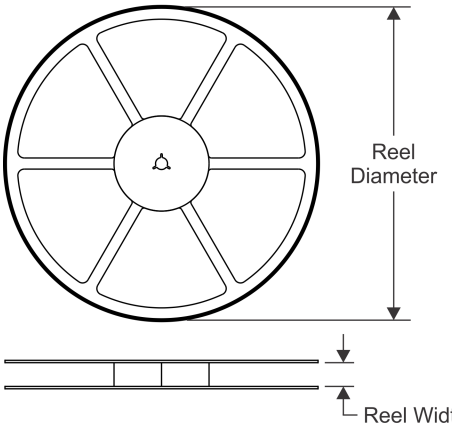
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

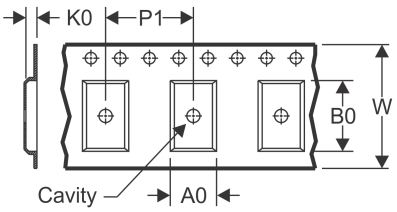
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

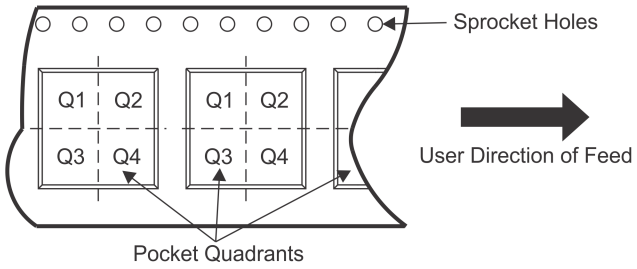


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

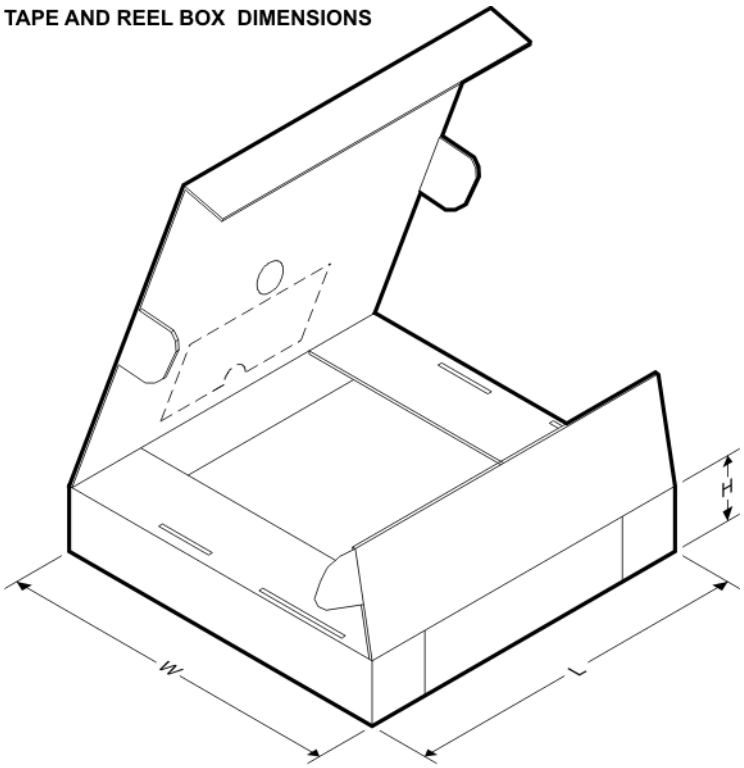
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2731XMF	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2731XMF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2731XMFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2731YMF	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2731YMF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2731YMFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

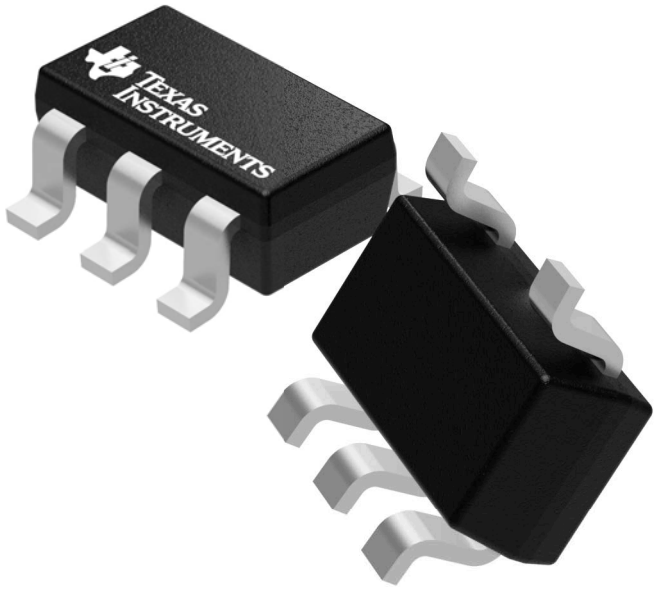


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2731XMF	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM2731XMF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM2731XMFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LM2731YMF	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM2731YMF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM2731YMFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

DBV 5 SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



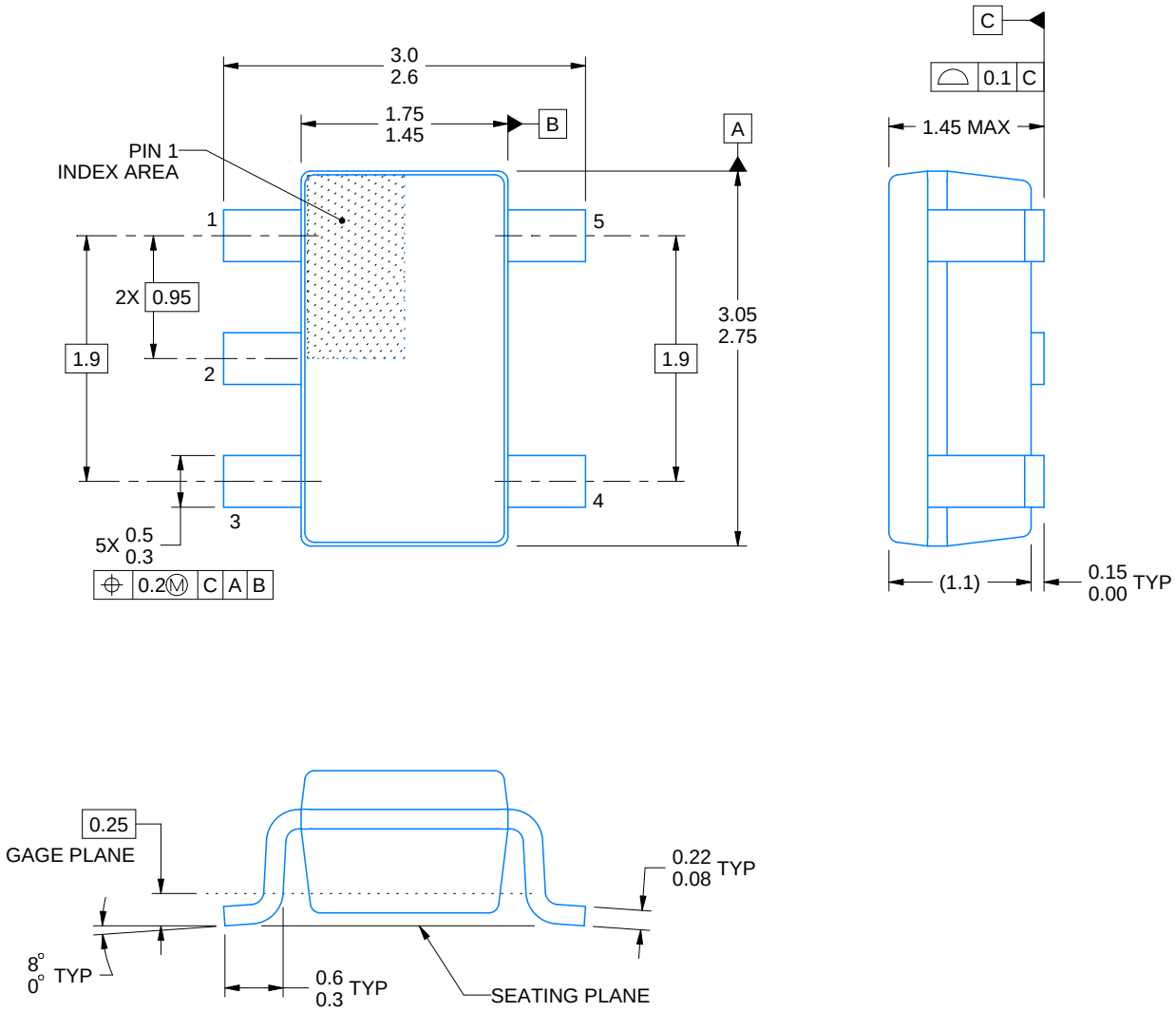
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

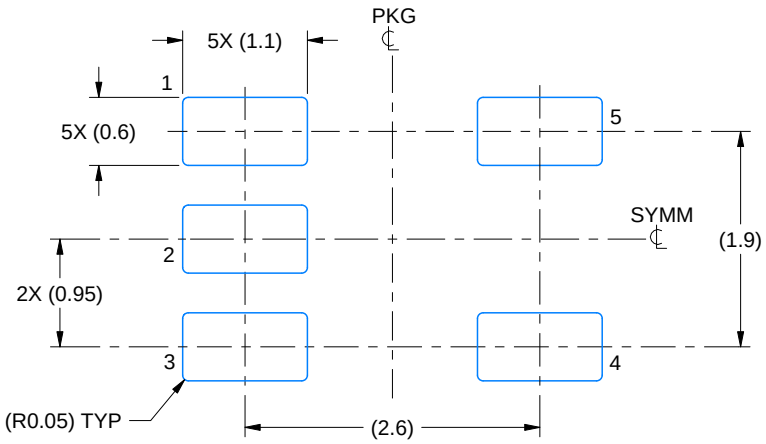
SMALL OUTLINE TRANSISTOR



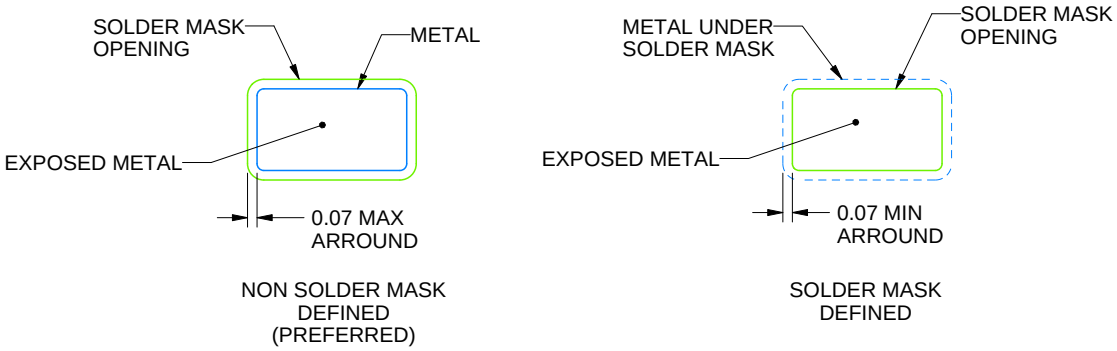
4214839/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

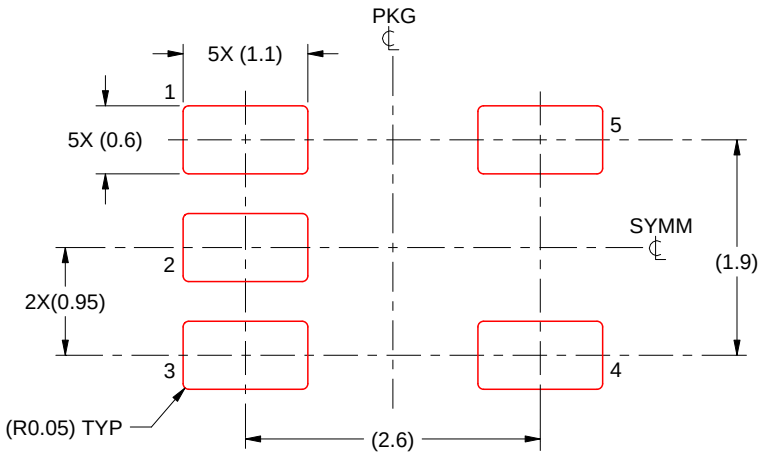


SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

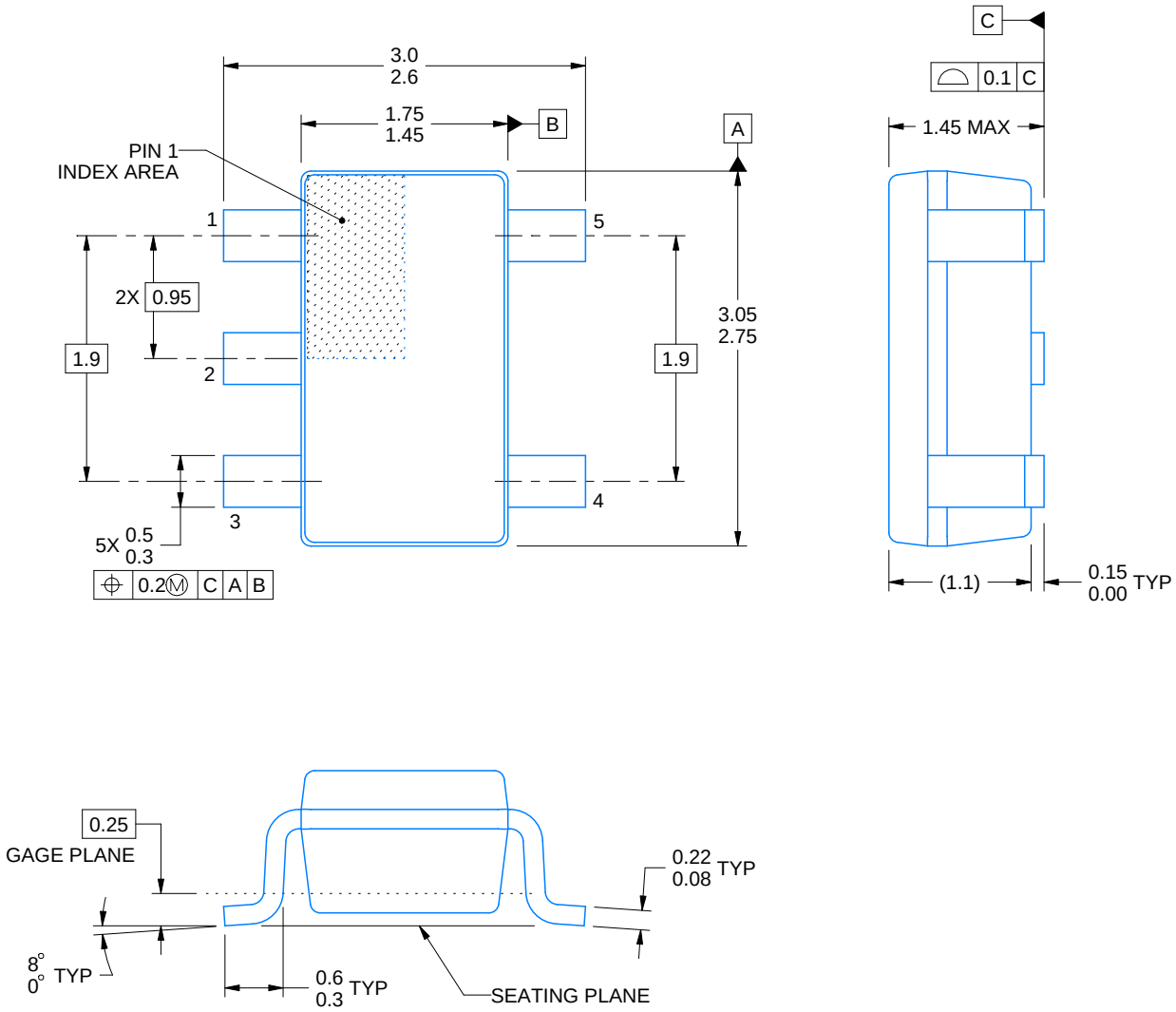
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

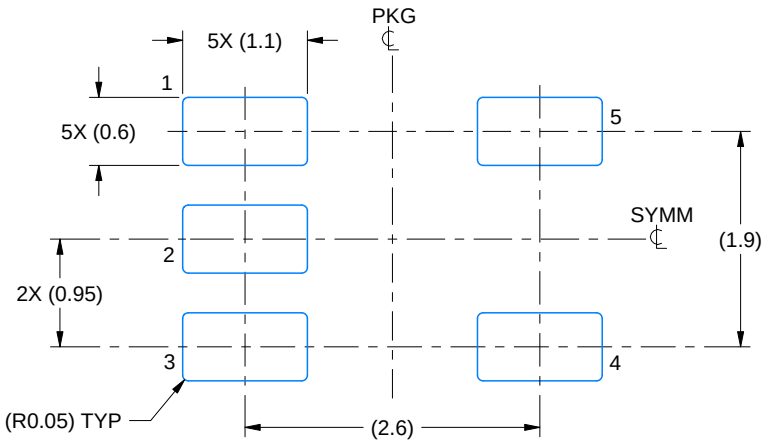
SMALL OUTLINE TRANSISTOR



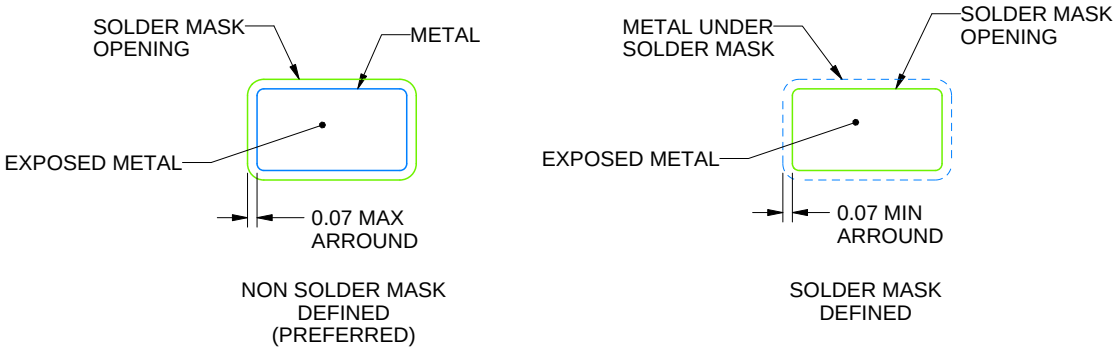
4214839/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

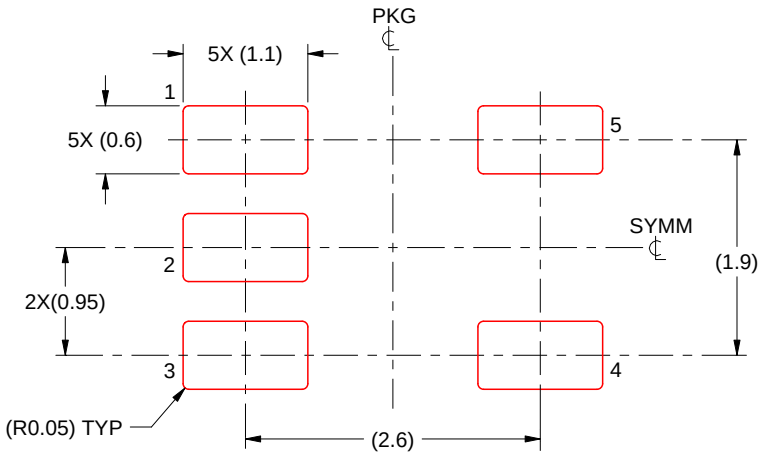


SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

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7. Board assembly site may have different recommendations for stencil design.

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