SH79F3252

Enhanced 8051 Microcontroller with 10bit ADC and LCD

1. Features

- 8 bits micro-controller with Pipe-line structured 8051 compatible instruction set
- Flash ROM: 32K Bytes
- RAM: internal 256 Bytes, external 1280 Bytes, LCD, RAM 32 Bytes
- EEPROM-Like: bulid-in 4096 Bytes (code option)
- Operation Voltage: 1.8V - 3.6V
- Oscillator (code option):
  - Crystal oscillator: 32.768kHz
  - Internal oscillator: Internal RC = 128KHz
  - Internal oscillator: Internal RC = 8MHz
- 45 CMOS bi-directional I/O pins
- Built-in pull-up resistor for I/O
- Three 16-bit timer/counters: T2, T3, T5
- one 12-bit Pulse Width Modulation (PWM1)
- the remote carrier generator
- 45 I/O with 20mA sink current
- 1 One I/O with 450mA sink current, act as remote control
- Powerful interrupt sources:
  - INT0, 2, 3
  - INT4: 8 input
  - Timer 2, 3, 5
  - PWM1, REM
  - ADC, EUART0, SCM, LPD
- 9 analog inputs 12-bit Analog Digital Converter, with comparator function built-in
- EUART
- LCD driver: (Resistor and Capacitor Mode)
  - 4 X 32 dots (1/4 duty, 1/3 bias)
  - 5 X 31 dots (1/5 duty, 1/3 bias)
- Built-in low voltage Reset (LVR) function:
  - LVR voltage:1.9V
- Low Power Detect (LPD) Module with 11 level optional
- Support single line or four line singsimulation and download
- CPU Machine period:
  - 1 oscillator clock
- Built-in Watch Dog Timer (WDT)
- Built-in oscillator Warm-up timer
- Support Low power operation modes:
  - Idle Mode
  - Power-Down Mode
- Flash Type
- Package:
  - TQFP48 Pin

2. General Description

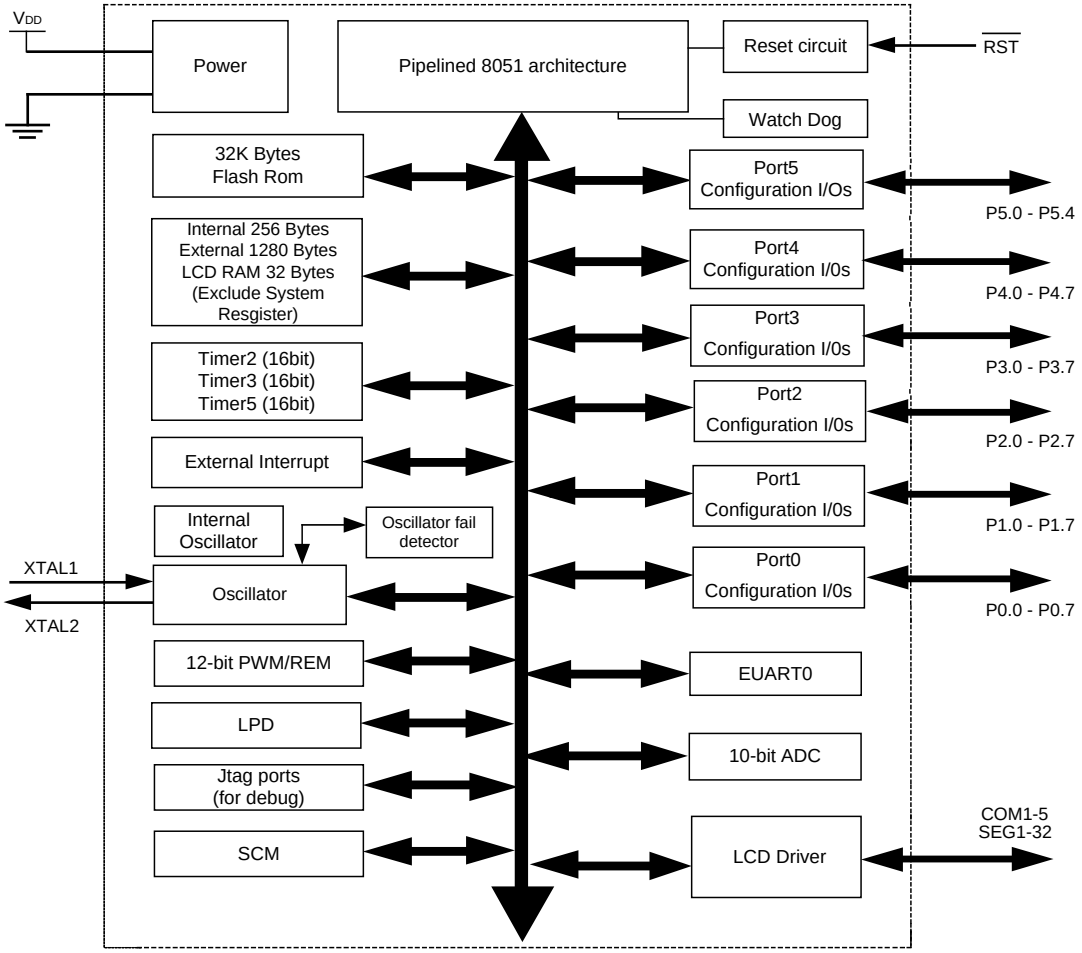
The SH79F3252 is a high performance 8051 compatible micro-controller. The SH79F3252 can perform more fast operation speed and higher calculation performance, if compare SH79F3252 with standard 8051 at same clock speed.

The SH79F3252 retains most features of the standard 8051. These features include internal 256 bytes RAM, UART, INT0, INT2, INT3 and INT4 (8 input). In addition, SH79F3252 provides external 1280 bytes RAM, It also contains 32K bytes Flash memory block for program storage. The SH79F3252 also embeds 4096 bytes EEPROM-like for program data after system power off.

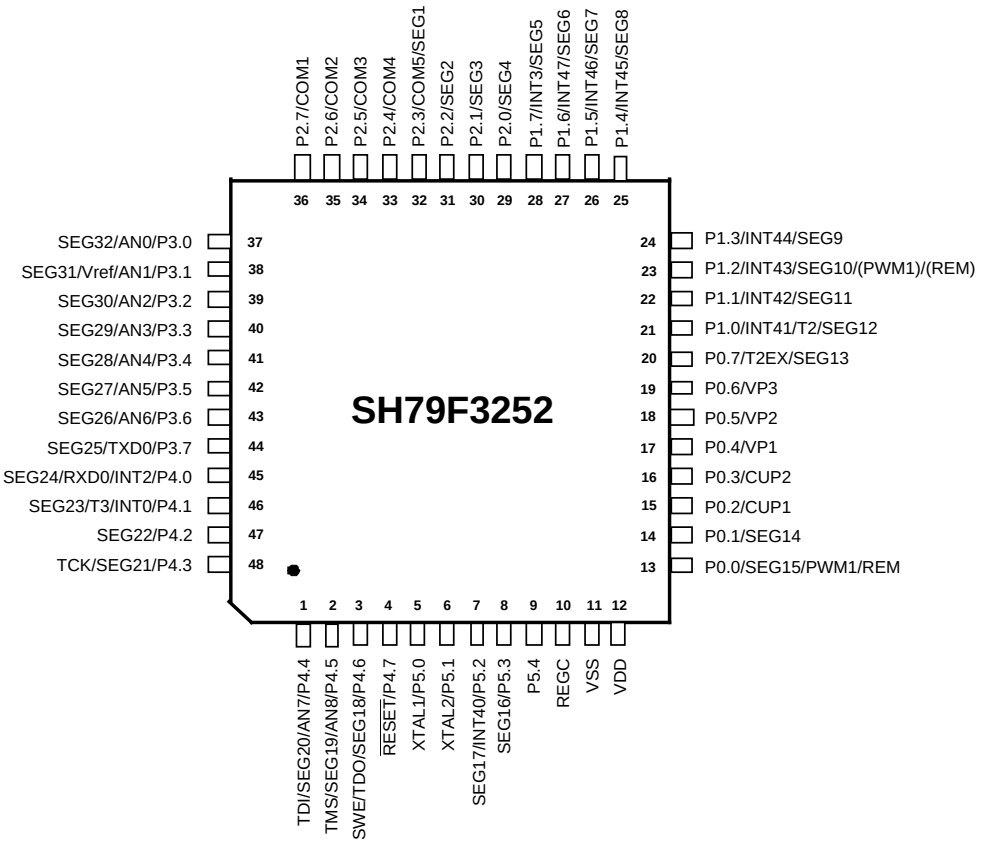
In addition, the SH79F3252 builds in UART standard communication module, LCD voltage regulator circuit, capacitor bias circuit, resistor bias circuit, 10 bit ADC and PWM, etc.

For high reliability and low cost issues, the SH79F3252 builds in Watchdog Timer, Low Voltage Reset function and system clock monitor. And SH79F3252 also supports two power saving modes to reduce power consumption.

3. Block Diagram



4. Pin Configration



Pin Configuration Diagram

Total: 48 PIN

Note:

REGC must be externally connected to 0.47uF -1uF capacitance to GND.

The out most pin function has the highest priority, and the inner most pin function has the lowest priority (Refer to Pin Configuration Diagram. This means when one pin is occupied by a higher priority function (if enabled) cannot be used as the lower priority functional pin, even when the lower priority function is also enabled. Until the higher priority function is closed by software, can the corresponding pin be released for the lower priority function use.

Table 4.1 Pin Function

Pin No.	Pin Name	Default Function	Pin No.	Pin Name	Default Function
1	TDI/SEG20/AN7/P4.4	P4.4	25	SEG8/INT45/P1.4	P1.4
2	TMS/SEG19/AN8/P4.5	P4.5	26	SEG7/INT46/P1.5	P1.5
3	SWE/TDO/SEG18/P4.6	P4.6	27	SEG6/INT47/P1.6	P1.6
4	$\overline{\text{RESET}}$/P4.7	P4.7	28	SEG5/INT3/P1.7	P1.7
5	XTAL1/P5.0	P5.0	29	SEG4/P2.0	P2.0
6	XTAL2/P5.1	P5.1	30	SEG3/P2.1	P2.1
7	SEG17/INT40/P5.2	P5.2	31	SEG2/P2.2	P2.2
8	SEG16/P5.3	P5.3	32	SEG1/COM5/P2.3	P2.3
9	P5.4	P5.4	33	COM4/P2.4	P2.4
10	REGC	REGC	34	COM3/P2.5	P2.5
11	VSS	VSS	35	COM2/P2.6	P2.6
12	VDD	VDD	36	COM1/P2.7	P2.7
13	REM/PWM1/SEG15/P0.0	P0.0	37	SEG32/AN0/P3.0	P3.0
14	SEG14/P0.1	P0.1	38	SEG31/Vref/AN1/P3.1	P3.1
15	CUP1/P0.2	P0.2	39	SEG30/AN2/P3.2	P3.2
16	CUP2/P0.3	P0.3	40	SEG29/AN3/P3.3	P3.3
17	VP1/P0.4	P0.4	41	SEG28/AN4/P3.4	P3.4
18	VP2/P0.5	P0.5	42	SEG27/AN5/P3.5	P3.5
19	VP3/P0.6	P0.6	43	SEG26/AN6/P3.6	P3.6
20	SEG13/T2EX/P0.7	P0.7	44	SEG25/TXD0/P3.7	P3.7
21	SEG12/T2/INT41/P1.0	P1.0	45	SEG24/RXD0/INT2/P4.0	P4.0
22	SEG11/INT42/P1.1	P1.1	46	SEG23/T3/INT0/P4.1	P4.1
23	SEG10 /INT43/P1.2	P1.2	47	SEG22/P4.2	P4.2
24	SEG9/INT44/P1.3	P1.3	48	TCK/SEG21/P4.3	P4.3

5. Pin Description

Pin No.	Type	Description
PORT		
P0.0 - P0.7	I/O	8 bit General purpose CMOS I/O
P1.0 - P1.7	I/O	8 bit General purpose CMOS I/O
P2.0 - P2.7	I/O	8 bit General purpose CMOS I/O
P3.0 - P3.7	I/O	8 bit General purpose CMOS I/O
P4.0 - P4.7	I/O	8 bit General purpose CMOS I/O
P5.0 - P5.4	I/O	5 bit General purpose CMOS I/O
Timer		
T2	I/O	Timer2 external input
T2EX	I	Timer2 auto-reload /capture/direction control
T3	I/O	Timer3 external input
EUART		
RXD0	I	EUART0 data input
TXD0	O	EUART0 data output
ADC		
AN0 - AN8	O	ADC input pin
V_{REF}	O	External ADC reference voltage input
PWM		
PWM1	O	PWM1 output pin
REM		
REM	O	Telecontrol carrier generator
LCD		
COM1 - COM4/5	O	Common signal output for LCD display
SEG1/2 - SEG32	O	Segment signal output for LCD display
LCD Capacitance Driver		
CUP1	P	Connection for LCD bias capacitor
CUP2	P	Connection for LCD bias capacitor
VP3	P	LCD Power
VP2	P	LCD Power
VP1	P	LCD Power

(to be continued)

(continue)

Interrupt & Reset & Clock & Power		
INT0	I	External interrupt0
INT2	I	External interrupt2
INT3	I	External interrupt3
INT40 - INT47	I	External interrupt40 - 47
$\overline{\text{RESET}}$	I	The device will be reset by A low voltage on this pin longer than 10us, an internal resistor about 50kΩ to V_{DD}, So using only an external capacitor to GND can cause a power-on reset
XTAL1	I	Low frequency Oscillator input
XTAL2	O	Low frequency Oscillator output
GND	P	Ground
V_{DD}	P	Power supply
REGC	P	*must be externally connected to 0.47 uF -1Uf capacitance to GND.*
Programming Port		
SWE (P4.6)	I/O	One line Debug interface, if the power on or power off slope of chip VDD is greater than 500ms/v, it is recommended to connect the 47K-1M cathode to GND or VDD to increase the stability of the chip.
TDO (P4.6)	O	Debug interface: Test data out
TMS (P4.5)	I	Debug interface: Test mode select
TDI (P4.4)	I	Debug interface: Test data in
TCK (P4.3)	I	Debug interface: Test clock in
Note: *When P4.3 - P4.6 used as debug interface, functions of P4.3 - P4.6 are blocked.*		

6. SFR Mapping

The SH79F3252 provides 256 bytes of internal RAM which contain general-purpose data memory and Special Function Register (SFR). The SFRs of the SH79F3252 are categoried as below:

CPU Core Registers:	ACC, B, PSW, SP, DPL, DPH
Enhanced CPU Core Registers:	AUXC, DPL1, DPH1, INSCON
Power and Clock Control Registers:	PCON, SUSLO
Flash Registers:	IB_OFFSET, IB_DATA, IB_CON1, IB_CON2, IB_CON3, IB_CON4, IB_CON5, FLASHCON
Data Memory Register:	XPAGE
Hardware Watchdog Timer Registers:	RSTSTAT, LPDCON
System Clock Control Register:	CLKCON
Interrupt System Registers:	IEN0, IEN1, EXF0, EXF1, IPH0, IPL0, IPH1, IPL1, IENC, EXCON, TCON
I/O Port Registers:	P0, P1, P2, P3, P4, P5, P0CR, P1CR, P2CR, P3CR, P4CR, P5CR, P0PCR, P1PCR, P2PCR, P3PCR, P4PCR, P5PCR
Timer Registers:	T2CON, T2MOD, TL2, TH2, RCAP2L, RCAP2H, T3CON, TL3, TH3, T5CON, TL5, TH5
EUART Registers:	SCON, SBUF, SADEN, SADDR, PCON, SBRTH, SBRTL, SFINE, UTOS
ADC Registers:	ADCON, ADCON1, ADT, ADCH1, ADCH2, ADDL, ADDH
LCD Registers:	LCDCON, P1SS, P2SS, P3SS, P4SS, P5SS, P0SS, LCDCON1, DISPCLK0, DISPCLK1
PWM Registers:	PWM1CON, PWM1PL, PWM1PH, PWM1DL, PWM1DH
REM Registers:	REMCON, REMNUMH, REMNUML

Table 6.1 CPU Core SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ACC	E0H	Accumulator	00000000	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
B	F0H	B Register	00000000	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
AUXC	F1H	AUXC Register	00000000	C.7	C.6	C.5	C.4	C.3	C.2	C.1	C.0
PSW	D0H	Program Status Word	00000000	CY	AC	F0	RS1	RS0	OV	F1	P
SP	81H	Stack Pointer	00000111	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0
DPL	82H	Data Pointer Low byte	00000000	DPL0.7	DPL0.6	DPL0.5	DPL0.4	DPL0.3	DPL0.2	DPL0.1	DPL0.0
DPH	83H	Data Pointer High byte	00000000	DPH0.7	DPH0.6	DPH0.5	DPH0.4	DPH0.3	DPH0.2	DPH0.1	DPH0.0
DPL1	84H	Data Pointer 1 Low byte	00000000	DPL1.7	DPL1.6	DPL1.5	DPL1.4	DPL1.3	DPL1.2	DPL1.1	DPL1.0
DPH1	85H	Data Pointer 1 High byte	00000000	DPH1.7	DPH1.6	DPH1.5	DPH1.4	DPH1.3	DPH1.2	DPH1.1	DPH1.0
INSCON	86H	Data pointer select	-0--00-0	-	BKS0	-	-	DIV	MUL	-	DPS

Table 6.2 Data Memory SFR

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
XPAGE	F7H	Data Memory	-----000	-	-	-	-	-	XPAGE.2	XPAGE.1	XPAGE.0

Table 6.3 Power and Clock control SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCON	87H	Power Control	00--0000	SMOD	SSTAT	-	-	GF1	GF0	PD	IDL
SUSLO	8EH	Suspend Mode Control	00000000	SUSLO.7	SUSLO.6	SUSLO.5	SUSLO.4	SUSLO.3	SUSLO.2	SUSLO.1	SUSLO.0

Table 6.4 Flash Control SFR

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_OFF SET	FBH	Offset Register for Programming	00000000	IB_OFF SET.7	IB_OFF SET.6	IB_OFF SET.5	IB_OFF SET.4	IB_OFF SET.3	IB_OFF SET.2	IB_OFF SET.1	IB_OFF SET.0
IB_DATA	FCH	Data Register for Programming	00000000	IB_DATA.7	IB_DATA.6	IB_DATA.5	IB_DATA.4	IB_DATA.3	IB_DATA.2	IB_DATA.1	IB_DATA.0
IB_CON1	F2H	Flash Memory Control Register	00000000	IB_CON1.7	IB_CON1.6	IB_CON1.5	IB_CON1.4	IB_CON1.3	IB_CON1.2	IB_CON1.1	IB_CON1.0
IB_CON2	F3H	Flash Memory Control Register1	----0000	-	-	-	-	IB_CON2.3	IB_CON2.2	IB_CON2.1	IB_CON2.0
IB_CON3	F4H	Flash Memory Control Register2	----0000	-	-	-	-	IB_CON3.3	IB_CON3.2	IB_CON3.1	IB_CON3.0
IB_CON4	F5H	Flash Memory Control Register3	----0000	-	-	-	-	IB_CON4.3	IB_CON4.2	IB_CON4.1	IB_CON4.0
IB_CON5	F6H	Flash Memory Control Register4	----0000	-	-	-	-	IB_CON5.3	IB_CON5.2	IB_CON5.1	IB_CON5.0
XPAGE	F7H	Memory Page	-0000000	-	XPAGE.6	XPAGE.5	XPAGE.4	XPAGE.3	XPAGE.2	XPAGE.1	XPAGE.0
FLASHCON	A7H	Flash access control	-------0	-	-	-	-	-	-	-	FAC

Table 6.5 WDT SFR

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RSTSTAT	B1H	Watchdog Timer Control	u-uuu000*	WDOF	-	PORF	LVRF	CLRF	WDT.2	WDT.1	WDT.0

***Note:** RSTSTAT initial value is determined by different RESET.*

Table 6.6 CLKCON SFR

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CLKCON	B2H	System Clock Control Register	1110000-	32K_SPDUP	CLKS1	CLKS0	SCMIF	HFON	FS	AHUM	-

Table 6.7 Interrupt SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IEN0	A8H	Interrupt Enable Control0	00000-0-	EA	EADC	ET2	ES0	ET5	-	EX2	-
IEN1	A9H	Interrupt Enable Control1	00000000	ESCM	EPWM1	ELPD	ET3	EX4	EX3	EREM	EX0
IPL0	B8H	Interrupt Priority Control Low0	-0000-0-	-	PADCL	PT2L	PS0L	PT5L	-	PX2L	-
IPH0	B4H	Interrupt Priority Control High0	-0000-0-	-	PADCH	PT2H	PS0H	PT5H	-	PX2H	-
IPL1	B9H	Interrupt Priority Control Low1	00000000	PSCML	PPWM1L	PLPDL	PT3L	PX4L	PX3L	PREML	PX0L
IPH1	B5H	Interrupt Priority Control High1	00000000	PSCMH	PPWM1L	PLPDH	PT3H	PX4H	PX3H	PREMH	PX1H

(to be continued)

(continue)

EXF0	E8H	External interrupt Control 0	00000000	IT4.1	IT4.0	IT3.1	IT3.0	IT2.1	IT2.0	IE3	IE2
IENC	BAH	Interrupt 4 channel enable control	00000000	EXS47	EXS46	EXS45	EXS44	EXS43	EXS42	EXS41	EXS40
EXF1	D8H	External interrupt Contro1	00000000	IF47	IF46	IF45	IF44	IF43	IF42	IF41	IF40
EXCON	C7H	External interrupt Sampling	----0000	-	-	-	-	I0PS1	I0PS0	I0SN1	I0SN0
TCON	88H	External interrupt0 Control	------00	-	-	-	-	-	-	IE0	IT0

Table 6.8 Port SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0	80H	8-bit Port0	00000000	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
P1	90H	8-bit Port1	00000000	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
P2	A0H	8-bit Port2	00000000	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
P3	B0H	8-bit Port3	00000000	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
P4	C0H	8-bit Port4	00000000	P4.7	P4.6	P4.5	P4.4	P4.3	P4.2	P4.1	P4.0
P5	F8H	5-bit Port5	---00000	-	-	-	P5.4	P5.3	P5.2	P5.1	P5.0
P0CR	E1H	Port0 input/output direction control	00000000	P0CR.7	P0CR.6	P0CR.5	P0CR.4	P0CR.3	P0CR.2	P0CR.1	P0CR.0
P1CR	E2H	Port1 input/output direction control	00000000	P1CR.7	P1CR.6	P1CR.5	P1CR.4	P1CR.3	P1CR.2	P1CR.1	P1CR.0
P2CR	E3H	Port2 input/output direction control	00000000	P2CR.7	P2CR.6	P2CR.5	P2CR.4	P2CR.3	P2CR.2	P2CR.1	P2CR.0
P3CR	E4H	Port3 input/output direction control	00000000	P3CR.7	P3CR.6	P3CR.5	P3CR.4	P3CR.3	P3CR.2	P3CR.1	P3CR.0
P4CR	E5H	Port4 input/output direction control	00000000	P4CR.7	P4CR.6	P4CR.5	P4CR.4	P4CR.3	P4CR.2	P4CR.1	P4CR.0
P5CR	E6H	Port5 input/output direction control	---00000	-	-	-	P5CR.4	P5CR.3	P5CR.2	P5CR.1	P5CR.0
P0PCR	E9H	Internal pull-high enable for Port0	00000000	P0PCR.7	P0PCR.6	P0PCR.5	P0PCR.4	P0PCR.3	P0PCR.2	P0PCR.1	P0PCR.0
P1PCR	EAH	Internal pull-high enable for Port1	00000000	P1PCR.7	P1PCR.6	P1PCR.5	P1PCR.4	P1PCR.3	P1PCR.2	P1PCR.1	P1PCR.0
P2PCR	EBH	Internal pull-high enable for Port2	00000000	P2PCR.7	P2PCR.6	P2PCR.5	P2PCR.4	P2PCR.3	P2PCR.2	P2PCR.1	P2PCR.0
P3PCR	ECH	Internal pull-high enable for Port3	00000000	P3PCR.7	P3PCR.6	P3PCR.5	P3PCR.4	P3PCR.3	P3PCR.2	P3PCR.1	P3PCR.0
P4PCR	EDH	Internal pull-high enable for Port4	00000000	P4PCR.7	P4PCR.6	P4PCR.5	P4PCR.4	P4PCR.3	P4PCR.2	P4PCR.1	P4PCR.0
P5PCR	EEH	Internal pull-high enable for Port5	---00000	-	-	-	P5PCR.4	P5PCR.3	P5PCR.2	P5PCR.1	P5PCR.0
UTOS	9FH	TTL logical selection register	-----00	-	-	-	-	-	-	ES1	ES0

Table 6.9 Timer SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T2CON	C8H	Timer/Counter 2 Control	00--0000	TF2	EXF2	-	-	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
T2MOD	C9H	Timer/Counter 2 Mode	0-----00	TCLKP2	-	-	-	-	-	T2OE	DCEN
RCAP2L	CAH	Timer/Counter 2 Reload /Caprure Low Byte	00000000	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0
RCAP2H	CBH	Timer/Counter 2 Reload /Caprure High Byte	00000000	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0
TL2	CCH	Timer/Counter 2 Low Byte	00000000	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0
TH2	CDH	Timer/Counter 2 High Byte	00000000	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0
T3CON	CEH	Timer/Counter 3 Control	0-00-000	TF3	-	T3PS1	T3PS0	-	TR3	T3CLKS1	T3CLKS0
TL3	91H	Timer/Counter 3 Low Byte	00000000	TL3.7	TL3.6	TL3.5	TL3.4	TL3.3	TL3.2	TL3.1	TL3.0
TH3	92H	Timer/Counter 3 High Byte	00000000	TH3.7	TH3.6	TH3.5	TH3.4	TH3.3	TH3.2	TH3.1	TH3.0
T5CON	C6H	Timer/Counter 5 Control	0-00--0-	TF5	-	T5PS1	T5PS0	-	-	TR5	-
TL5	C4H	Timer/Counter 5 Low Byte	00000000	TL5.7	TL5.6	TL5.5	TL5.4	TL5.3	TL5.2	TL5.1	TL5.0
TH5	C5H	Timer/Counter 5 High Byte	00000000	TH5.7	TH5.6	TH5.5	TH5.4	TH5.3	TH5.2	TH5.1	TH5.0

Table 6.10 EUART SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCON	98H	Serial Control	00000000	SM0/FE	SM1/RXOV	SM2/TXCOL	REN	TB8	RB8	TI	RI
SBUF	99H	Serial Data Buffer	00000000	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0
SADDR	9AH	Slave Address	00000000	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0
SADEN	9BH	Slave Address Mask	00000000	SADEN.7	SADEN.6	SADEN.5	SADEN.4	SADEN.3	SADEN.2	SADEN.1	SADEN.0
PCON	87H	Power and Serial Control	00--0000	SMOD	SSTAT	-	-	GF1	GF0	PD	IDL
SBRTH	9CH	Baud Rate Generator High Byte	00000000	SBRTEN	SBRT.14	SBRT.13	SBRT.12	SBRT.11	SBRT.10	SBRT.9	SBRT.8
SBRTL	9DH	Baud Rate Generator Low Byte	00000000	SBRT.7	SBRT.6	SBRT.5	SBRT.4	SBRT.3	SBRT.2	SBRT.1	SBRT.0
SFINE	9EH	Baud Rate Generator (Fine tuning)	----0000	-	-	-	-	SFINE.3	SFINE.2	SFINE.1	SFINE.0

Table 6.11 ADC SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCON	93H	ADC Control	0000---0	ADON	ADCIF	EC	REFC	-	-	-	GO/$\overline{\text{DONE}}$
ADCON1	8FH	ADC Control 1	000-0000	VBG	ALR	ADCPUMP	-	SCH3	SCH2	SCH1	SCH0
ADT	94H	ADC Time Configuration	00000000	TADC7	TADC6	TADC5	TADC4	TADC3	TADC2	TADC1	TADC0
ADCH1	95H	ADC Channel Configuration1	00000000	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
ADCH2	C2H	ADC Channel Configuration2	-------0	-	-	-	-	-	-	-	CH8
ADDL	96H	ADC Data Low Byte	00------	A1	A0	-	-	-	-	-	-
ADDH	97H	ADC Data High Byte	00000000	A9	A8	A7	A6	A5	A4	A3	A2

Table 6.12 LCD SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LCDCON1	AAH	LCD Control1	--00-000	-	-	FCCTL1	FCCTL0	-	RLCD	MOD1	MOD0
LCDCON	ABH	LCD Control	00000000	LCDON	LCDSEL	DUTY	TYPESEL	VOL3	VOL2	VOL1	VOL0
DISPCLK0	E7H	LCD Clock Control register	------00	-	-	-	-	-	-	DCK1	DCK1
P0SS	BFH	P0 mode Select	0-----00	P0S7	-	-	-	-	-	P0S1	P0S0
P1SS	ADH	P1 mode Select	00000000	P1S7	P1S6	P1S5	P1S4	P1S3	P1S2	P1S1	P1S0
P2SS	BBH	P2 mode Select	00000000	P2S7	P2S6	P2S5	P2S4	P2S3	P2S2	P2S1	P2S0
P3SS	BCH	P3 mode Select	00000000	P3S7	P3S6	P3S5	P3S4	P3S3	P3S2	P3S1	P3S0
P4SS	BDH	P4 mode Select	-0000000	-	P4S6	P4S5	P4S4	P4S3	P4S2	P4S1	P4S0
P5SS	BEH	P5 mode Select	----00--	-	-	-	-	P5S3	P5S2	-	-
DISPCLK1	DFH	LCD Pump Clock Control register	------00	-	-	-	-	-	-	LCDPUMP1	LCDPUMP0

Table 6.13 PWM SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
REMCON	D9H	REM Control	------00	-	-	-	-	-	-	REMIF	REMSW
REMNUMH	DAH	REM Envelope Carrier Number High Byte	0-000000	REMHLSIGN	-	REMNUMH.5	REMNUMH.4	REMNUMH.3	REMNUMH.2	REMNUMH.1	REMNUMH.8
REMNUML	DBH	REM Envelope Carrier Number Low Byte	00000000	REMNUML.7	REMNUML.6	REMNUML.5	REMNUML.4	REMNUML.3	REMNUML.2	REMNUML.1	REMNUML.0
PWM1CON	DCH	PWM1 Control	00000000	PWM1EN	PWM1S	PWM1CK2	PWM1CK1	PWM1CK0	PWM1IE	PWM1IF	PWM1SS
PWM1PL	DDH	12 bit PWM1 Period Control Low Byte	00000000	PWM1PL.7	PWM1PL.6	PWM1PL.5	PWM1PL.4	PWM1PL.3	PWM1PL.2	PWM1PL.1	PWM1PL.0
PWM1PH	DEH	12 bit PWM1 Period Control High Byte	----0000	-	-	-	-	PWM1PH.3	PWM1PH.2	PWM1PH.1	PWM1PH.0
PWM1DL	B6H	PWM1 Duty Control low Byte	00000000	PWM1DL.7	PWM1DL.6	PWM1DL.5	PWM1DL.4	PWM1DL.3	PWM1DL.2	PWM1DL.1	PWM1DL.0
PWM1DH	B7H	PWM1 Duty Control High Byte	----0000	-	-	-	-	PWM1DH.3	PWM1DH.2	PWM1DH.1	PWM1DH.0

Table 6.14 LPD SFRs

Mnem	Add	Name	POR/WDT/LVR /PIN Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LPDCON	B3H	LPD Control	00000000	LPDEN	LPDF	LPDMD	LPDIF	LPDS3	LPDS2	LPDS1	LPDS0

Note: *- :Reserved bit.*

SFR Map

	Bit addressable	Non Bit addressable							
	0/8	*1/9*	*2/A*	*3/B*	*4/C*	*5/D*	*6/E*	*7/F*	
F8H	P5	-	-	IB_OFFSET	IB_DATA	-	-	(Reserved)	FFH
F0H	B	AUXC	IB_CON1	IB_CON2	IB_CON3	IB_CON4	IB_CON5	XPAGE	F7H
E8H	EXF0	P0PCR	P1PCR	P2PCR	P3PCR	P4PCR	P5PCR	-	EFH
E0H	ACC	P0CR	P1CR	P2CR	P3CR	P4CR	P5CR	DISPCLK0	E7H
D8H	EXF1	REMCON	REMNUMH	REMNUML	PWM1CON	PWM1PL	PWM1PH	DISPCLK1	DFH
D0H	PSW	-	-	-	-	-	-	-	D7H
C8H	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2	T3CON	-	CFH
C0H	P4	-	ADCH2	-	TL5	TH5	T5CON	EXCON	C7H
B8H	IPL0	IPL1	IENC	P2SS	P3SS	P4SS	P5SS	P0SS	BFH
B0H	P3	RSTSTAT	CLKCON	LPDCON	IPH0	IPH1	PWM1DL	PWM1DH	B7H
A8H	IEN0	IEN1	LCDCON1	LCDCON	-	P1SS	-	-	AFH
A0H	P2	-	-	-	-	-	-	FLASHCON	A7H
98H	SCON	SBUF	SADDR	SADEN	SBRTH	SBRTL	SFINE	UTOS	9FH
90H	P1	TL3	TH3	ADCON	ADT	ADCH1	ADDL	ADDH	97H
88H	TCON	-	-	-	-	-	SUSLO	ADCON1	8FH
80H	P0	SP	DPL	DPH	DPL1	DPH1	INSCON	PCON	87H
	0/8	*1/9*	*2/A*	*3/B*	*4/C*	*5/D*	*6/E*	7/F	

Note: *The unused addresses of SFR are not available.*

7. Normal Function

7.1 CPU

7.1.1 Feature

- CPU core registers: ACC, B, PSW, SP, DPL, DPH

Accumulator

ACC is the Accumulator register. The Names for accumulator-specific instructions, however, refer to the Accumulator simply as A.

B Register

The B register is used during multiply and divide operations. For other instructions it can be treated as another scratch pad register.

Stack Pointer (SP)

The Stack Pointer Register is 8 bits wide, It is incremented before data is stored during PUSH, CALL executions and it is decremented after data is out of stack during POP, RET, RETI executions. The stack may reside anywhere in on-chip internal RAM (00H-FFH). On reset, the Stack Pointer is initialized to 07H causing the stack to begin at location 08H.

Program Status Word Register (PSW)

The PSW register contains program status information.

Table 7.1 PSW Register

D0H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PSW	CY	AC	F0	RS1	RS0	OV	F1	P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
7	**CY**	**Carry flag bit** 0: no carry or borrow in an arithmetic or logic operation 1: a carry or borrow in an arithmetic or logic operation
6	**AC**	**Auxiliary Carry flag bit** 0: an auxiliary carry or borrow in an arithmetic or logic operation 1: an auxiliary carry or borrow in an arithmetic or logic operation
5	**F0**	**F0 flag bit** Available to the user for general purposes
4-3	**RS[1:0]**	**R0-R7 Register bank select bits** 00: Bank0 (Address to 00H-07H) 01: Bank1 (Address to 08H-0FH) 10: Bank2 (Address to 10H-17H) 11: Bank3 (Address to 18H-1FH)
2	**OV**	**Overflow flag bit** 0: no overflow happen 1: an overflow happen
1	**F1**	**F1 flag bit** Available to the user for general purposes
0	**P**	**Parity flag bit** 0: an even number of “one” bits in the Accumulator 1: an odd number of “one” bits in the Accumulator

Data Pointer Register (DPTR)

DPTR consists of a high byte (DPH) and a low byte (DPL). Its intended function is to hold a 16-bit address, but it may be manipulated as a 16-bit register or as two independent 8-bit registers.

7.1.2 Enhanced CPU core SFRs

- Extended 'MUL' and 'DIV' instructions: 16bit*8bit, 16bit/8bit
- Dual Data Pointer
- Enhanced CPU core registers: AUXC, DPL1, DPH1, INSCON

The SH79F3252 has modified 'MUL' and 'DIV' instructions. These instructions support 16 bit operand. A new register - the register is applied to hold the upper part of the operand/result.

The AUXC register is used during 16 bit operand multiply and divide operations. For other instructions it can be treated as another scratch pad register.

After reset, the CPU is in standard mode, which means that the 'MUL' and 'DIV' instructions are operating like the standard 8051 instructions. To enable the 16 bit mode operation, the corresponding enable bit in the INSCON register must be set.

	Operation		Result		
			A	B	AUXC
MUL	INSCON.2 = 0; 8 bit mode	(A)*(B)	Low Byte	High Byte	---
	INSCON.2 = 1; 16 bit mode	(AUXC A)*(B)	Low Byte	Middle Byte	High Byte
DIV	INSCON.3 = 0; 8 bit mode	(A)/(B)	Quotient Low Byte	Remainder	---
	INSCON.3 = 1; 16 bit mode	(AUXC A)/(B)	Quotient Low Byte	Remainder	Quotient High Byte

Dual Data Pointer

Using two data pointers can accelerate data memory moves. The standard data pointer is called DPTR and the new data pointer is called DPTR1.

DPTR1 is the same with DPTR, which consists of a high byte (DPH1) and a low byte (DPL1). Its intended function is to hold a 16-bit address, but it may be manipulated as a 16-bit register or as two independent 8-bit registers.

The DPS bit in INSTCON register is used to choose the active pointer. The user can switch data pointers by toggling the DPS bit. And all DPTR-related instructions will use the currently selected data pointer.

7.1.3 Registers

Table 7.2 Data Pointer Selection Register

86H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INSCON	-	-	-	-	DIV	MUL	-	DPS
R/W	-	-	-	-	R/W	R/W	-	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	-	0

Bit Number	Bit Name	Description
3	**DIV**	**16 bit/8 bit Divide Selection Bit** 0: 8 bit Divide 1: 16 bit Divide
2	**MUL**	**16 bit/8 bit Multiply Selection Bit** 0: 8 bit Multiply 1: 16 bit Multiply
0	**DPS**	**Data Pointer Selection Bit** 0: Data pointer 1: Data pointer1

Note: *bit6 must be 0.*

7.2 RAM

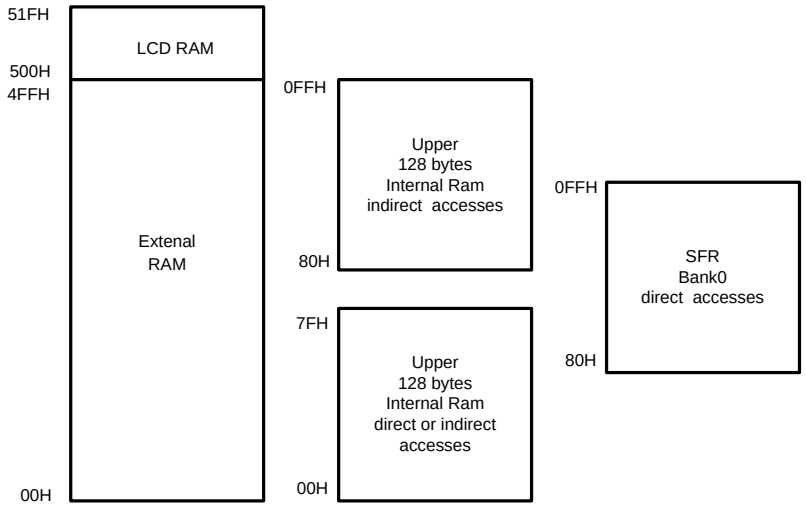
7.2.1 Features

SH79F3252 provides both internal RAM and external RAM for random data storage. The internal data memory is mapped into four separated segments:

- The Lower 128 bytes of RAM (addresses 00H to 7FH) are directly and indirectly addressable.
- The Upper 128 bytes of RAM (addresses 80H to FFH) are indirectly addressable only.
- The Special Function Registers (SFR, addresses 80H to FFH) are directly addressable only.
- The external RAM are indirectly accessed by MOVX instructions.

The Upper 128 bytes occupy the same address space as SFR, but they are physically separate from SFR space. When an instruction accesses an internal location above address 7FH, the CPU can distinguish whether to access the upper 128 bytes data RAM or to access SFR by different addressing mode of the instruction.

SH79F3252 provides an extra 1280 bytes of RAM to support high-level language in external data space. Also, SH79F3252 proviodes 32 bytes LCD RAM(addresses 500H to 51FH).



The SH79F3252 provides traditional method for accessing of external RAM. Use *MOVXA, @Ri* or *MOVX @Ri, A;* to access external low 256 bytes RAM; *MOVX A, @DPTR* or *MOVX @DPTR, A* also to access external 1312 bytes RAM.

In SH79F3252 the user can also use XPAGE register to access external RAM only with *MOVX A, @Ri* or *MOVX @Ri, A* instructions. The user can use XPAGE to represent the high byte address of RAM above 256 Bytes.

In Flash SSP mode, the XPAGE can also be used as sector selector (Refer to SSP Function).

7.2.2 Register

Table 7.3 Data Memory Page Register (XPAGE)

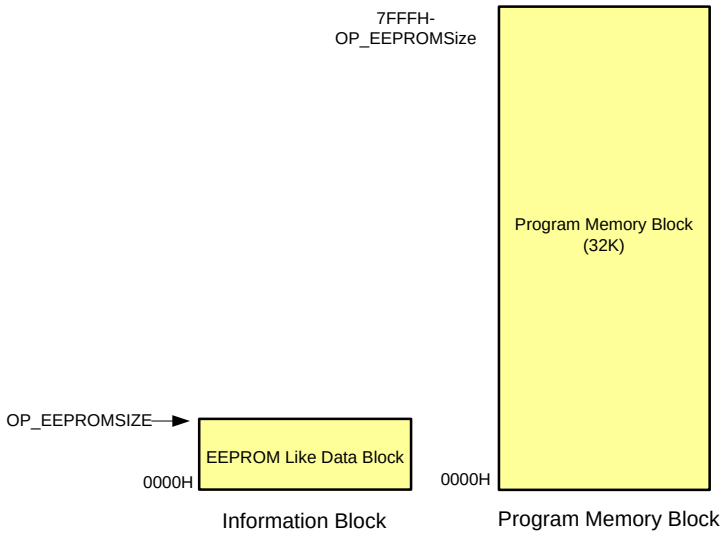
F7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
XPAGE	-	XPAGE.6	XPAGE.5	XPAGE.4	XPAGE.3	XPAGE.2	XPAGE.1	XPAGE.0
R/W	**-**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
Reset Value (POR/WDT/LVR/PIN)	-	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
6-3	**XPAGE[6:3]**	RAM Page Selector no significance
2-0	**XPAGE[2:0]**	RAM page control-bit

7.3 Flash Program Memory

7.3.1 Features

- The program memory consists 64 X 512Byte sectors, total 32KB
- EEPROM like memory 0 ~ 4KB (code option)
- Programming and erasing can be done over the full operation voltage range
- Write, read and erase operation are all supported by In-Circuit Programming (ICP)
- Fast mass/sector erase and programming
- Minimum program/erase cycles:
  Main program memory: 10,000
  EEPROM like memory: 100,000
- Minimum years data retention: 10
- Low power consumption



The SH79F3252 embeds 32K flash program memory for program code. The flash program memory provides electrical erasure and programming and supports In-Circuit Programming (ICP) mode and Self-Sector Programming (SSP) mode.Every sector is 512 bytes.

The SH79F3252 also embeds 4096 bytes EEPROM-like for program data with 512bytes per sector.and maximum support 8 sectors. EEPROM Data block is located in Flash memory and sharing the space with program memory block. For example, when OP_EEPROMSIZE = 0000, selected 4KB EEPROM, the program memory size is 32KB-4KB = 28KB, when OP_EEPROMSIZE = 0100, selected 2KB EEPROM, the program memory size is 32KB-2KB = 30KB. The specific content of selecting EEPROM size refers to code option chapter.

Flash operation definition:

In-Circuit Programming (ICP) mode: Erase, read and write to flash memory by the Flash Programmer

Self-Sector Programming (SSP) mode: Erase, read and write to flash memory by the user code in program memory.

Flash memory supports the following operations:

(1) Code-Protect Control mode Programming

SH79F3252 implements code-protect function to offer high safeguard for customer code. Four modes are available for each sector.

Code-protect control mode 0: Used to enable/disable the write/read operation (except mass erase) from any programmer.
Code-protect control mode 1: Used to enable/disable the read operation through MOVC instruction from other sectors.
Code-protect control mode 2: Used to enable/disable SSP Function,once enable, the sector erase/write operation through SSP is forbiden.But it will not forbid the operation on EEPROM-like block.
Code-protect control mode 3: Customer password, write by customer, consists of 6 bytes. To enable the wanted protect mode, the user must use the Flash Programmer to set the corresponding protect bit.
The user must use the following two ways to complete code protection control mode Settings:
1. Flash programmer in ICP mode is set to corresponding protection bit to enter the protected mode.
2. The SSP mode does not support code protection control mode programming.

(2) Mass Erase

Regardless of the state of the code protection control mode, the overall erasure operation will erase all programs, code options, the code protection bit, but they will not erase EEPROM-like memory block.

The user must use the following way to complete the overall erasure:

Flash programmer in ICP mode send overall erasure instruction to run overall erasure.

The SSP mode does not support overall erasure mode.

(3) Sector Erase

Sector erasure operations will erase the content of selected sector. The user program (SSP) and Flash programmer can perform this operation.

For user programs to perform the operation, code protection mode 1 in the selected sector must be forbidden.

For Flash programmer to perform the operation,code protection mode 0 in the selected sector must be forbidden.

The user must use one of the following two ways to complete sector erasure:

1. Flash programmer in ICP mode send sector erasure instruction to run sector erasure.
2. Through the SSP function send sector erasure instruction to run sector erasure (see chapter SSP).

(4) EEPROM-Like Erase

EEPROM-like memory block erasure operations will erase the content in EEPROM-like memory block.The user program (SSP) and Flash programmer can perform this operation.

The user must use one of the following two ways to complete EEPROM-like memory block erasure:

1. Flash programmer in ICP mode send EEPROM-like memory block erasure instruction to run EEPROM-like memory block erasure.
2. Through the SSP function send EEPROM-like memory block erasure instruction to run EEPROM-like memory block erasure (see chapter SSP).

(5) Write/Read Code

Write/read code operation can read or write code from flash memory block. The user program (SSP) and Flash programmer can perform this operation.

For user programs to perform the operation, code protection mode 1 and mode 2 in the selected sector must be forbidden. Regardless of the security bit Settings or not, the user program can read/write the sector which contains program itself.

For Flash programmer to perform the operation, code protection mode 0 in the selected sector must be forbidden. If the code protection mode 3 enabled, it need to enter the correct customer password.

The user must use one of the following two ways to complete write/read code:

1. Flash programmer in ICP mode send write/read code instruction to run write/read code.
2. Through the SSP function send write/read code instruction to run write/read code.

(6) Write/Read EEPROM-Like

EEPROM-like memory block operation can read or write data from EEPROM-like memory block. The user program (SSP) and Flash programmer can perform this operation.

The user must use one of the following two ways to complete write/read EEPROM-like memory block:

1. Flash programmer in ICP mode send write/read EEPROM-like memory block instruction to run write/read EEPROM-like memory block.
2. Through the SSP function send write/read EEPROM-like memory block instruction to run write/read EEPROM-like memory block.

Flash Memory Operation

Operation	ICP	SSP
Code Protection	Yes	No
Sector Erase	Yes (without security bit)	Yes (without security bit)
Mass Erase	Yes	No
EEPROM-like Erase	Yes	Yes
Write/Read	Yes (without security bit)	Yes (without security bit)
EEPROM-like Write/Read	Yes	Yes

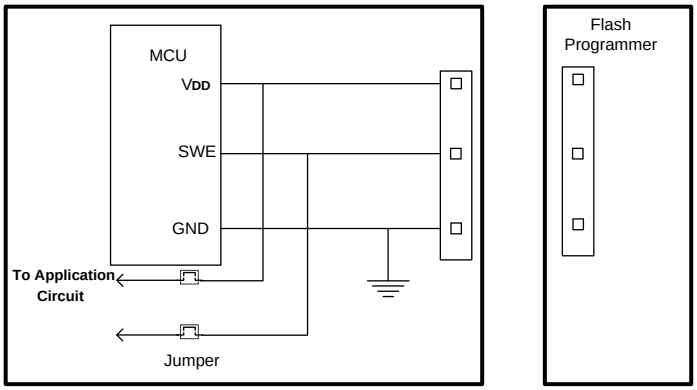
7.3.2 Flash Operation in ICP Mode

Single Line Simulation model

ICP mode is performed without removing the micro-controller from the system. In ICP mode, the user system must be power-off, and the programmer can refresh the program memory through ICP programming interface. The ICP programming interface consists of 3 pins (V_{DD}, GND, SWE).

At first the one JTAG pin (SWE) is used to enter the programming mode. Only after the one pin is inputted the specified waveform, the CPU will enter the programming mode. For more detail description please refers to the **FLASH Programmer's user guide**.

In ICP mode,all the flash operations are completed by the programmer through 3-wire interface. Since the program signal is very sensitive, three jumpers are needed (VDD, GND, SWE) to separate the program pins from the application circuit as the following diagram.



The recommended steps are as following:

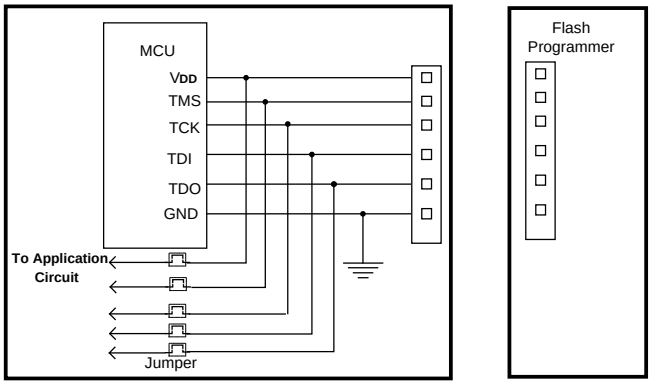
(1) The jumpers must be open to separate the programming pins from the application circuit before programming.
(2) Connect the programming interface with programmer and begin programming.
(3) Disconnect programmer and short these jumpers after programming is complete

Four Line Smiulation model

ICP mode is performed without removing the micro-controller from the system. In ICP mode, the user system must be power-off, and the programmer can refresh the program memory through ICP programming interface. The ICP programming interface consists of 6 wires (V_{DD}, GND, TCK, TDI, TMS, TDO).

At first the four JTAG pins (TDO, TDI, TCK, TMS) are used to enter the programming mode. Only after the three pins are inputted the specified waveform, the CPU will enter the programming mode. For more detail description please refers to the FLASH Programmer's user guide.

In ICP mode,all the flash operations are completed by the programmer through 6-wire interface. Since the program timing is very sensitive, five jumpers are needed (V_{DD}, TDO, TDI, TCK, TMS) to separate the program pins from the application circuit as the following diagram.



The recommended steps are as following:

(1) The jumpers must be open to separate the programming pins from the application circuit before programming.
(2) Connect the programming interface with programmer and begin programming.
(3) Disconnect programmer and short these jumpers after programming is complete

7.4 SSP Function

The SH79F3252 provides SSP (Self Sector Programming) function, each sector can be sector erased or programmed by the user's code if the selected sector is not be protected. But once sector has been programmed, it cannot be reprogrammed before sector erase.

The SH79F3252 builds in a complex control flow to prevent the code from carelessly modification. If the dedicated conditions are not met (IB_CON1-5), the SSP will be terminated.

7.4.1 Registers

Table 7.4 Offset Register for Programming

Flash memory, one sector is 512bytes:

F7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
XPAGE	-	XPAGE.6	XPAGE.5	XPAGE.4	XPAGE.3	XPAGE.2	XPAGE.1	XPAGE.0
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
6-1	**XPAGE[6:1]**	Sector of the flash memory to be programmed, 000000---means sector 0, and so on
0	**XPAGE[0]**	High Address of Offset of the flash memory sector to be programmed

Table 7.5 Memory Page Register for Programming/Erase

EEPROM-like memory, one sector is 512 bytes, total 8 sectors, register defined as below:

F7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
XPAGE	-	XPAGE.6	XPAGE.5	XPAGE.4	XPAGE.3	XPAGE.2	XPAGE.1	XPAGE.0
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
6-4	**XPAGE[6:4]**	Meaningless in erase/program sector
3-1	**XPAGE[3:1]**	Erased/programmed sector number of EEPROM-like
0	**XPAGE[0]**	High address bit of Erased/programmed storage location

Through "MOVC A, @A+DPTR" or "MOVC A, @A+PC" can access EEPROM-like memory block.

Note: *The FAC bit in FLASHCON need to be set 1.*

Table 7.6 Offset of Flash Memory for Programming

FBH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_OFFSET	IB_OFF SET.7	IB_OFF SET.6	IB_OFF SET.5	IB_OFF SET.4	IB_OFF SET.3	IB_OFF SET.2	IB_OFF SET.1	IB_OFF SET.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**IB_OFFSET[7:0]**	Low Address of Offset of the flash memory sector to be programmed

Table 7.7 Data Register for Programming

FCH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_DATA	IB_DATA.7	IB_DATA.6	IB_DATA.5	IB_DATA.4	IB_DATA.3	IB_DATA.2	IB_DATA.1	IB_DATA.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**IB_DATA[7:0]**	Data to be programmed

Table 7.8 SSP Type select Register

F2H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_CON1	IB_CON1.7	IB_CON1.6	IB_CON1.5	IB_CON1.4	IB_CON1.3	IB_CON1.2	IB_CON1.1	IB_CON1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**IB_CON1[7:0]**	**SSP Type select** 0xE6:Sector Erase 0x6E:Sector Programming

Table 7.9 SSP Flow Control Register1

F3H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_CON2	-	-	-	-	IB_CON2.3	IB_CON2.2	IB_CON2.1	IB_CON2.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
3-0	**IB_CON2[3:0]**	Must be 05H, else Flash Programming will terminate

Table 7.10 SSP Flow Control Register2

F4H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_CON3	-	-	-	-	IB_CON3.3	IB_CON3.2	IB_CON3.1	IB_CON3.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
3-0	**IB_CON3[3:0]**	Must be 0AH else Flash Programming will terminate

Table 7.11 SSP Flow Control Register3

F5H, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_CON4	-	-	-	-	IB_CON4.3	IB_CON4.2	IB_CON4.1	IB_CON4.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

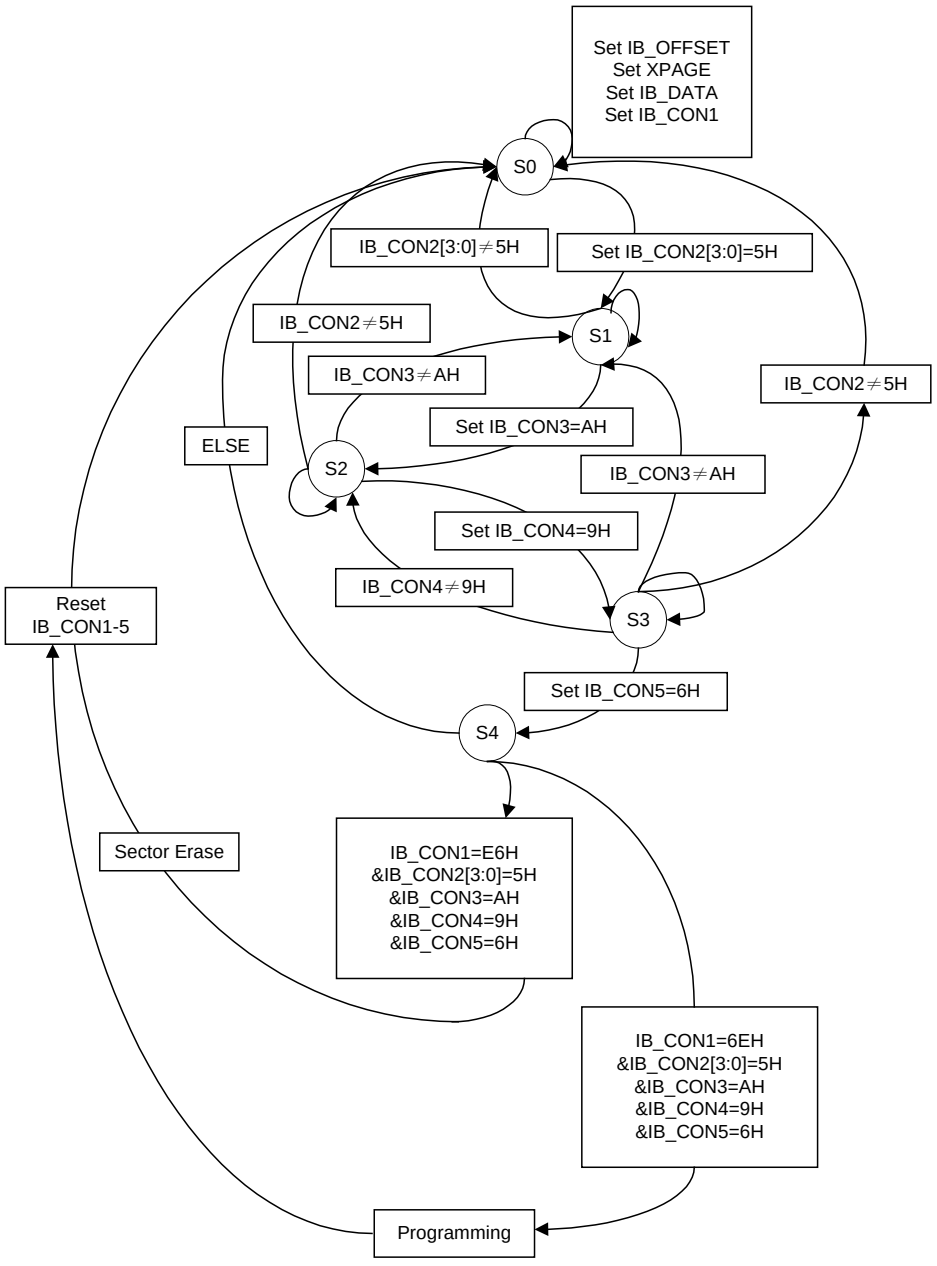
Bit Number	Bit Mnemonic	Description
3-0	**IB_CON4[3:0]**	Must be 09H, else Flash Programming will terminate

Table 7.12 SSP Flow Control Register4

F6H, Bank0	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IB_CON5	-	-	-	-	IB_CON5.3	IB_CON5.2	IB_CON5.1	IB_CON5.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
3-0	**IB_CON5[3:0]**	Must be 06H, else Flash Programming will terminate

7.4.2 Flash Control Flow



7.4.3 SSP Programming Note

To successfully complete SSP programming, the user's software must following the steps below:

(1) For Code/Data Programming

1. Disable interrupt;
2. Fill in the XPAGE, IB_OFFSET for the corresponding address;
3. Fill in IB_DATA if programming is wanted;
4. Fill in IB_CON1-5 sequentially;
5. Add 4 nops for more stable operation;
6. Code/Data programming, CPU will be in IDLE mode;
7. Go to Step 3 if more data are to be programmed;
8. Clear XPAGE; enable interrupt if necessary.

(2) For Sector Erase

1. Disable interrupt;
2. Fill in the XPAGE for the corresponding sector;
3. Fill in IB_CON1-5 sequentially;
4. Add 4 NOPs for more stable operation;
5. Sector Erase, CPU will be in IDLE mode;
6. Go to step 2 if more sectors are to be erased;
7. Clear XPAGE; enable interrupt if necessary.

(3) For Code Reading

Just Use "MOVC A, @A+DPTR" or "MOVC A, @A+PC".

(4) For EEPROM-Like

Steps is same as code programming,the diffenrences are:

1. Set FAC bit in FLASHCON register before programming or erase EEPROM-Like.

Note:

1. To ensure normal programming the system clock must above 200KHz.

2. It is needed to clear FAC after reading readable random code, otherwise it will influence on the instructions execution of reading program ROM.

7.4.4 Readable identificantion Code

A 40-Byte readable identificantion code is burned in the chip after produced, Every byte is between 0 and 0xfffffffff. They can not be erased,and can be read by program and program tool.

Reading the identificantion code program:

```
Unsigned char Temp1, Temp2, Temp3, Temp4, Temp5;
FLASHCON = 0x01;
Temp1 = CBYTE[0x127b];
Temp2 = CBYTE[0x127c];
Temp3 = CBYTE[0x127d];
Temp4 = CBYTE[0x127e];
Temp5 = CBYTE[0x127f];
FLASHCON = 0x00;
```

FLASHCON Register is described as follow:

Table 7.13 Flash Access Control Register

A7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
FLASHCON	-	-	-	-	-	-	-	FAC
R/W	-	-	-	-	-	-	-	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	-	-	-	0

Bit Number	Bit Mnemonic	Description
7-1	**-**	**Reserved**
0	**FAC**	**Flash access control** 0: MOVC or SSP access main memory 1: MOVC or SSP access EEPROM-like or information

7.5 System Clock and Oscillator

7.5.1 Features

- 32.768kHz crystal, Built-in 8MHz RC , 128k/32kHz RC and external clock source
- 2 Oscillator pins (XTAL1, XTAL2) are used to connect 32.768kHz crystal or external clock produces a clock
- Built-in 32kHz WDT RC
- Built-in 32.768kHz speed up circuit
- Built-in system clock prescaler

7.5.2 Clock Definition

The SH79F3252 have several internal clocks defined as below:

OSCCLK: The oscillator clock from one of the four oscillator types (32.768kHz crystal oscillator, internal low frequency RC oscillator and internal high frequency RC oscillator). f_{OSC} is defined as the OSCCLK frequency, t_{OSC} is defined as the OSCCLK period.

32KCRYCLK: 32.768kHz crystal from external XTAL input, f_{32KCRY} is defined as the 32KCRYCLK frequency, t_{32KCRY} is defined as the 32KCRYCLK period.

LRCCLK: Internal 128/32kHz oscillator clock. f_{LRC} is defined as the LRCCLK frequency, t_{LRC} is defined as the LRCCLK period.

HRCCLK: Internal 88MHz oscillator clock. f_{HRC} is defined as the HRCCLK frequency, t_{HRC} is defined as the HRCCLK period.

LOSCCLK: LOSCCLK is selected from four oscillator types defined by OP_OSC. f_{LOSC} is defined as the LOSCCLK frequency, t_{LOSC} is defined as the LOSCCLK period.

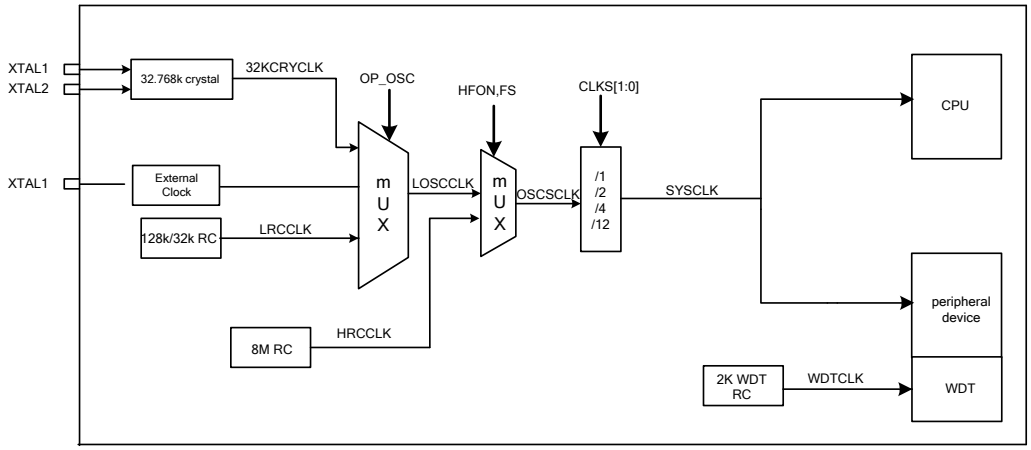
WDTCLK: the internal 2kHz WDT RC clock. f_{WDT} is defined as the WDTCLK frequency. t_{WDT} is defined as the WDTCLK

OSCSCLK: the input of system clock prescaler. It can be LOSCCLK or HRCCLK, is selected by FS. f_{OSCS} is defined as the OSCSCLK frequency, t_{OSCS} is defined as the OSCSCLK period.

SYSCLK: system clock, the output of system clock prescaler. It is the CPU instruction clock. f_{SYS} is defined as the SYSCLK frequency, t_{SYS} is defined as the SYSCLK period.

7.5.3 Description

SH79F3252 has four oscillator types: 32.768kHz crystal oscillator, internal low frequency RC, internal high frequency RC and external clock source, which is selected by code option OP_OSC (Refer to code option section for details).SH79F3252 have 2 Oscillator pins (XTAL1, XTAL2,) and can generates one or two clock sources from four oscillator types. It is selected by code option OP_OSC (Refer to code option section for details). The oscillator generates the basic clock pulse that provides the system clock to supply CPU and on-chip peripherals.



7.5.4 Power Consumption Control

SH79F3252 can select LOSCCLK or HRCCLK as OSCSCLK, No useful clock soure can be shut down after OSCSCLK is selected to reduce power consumption. After the clock source is shut down, if it is turned on again, you must wait for the oscillator warm-up time. It appears slow because of the clock source is not turned off throughout the clock switching process.

7.5.5 Register

Table 7.14 System Clock Control Register

B2H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CLKCON	32k_SPDUP	CLKS1	CLKS0	SCMIF	HFON	FS	AHUM	-
R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	-
Reset Value (POR/WDT/LVR/PIN)	1	1	1	0	0	0	OP_AHRV	-

Bit Number	Bit Name	Description
7	**32k_SPDUP**	**32.768kHz oscillator speed up mode control bit** 0: 32.768kHz oscillator normal mode, cleared by software。 1: 32.768kHz oscillator speed up mode, set by hardware or software. This control bit is set by hardware automatically in all kinds of RESET such as Power on reset, watch dog reset etc. to speed up the 32.768kHz Oscillator oscillating, shorten the 32.768kHz oscillator start-oscillating time. This bit also can be set or cleared by software if necessary. Such as set before entering Power-down mode and cleared when exit Power-down mode. It should be noticed that turning off 32.768kHz oscillator speed up (clear this bit) could reduce the system power consumption.Only when code option OP_OSC is 1010, this bit is valid. (32.768kHz oscillator is selected, Refer to **code option** section for details)
6-5	**CLKS[1:0]**	**SYSCLK Prescaler Register** 00: $f_{SYS} = f_{OSCS}$ 01: $f_{SYS} = f_{OSCS}/2$ 10: $f_{SYS} = f_{OSCS}/4$ 11: $f_{SYS} = f_{OSCS}/12$ If 32.768kHz oscillator or 32KRC is selected as OSCSCLK, these control bits is invalid.
3	**HFON**	**Internal 8MHz RC Switch Control Register** 0: turn off Internal 8MHz RC 1: turn on Internal 8MHz RC Only when code option OP_OSC is 0011 or 1010,this bit is valid. (32.768kHz oscillator or internal low frequency RC is selected, Refer to **code option** section for details)
2	**FS**	**Frequency Select Register** 0: LOSCCLK is selected as OSCSCLK 1: Internal 8Hz RC is selected as OSCSCLK Only when code option OP_OSC is 0011 or 1010,this bit is valid. (32.768kHz oscillator or internal low frequency RC is selected, Refer to **code option** section for details)
1	**AHUM**	**32.768kHz crystal Humidity resistance function control bit** 0:Disable Humidity resistance function 1: Enable Humidity resistance function Note Disable Humidity resistance function (the bit clear), The power consumption of the system can be saved. This control bit is valid only when the code option OP_OSC is 1010 (select the 32.768kHz crystal oscillator, Refer to code option section for details). The reset initial value of this control bit is selected by the code option OP_AHRV (Refer to code option section for details).

Note:

(1) 32kHz or 128kHz which is selected as Internal low frequency clock by code option
(2) If code option OP_OSC is 1010, OSCXCLK is the external 32.768kHz oscillator*.*
(3) If code option OP_OSC is 0011, OSCXCLK is the internal 128K/32KHz oscillator*.*

(4) When OSCSCLK changed from 32.768kHz/ internal 128K /32kHz to 8MHz RC *and HRCCLK is turned off, the steps below must be done in sequence:*

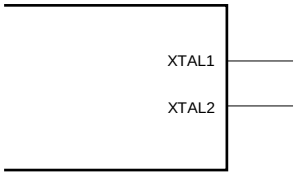
a. Set HFON = 1 to turn on the HRCCLK
b. Wait at least Oscillator Warm-up time (Refer to ***Warm-up Timer*** *section for details)*
c. Set FS = 1 to select 8MHz *as OSCSCLK*

(5) When OSCSCLK changed from 8MHz RC *to 32.768kHz/ internal 128K /32kHz, the steps below must be done in sequence:*

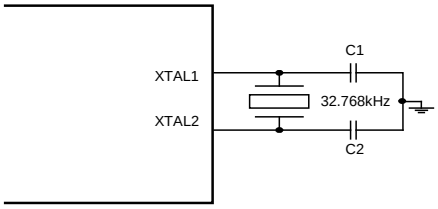
a. Clear FS to select 32.768kHz/ internal 128K /32kHz as OSCSCLK
b. Add one nop
c. Clear HFON
d. Add four nop

7.5.6 Oscillator Type

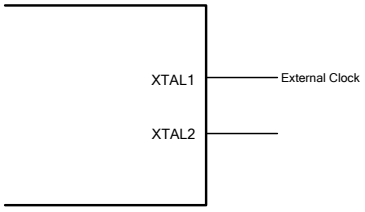
(1) OP_OSC = 0000,0011:internal RC, XTAL1 and XTAL2 are shared with IO



(2) OP_OSC = 1010:32.768kHz Crystal Oscillator from XTAL input, Internal 128K/32K RC is turned off



(3) OP_OSC = 1110:30kHz - 16MHz Crystal/Ceramic Oscillator input from XTAL1,XTAL2 is shared with IO



7.5.7 Capacitor Selection for Oscillato

Crystal Oscillator			remarks
Frequency	**C1**	**C2**	
32.768kHz	15pF	15pF	DT 38 (ϕ 3 X 8) ϕ 3x8 - 32.768kHz

Notes:

(1) ***Capacitor values are used for design guidance only!***

(2) These capacitors were tested with the crystals listed above for basic start-up and operation. They are ***not optimized.***

(3) Be careful for the stray capacitance on PCB board, the user should test the performance of the oscillator over the expected V_{DD} and the temperature range for the application.

Before selecting crystal/ceramic, the user should consult the crystal/ceramic manufacturer for appropriate value of external component to get best performance, visit http://www.sinowealth.comfor more recommended manufactures.

7.6 System Clock Monitor (SCM)

In order to enhance the system reliability, SH79F3252 contains a system clock monitor (SCM) module. If the system clock fails (for example the oscillator stops oscillating), the built-in SCM will switch the OSCCLK to the internal 32k and set system clock monitor bit (SCMIF). And the SCM interrupt will be generated when EA and ESCM is enabled. If the external clock comes back, SCM will switch the OSCCLK to the external oscillator and clears the SCMIF automatically.

If OP_SCMSEL selects SCM clock by code option, *the SCM switches the* OSCSCLK *to the internal SCM clock automatically after the external clock fails and has been detected.*

Notes:

The SCMIF is read only register; it can be clear to 0 or set to 1 by hardware only.
If SCMIF is cleared, the SCM switches the system clock to the state before system clock fail automatically.
If Internal RC is selected as OSCCLK by code option (Refer to ***code option*** *section for detail), the SCM can not work.*

Table 7.15 System Clock Control Register

B2H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CLKCON	-	-	-	SCMIF	-	-	-	-
R/W	-	-	-	R	-	-	-	-
Reset Value (POR/WDT/LVR/PIN)	-	-	-	0	-	-	-	-

Bit Number	Bit Mnemonic	Description
4	**SCMIF**	**System Clock Monitor bit** 0: Clear by hardware to indicate system clock is normal 1: Set by hardware to indicate system clock fails

7.7 I/O Port

7.7.1 Features

- 45 bi-directional I/O ports, all support bit operation
- Share with alternative functions

The SH79F3252 has 45 bi-directional I/O ports. The PORT data is put in Px register. The PORT control register (PxCRy) controls the PORT as input or output. Each I/O port has an internal pull-high resistor, which is controlled by PxPCRy when the PORT is used as input (x = 0-5, y = 0-7). some I/O pins can share with alternative functions. There exists a priority rule in CPU to avoid these functions be conflict when all the functions are enabled. (Refer to Port Share Section for details).

7.7.2 Registers

Table 7.16 Port Control Register

E1H - E6H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0CR (E1H)	P0CR.7	P0CR.6	P0CR.5	P0CR.4	P0CR.3	P0CR.2	P0CR.1	P0CR.0
P1CR (E2H)	P1CR.7	P1CR.6	P1CR.5	P1CR.4	P1CR.3	P1CR.2	P1CR.1	P1CR.0
P2CR (E3H)	P2CR.7	P2CR.6	P2CR.5	P2CR.4	P2CR.3	P2CR.2	P2CR.1	P2CR.0
P3CR (E4H)	P3CR.7	P3CR.6	P3CR.5	P3CR.4	P3CR.3	P3CR.2	P3CR.1	P3CR.0
P4CR (E5H)	P4CR.7	P4CR.6	P4CR.5	P4CR.4	P4CR.3	P4CR.2	P4CR.1	P4CR.0
P5CR (E6H)	-	-	-	P5CR.4	P5CR.3	P5CR.2	P5CR.1	P5CR.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**PxCRy** **x = 0-5, y = 0-7**	**Port input/output direction control Register** 0: input mode 1: output mode

Table 7.17 Port Pull up Resistor Control Register

E9H - EEH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0PCR (E9H)	P0PCR.7	P0PCR.6	P0PCR.5	P0PCR.4	P0PCR.3	P0PCR.2	P0PCR.1	P0PCR.0
P1PCR (EAH)	P1PCR.7	P1PCR.6	P1PCR.5	P1PCR.4	P1PCR.3	P1PCR.2	P1PCR.1	P1PCR.0
P2PCR (EBH)	P2PCR.7	P2PCR.6	P2PCR.5	P2PCR.4	P2PCR.3	P2PCR.2	P2PCR.1	P2PCR.0
P3PCR (ECH)	P3PCR.7	P3PCR.6	P3PCR.5	P3PCR.4	P3PCR.3	P3PCR.2	P3PCR.1	P3PCR.0
P4PCR (EDH)	P4PCR.7	P4PCR.6	P4PCR.5	P4PCR.4	P4PCR.3	P4PCR.2	P4PCR.1	P4PCR.0
P5PCR (EEH)	-	-	-	P5PCR.4	P5PCR.3	P5PCR.2	P5PCR.1	P5PCR.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**PxPCRy** **x = 0-5, y = 0-7**	**Input Port internal pull-high resistor enable/disable control** 0: internal pull-high resistor disabled 1: internal pull-high resistor enabled

Note: *If IO port is output mode, internal pull-high resistor must be disabled.*

Table 7.18 Port Data Register

80H - F8H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0 (80H)	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
P1 (90H)	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
P2 (A0H)	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
P3 (B0H)	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
P4 (C0H)	P4.7	P4.6	P4.5	P4.4	P4.3	P4.2	P4.1	P4.0
P5 (F8H)	-	-	-	P5.4	P5.3	P5.2	P5.1	P5.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**Px.y** **x = 0-5, y = 0-7**	Port Data Register

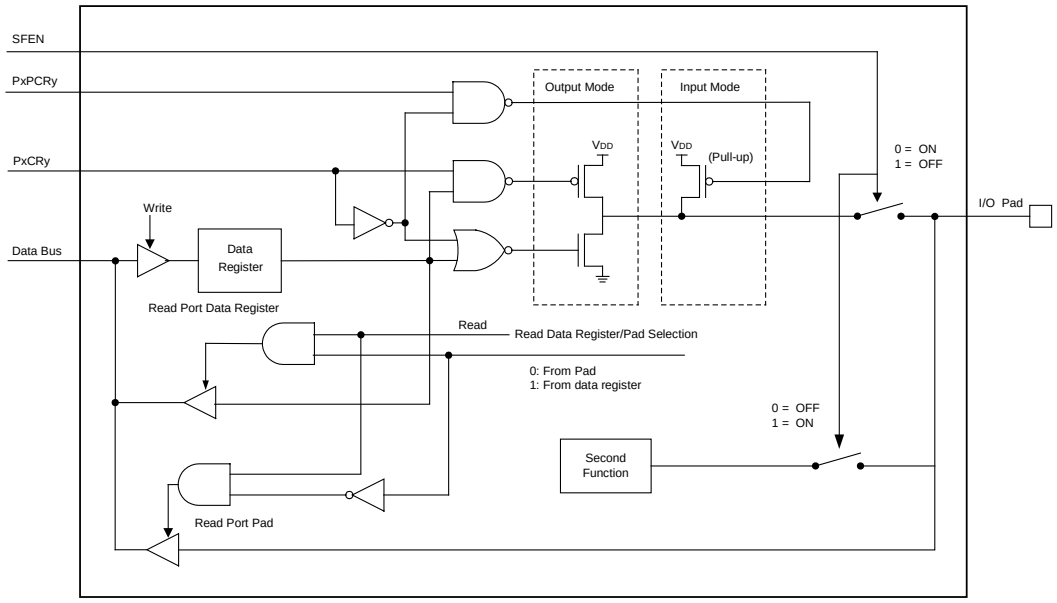
Table 7.19 TTL logic select Register

9FH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UTOS	-	-	-	-	-	-	ES1	ES0
R/W	-	-	-	-	-	-	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	-	-	0	0

Bit Number	Bit Mnemonic	Description
1	**ES1**	**P17 Port input level select** 0: the threshold of input high level is $0.8V_{DD}$, the threshold of input low level is $0.2V_{DD.}$(CMOS logic) 1: the threshold of input high level is $0.25V_{DD}$+0.8, the threshold of input low level is $0.15V_{DD.}$ (V_{DD} = 1.8 - 3.6V) (TTL logic) ***Note:*** *Under the Power-Down mode, TTL logic is invalid*
0	**ES0**	**P40 Port input level select** 0: the threshold of input high level is $0.8V_{DD}$, the threshold of input low level is $0.2V_{DD.}$(CMOS logic) 1: the threshold of input high level is $0.25V_{DD}$+0.8, the threshold of input low level is $0.15V_{DD.}$ (V_{DD} = 1.8 - 3.6V) (TTL logic) ***Note:*** *Under the Power-Down mode, TTL logic is invalid*

Note: *after the TTL function is turned on, all the other second functions (input states) except IO have TTL logic functions. The TTL function is turned on, if the IO port as RXD (INT), RXD (INT) with TTL logic function.*

7.7.3 Port Diagram



Note:

(1) The input source of reading input port operation is from the input pin directly.

(2) The input source of reading output port operation has two paths, one is from the port data Register, and the other is from the output pin directly.

(3) The read Instruction distinguishes which path is selected: The read-modify-write instruction is for the reading of the data register in output mode, and the other instructions are for reading of the output pin directly.

(4) The destination of writing port operation is the data register regardless the port shared as the second function or not.

7.7.4 Port Share

The 45 bi-directional I/O ports can also share second or third special function. But the share priority should obey the **Outer Most Inner Lest** rule:

The out most pin function in **Pin Configuration** has the highest priority, and the inner most pin function has the lowest priority. This means when one pin is occupied by a higher priority function (if enabled), it cannot be used as the lower priority functional pin, even the lower priority function is also enabled. Only until the higher priority function is closed by hardware or software, can the corresponding pin be released for the lower priority function use. Also the function that need pull up resister is also controlled by the same rule.

When port share function is enabled, the user can modify PxCR, PxPCR (x = 0-5), but these operations will have no effect on the port status until the second function was disabled.

When port share function is enabled, any read or write operation to port will only affect the data register while the port pin keeps unchanged until all the share functions are disabled.

PORT0:

- REM/PWM1**/**SEG15:REM signal output pin /PWM1 signal output pin /LCD Segment15 (P0.0)
- SEG14: LCD Segment14 (P0.1)
- CUP1: PUMP circuit external capacitor pin (P0.2)
- CUP2: PUMP circuit external capacitor pin (P0.3)
- VP1: PUMP circuit external capacitor pin (P0.4)
- VP2: PUMP circuit external capacitor pin (P0.5)
- VP3: PUMP circuit external capacitor pin (P0.6)
- SEG13/T2EX: LCD Segment13/Timer2 reload, capture, direction control (P0.7)

Table 7.20 PORT0 Share function Table

Pin No.	Priority	Function	Enable bit
13	1	REM	Set PWM1SS bit and set REMSW
	2	PWM1	Set PWM1SS bit and clear REMSW
	3	SEG15	Set P0S0 bit in P0SS register
	4	P0.0	Above condition is not met
14	1	SEG14	Set P0S1 bit in P0SS register
	2	P0.1	Above condition is not met
15	1	CUP1	**OP_LCDSEL** select capacitor LCD driver in **option code**, at the same time Set Bit6 in LCDCON register or Set Bit5 in ADCON1 register.
	2	P0.2	**OP_LCDSEL** select resistor LCD driver in **option code**; or clear Bit5 in ADCON1 register.
16	1	CUP2	**OP_LCDSEL** select capacitor LCD driver in **option code**, at the same time Set Bit6 in LCDCON register or Set Bit5 in ADCON1 register.
	2	P0.3	**OP_LCDSEL** select resistor LCD driver in **option code**;or clear Bit5 in ADCON1 register.
17	1	VP1	**OP_LCDSEL** select capacitor LCD driver in **option code**, at the same time Set Bit6 in LCDCON register or Set Bit5 in ADCON1 register.
	2	P0.4	**OP_LCDSEL** select resistor LCD driver in **option code**;or clear Bit5 in ADCON1 register.
18	1	VP2	**OP_LCDSEL** select capacitor LCD driver in **option code**, at the same time Set Bit6 in LCDCON register or Set Bit5 in ADCON1 register.
	2	P0.5	**OP_LCDSEL** select resistor LCD driver in **option code**;or clear Bit5 in ADCON1 register.
19	1	VP3	**OP_LCDSEL** select capacitor LCD driver in **option code**, at the same time Set Bit6 in LCDCON register or Set Bit5 in ADCON1 register.
	2	P0.6	**OP_LCDSEL** select resistor LCD driver in **option code**;or clear Bit5 in ADCON1 register.
20	1	SEG13	Set P0S7 bit in P0SS register
	2	T2EX	In mode 0 or 2, set **EXEN2 bit in T2CON** register, or in mode 1, set **DCEN bit in T2CON** register or in mode1, clear **DCEN** bit and set **EXEN2** bit (Auto Pull up)
	3	P0.7	Above condition is not met

PORT1:

- SEG12/T2/INT41: LCD Segment12/timer2 external input/external interrupt 41 (P10)
- SEG11/INT42: LCD Segment11/external interrupt 42 (P1.1)
- SEG10/INT43: LCD Segment10/external interrupt 43 (P1.2)
- SEG9/INT44: LCD Segment9/external interrupt 44 (P1.3)
- SEG8/INT45: LCD Segment8/external interrupt 45 (P1.4)
- SEG7/INT46: LCD Segment7/external interrupt 46 (P1.5)
- SEG6/INT47: LCD Segment6/external interrupt 47 (P1.6)
- SEG5/INT3: LCD Segment5/external interrupt 3 (1.7)

Table 7.21 PORT1 share function table

Pin No.	Priority	Function	Enable bit
21	1	SEG12	Set P1S0 bit in P1SS register
	2	T2	Set **TR2** bit and **C/$\overline{T2}$** bit in **T2CON** register (Auto Pull up) or clear **C/$\overline{T2}$** bit and set **T2OE** bit in **T2MOD** register
	3	INT41	Set EX4 bit in IEN1 Register, Set EXS41 bit in IENC Register and Port1.0 work in input mode (pull up by software)
	4	P1.0	Above condition is not met
22	1	SEG11	Set P1S1 bit in P1SS Register
	2	INT42	Set EX4 bit in IEN1 Register, Set EXS42 bit in IENC Register and Port1.1 work in input mode (pull up by software)
	3	P1.1	Above condition is not met
23	1	SEG10	Set P1S2 bit in P1SS Register
	2	INT43	Set EX4 bit in IEN1 Register, Set EXS43 bit in IENC Register and Port1.2 work in input mode (pull up by software)
	3	P1.2	Above condition is not met
24	1	SEG9	Set P1S3 bit in P1SS Register
	2	INT44	Set EX4 bit in IEN1 Register, Set EXS44 bit in IENC Register and Port1.3 work in input mode (pull up by software)
	3	P1.3	Above condition is not met
25	1	SEG8	Set P1S4 bit in P1SS Register
	2	INT45	Set EX4 bit in IEN1 Register, Set EXS45 bit in IENC Register and Port1.4 work in input mode (pull up by software)
	3	P1.4	Above condition is not met
26	1	SEG7	Set P1S5 bit in P1SS Register
	2	INT46	Set EX4 bit in IEN1 Register, Set EXS46 bit in IENC Register and Port1.5 work in input mode (pull up by software)
	3	P1.5	Above condition is not met
27	1	SEG6	Set P1S6 bit in P1SS Register
	2	INT47	Set EX4 bit in IEN1 Register, Set EXS47 bit in IENC Register and Port1.6 work in input mode (pull up by software)
	3	P1.6	Above condition is not met
28	1	SEG5	Set P1S7 bit in P1SS Register
	2	INT3	Set EX3 bit in IEN1 Register, Port1.7 work in input mode (pull up by software)
	3	P1.7	Above condition is not met

PORT2:

- SEG4: LCD Segment4 (P2.0)
- SEG3: LCD Segment2 (P2.1)
- SEG2: LCD Segment1 (P2.2)
- SEG1/COM5: LCD Segment1/LCD COM5 (P2.3)
- COM4: LCD COM4 (P2.4)
- COM3: LCD COM3 (P2.5)
- COM2: LCD COM2 (P2.6)
- COM1: LCD COM1 (P2.7)

Table 7.22 PORT2 share function table

Pin No.	Priority	Function	Enable bit
29	1	SEG4	Set P2S0 bit in P2SS Register
	2	P2.0	Above condition is not met
30	1	SEG3	Set P2S1 bit in P2SS Register
	2	P2.1	Above condition is not met
31	1	SEG2	Set P2S2 bit in P2SS Register
	2	P2.2	Above condition is not met
32	1	SEG1	Set P2S3 bit in P2SS Register
	2	COM5	Set DUTY in LCDCON Register
	3	P2.3	Above condition is not met
33	1	COM4	Set P2S4 bit in P2SS Register
	2	P2.4	Above condition is not met
34	1	COM3	Set P2S5 bit in P2SS Register
	2	P2.5	Above condition is not met
35	1	COM2	Set P2S6 bit in P2SS Register
	2	P2.6	Above condition is not met
36	1	COM1	Set P2S7 bit in P2SS Register
	2	P2.7	Above condition is not met

PORT3:

- SEG32/AN0: LCD Segment32/ADC input channel 0 (P3.0)
- SEG31/Vref/AN1: LCD Segment31/ADC reference voltage/ADC input channel 1 (P3.1)
- SEG30/AN2: LCD Segment30/ADC input channel 2 (P3.1)
- SEG29/AN3: LCD Segment29/ADC input channel 3 (P3.3)
- SEG28/AN4: LCD Segment28/ADC input channel 4 (P3.4)
- SEG27/AN5: LCD Segment27/ADC input channel 5 (P3.5)
- SEG26/AN6: LCD Segment26/ADC input channel 6 (P3.6)
- SEG25/TXD0: LCD Segment25/UART0 transmit (3.7)

Table 7.23 PORT3 share function table

Pin No.	Priority	Function	Enable bit
37	1	SEG32	Set P3S0 bit in P3SS register
	2	AN0	Set CH0 bit in ADCH1 register
	3	P3.0	Above condition is not met
38	1	SEG31	Set P3S3 bit in P3SS register
	2	Vref	Set ADON bit and set REFC bit in ADCON register
	3	AN1	Set CH1 bit in ADCH1 register
	4	P3.1	Above condition is not met
39	1	SEG30	Set P3S2 bit in P3SS register
	2	AN2	Set CH2 bit in ADCH1 register
	3	P3.2	Above condition is not met
40	1	SEG29	Set P3S3 bit in P3SS register
	2	AN3	Set CH3 bit in ADCH1 register
	3	P3.3	Above condition is not met
41	1	SEG28	Set P3S4 bit in P3SS register
	2	AN4	Set CH4 bit in ADCH1 register
	3	P3.4	Above condition is not met
42	1	SEG27	Set P3S5 bit in P3SS register
	2	AN5	Set CH5 bit in ADCH1 register
	3	P3.5	Above condition is not met
43	1	SEG26	Set P3S6 bit in P3SS register
	2	AN6	Set CH6 bit in ADCH1 register
	3	P3.6	Above condition is not met
44	1	SEG25	Set P3S7 bit in P3SS register
	2	TXD0	Write to **SBUF0** Register
	3	P3.7	Above condition is not met

PORT4:

- SEG24/RXD0/INT2: LCD Segment24/EUART0 receive/External interrupt 2 (P4.0)
- SEG23/T3/INT0: LCD Segment23/Timer3 external input/External interrupt 0 (P4.1)
- SEG22/P0CEX0: LCD Segment22/output pin (P4.2)
- TCK/SEG21/P0CEX1: JTAG/LCD Segment21/output pin (P4.3)
- TDI/SEG20/AN7: JTAG mode/LCD Segment20/ADC input channel 7 (P4.4)
- TMS/SEG19/AN8: JTAG mode/LCD Segment19/ADC input channel 8 (P4.5)
- SWE/TDO/SEG18: One line Debug interface/JTAG **mode**/LCD Segment18 (P4.6)
- $\overline{\text{RESET}}$: PIN reset (P4.7)

Table 7.24 PORT4 share function table

Pin No.	Priority	Function	Enable bit
45	1	SEG24	Set P4S0 bit in P4SS register
	2	RXD0	Set REN bit in SCON0 register
	3	INT2	Set EX2 bit in IEN0 Register, Port4.0 work in input mode (pull up by software)
	4	P4.0	Above condition is not met
46	1	SEG23	Set P4S1 bit in P4SS register
	2	T3	Set **TR3** bit in **T3CON** register and **T3CLKS[1:0] = 01**. (auto pull up)
	3	INT0	Set EX0 bit in IEN1 Register, Port4.1 work in input mode (pull up by software)
	4	P4.1	Above condition is not met
47	1	SEG22	Set P4S2 bit in P4SS register
	2	P4.2	Above condition is not met
48	1	TCK	JTAG mode
	2	SEG21	Set P4S3 bit in P4SS register
	3	P4.3	Above condition is not met
1	1	TDI	JTAG mode
	2	SEG20	Set P4S4 bit in P4SS register
	3	AN7	Set CH7 bit in ADCH1 register
	4	P4.4	Above condition is not met
2	1	TMS	JTAG mode
	2	SEG19	Set P4S5 bit in P4SS register
	3	AN8	Set CH0 bit in ADCH2 register
	4	P4.5	Above condition is not met
3	1	SWE	One line Debug interface
	2	TDO	JTAG mode
	3	SEG18	Set P4S6 bit in P4SS register
	4	P4.6	Above condition is not met
4	1	$\overline{\text{RESET}}$	P4.7 is Selected as reset pin in OP_RST register by Code Option
	2	P4.7	Above condition is not met

PORT5:

- XTAL1: External crystal input (P5.0)
- XTAL2: External crystal output (P5.0)
- SEG17INT40: LCD Segment17/External interrupt 40 (P5.2)
- SEG16: LCD Segment16 (P5.3)
- P5.4

Table 7.25 PORT5 share function table

Pin No.	Priority	Function	Enable bit
5	1	XTAL1	Option code select external 32.768kHz crystal as oscillator1
	2	P5.0	Above condition is not met
6	1	XTAL2	Option code select external 32.768kHz crystal as oscillator1
	2	P5.1	Above condition is not met
7	1	SEG17	Set P5S2 bit in P5SS register
	2	INT40	Set EX4 bit in IEN1 Registerand set **EXS40** bit in **IENC** register, Port5.2 work in input mode (pull up by software)
	3	P5.2	Above condition is not met
8	1	SEG16	Set P5S3 bit in P5SS register
	2	P5.3	Above condition is not met
9	1	P5.4	NO

7.8 Timer

7.8.1 Timer2

The Timer 2 is implemented as a 16-bit register accessed as two cascaded data registers: TH2 and TL2. It is controlled by the register T2CON and T2MOD. The Timer2 interrupt can be enabled by setting the ET2 bit in the IEN0 register. (Refer to Interrupt Section for details)

C/$\overline{T2}$ selects system clock (timer operation) or external pin T2 (counter operation) as the timer clock input. Setting TR2 allows Timer 2/Counter 2 Data Register to increment by the selected input.

System clock or system clock devided by 12 can be selected as the clock source of timer2 by setting TCLKP2 bit in T2MOD register.

Timer2 Modes

Timer2 has 3 operating modes: Capture/Reload, Auto-reload mode with up or down counter, Baud Rate Generator and Programmable clock-output.

Timer2 Mode select

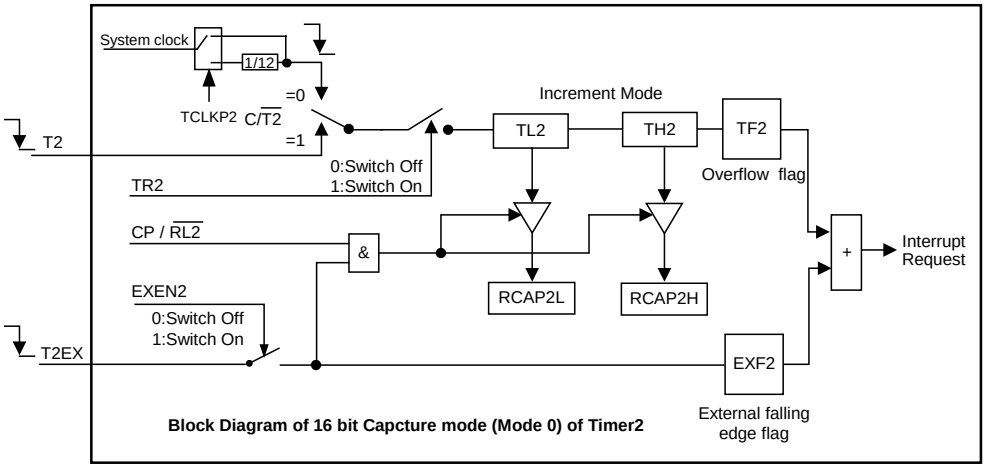
C/$\overline{T2}$	T2OE	DCEN	TR2	CP/RL2	Mode	
X	0	X	1	1	0	16-bit capture
X	0	0	1	0	1	16-bit auto-reload timer
X	0	1	1	0		
0	1	X	1	X	2	Programmable clock
1	1	X	1	X		Not recommed to use
X	X	X	0	X	X	Timer 2 stop to work, still allows the T2EX path way

Mode0: 16-bit Capture

In the capture mode, two options are selected by bit EXEN2 in T2CON.

If EXEN2 = 0, Timer2 is a 16-bit timer or counter which will set TF2 on overflow to generate an interrupt if ET2 is enabled.

If EXEN2 = 1, Timer2 performs the same operation, but a 1-to-0 transition at external input T2EX also causes the current value in TH2 and TL2 to be captured into RCAP2H and RCAP2L respectively, In addition, a 1-to-0 transition at T2EX causes bit EXF2 in T2CON to be set. The EXF2 bit, like TF2, can also generate an interrupt if ET2 is enabled.



Block Diagram of 16 bit Capcture mode (Mode 0) of Timer2

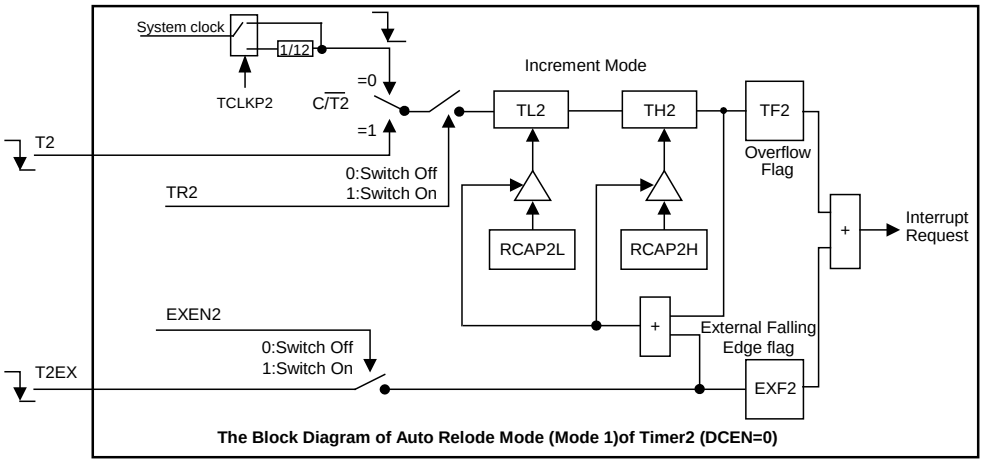
Mode1: 16-bit auto-reload Timer

Timer2 can be programmed to count up or down when configured in its 16-bit auto-reload mode. This feature is invoked by the DCEN (Down Counter Enable) bit in T2MOD. After reset, the DCEN bit is set to 0 so that Timer2 will default to count up. When DCEN is set, Timer2 can count up or down, depending on the value of the T2EX pin.

When DCEN = 0, two options are selected by bit EXEN2 in T2CON.

If EXEN2 = 0, Timer2 counts up to 0FFFFH and then sets the TF2 bit upon overflow. The overflow also causes the timer registers to be reloaded with the 16-bit value in RCAP2H and RCAP2L, which are pressed by software.

If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at external input T2EX. This transition also sets the EXF2 bit. Both the TF2 and EXF2 bits can generate an interrupt if ET2 is enabled.



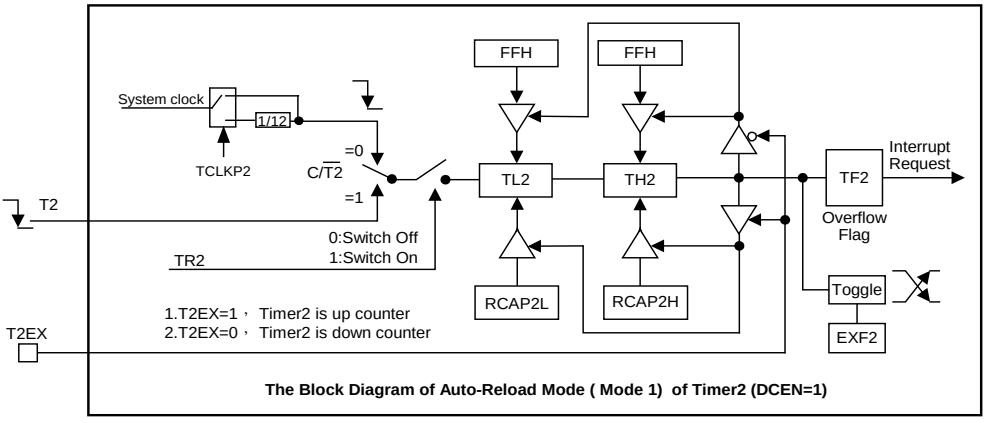
The Block Diagram of Auto Relode Mode (Mode 1)of Timer2 (DCEN=0)

Setting the DCEN bit enables Timer2 to count up or down. When DCEN = 1, the T2EX pin controls the direction of the count, and EXEN2's control is invalid.

A logical "1" at T2EX makes Timer2 count up. The timer will overflow at 0FFFFH and set the TF2 bit. This overflow also causes the 16-bit value in RCAP2H and RCAP2L to be reloaded into the timer registers, TH2 and TL2, respectively.

A logical "0" at T2EX makes Timer2 count down. The timer underflows when TH2 and TL2 equal the values stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and causes 0FFFFH to be reloaded into the timer registers.

The EXF2 bit toggles whenever Timer2 overflows or underflows and can be used as a 17th bit of resolution. In this operating mode, EXF2 does not flag an interrupt.



The Block Diagram of Auto-Reload Mode (Mode 1) of Timer2 (DCEN=1)

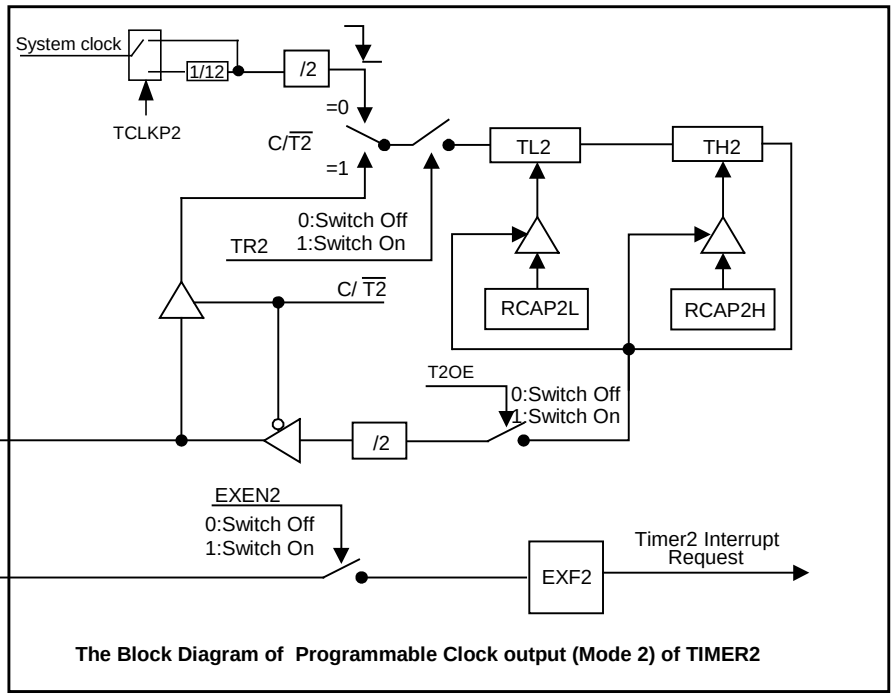
Mode2: Programmable Clock Output

To configure the Timer2 as a clock generator, bit C/$\overline{T2}$ must be cleared and bit T2OE must be set. Bit TR2 starts and stops the timer.

In this mode T2 will output a 50% duty period clock:

$$\text{Clock Out Frequency} = \frac{1}{2 \times 2} \times \frac{f_{SYS}}{65536 - [\text{RCAP2H,RCAP2L}]}$$

Timer2 overflow will not generate an interrupt, so it is possible to use Timer2 as a baud-rate generator and a clock output simultaneously with the same frequency.



The Block Diagram of Programmable Clock output (Mode 2) of TIMER2

Note:

(1) Both TF2 and EXF2 can cause timer2 interrupt request, and they have the same vector address.

(2) TF2 and EXF2 are set as 1 by hardware while event occurs. But they can also be set by software at any time. Only the software and the hardware reset will be able to clear TF2 & EXF2 to 0.

(3) When EA = 1 & ET2 = 1, setting TF2 or EXF2 as 1 will cause a timer2 interrupt.

Registers

Table 7.26 Timer2 Control Register

C8H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T2CON	TF2	EXF2	-	-	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
R/W	R/W	R/W	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**TF2**	**Timer2 overflow flag bit** 0: No overflow (Must be cleared by software) 1: Overflow (Set by hardware)
6	**EXF2**	**External event input (falling edge) from T2EX pin detected flag bit** 0: No external event input (Must be cleared by software) 1: Detected external event input (Set by hardware if EXEN2 = 1)
3	**EXEN2**	**External event input (falling edge) from T2EX pin used as Reload/Capture trigger enable/disable control bit** 0: Ignore events on T2EX pin 1: Cause a capture or reload when a negative edge on T2EX pin is detected
2	**TR2**	**Timer2 start/stop control bit** 0: Stop Timer2 1: Start Timer2
1	**C/$\overline{T2}$**	**Timer2 Timer/Counter mode selected bit** 0: Timer Mode, T2 pin is used as I/O port 1: Counter Mode, the internal pull-up resister is turned on
0	**CP/$\overline{RL2}$**	**Capture/Reload mode selected bit** 0: 16-bits timer/counter with reload function 1: 16-bits timer/counter with capture function

Table 7.27 Timer2 Mode Control Register

C9H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T2MOD	TCLKP2	-	-	-	-	-	T2OE	DCEN
R/W	R/W	-	-	-	-	-	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	-	-	-	-	-	0	0

Bit Number	Bit Mnemonic	Description
7	**TCLKP2**	**Prescale control bit** 0:Timer2 source is 1/12 prescale of system clock 1: Timer2 source is system clock
1	**T2OE**	**Timer2 Output Enable bit** 0: Set P1.0/T2 as clock input or I/O port 1: Set P1.0/T2 as clock output
0	**DCEN**	**Down Counter Enable bit** 0: Disable Timer2 as up/down counter, Timer2 is an up counter 1: Enable Timer2 as up/down counter

Table 7.28 Timer2 Reload/Capture & Data Registers

CAH-CDH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RCAP2L	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0
RCAP2H	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0
TL2	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0
TH2	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**RCAP2L[7:0]**	Timer2 Reload/Capturer Data
	RCAP2H[7:0]	
7-0	**TL2[7:0]**	Timer2 Low & High byte counter
	TH2[7:0]	

7.8.2 Timer3

Timer3 is a 16-bit auto-reload timer. It is implemented as a 16-bit register accessed as two cascaded Data Registers: TH3 and TL3. It is controlled by the T3CON register. The Timer3 interrupt can be enabled by setting ET3 bit in IEN1 register (Refer to Interrupt Section for details).

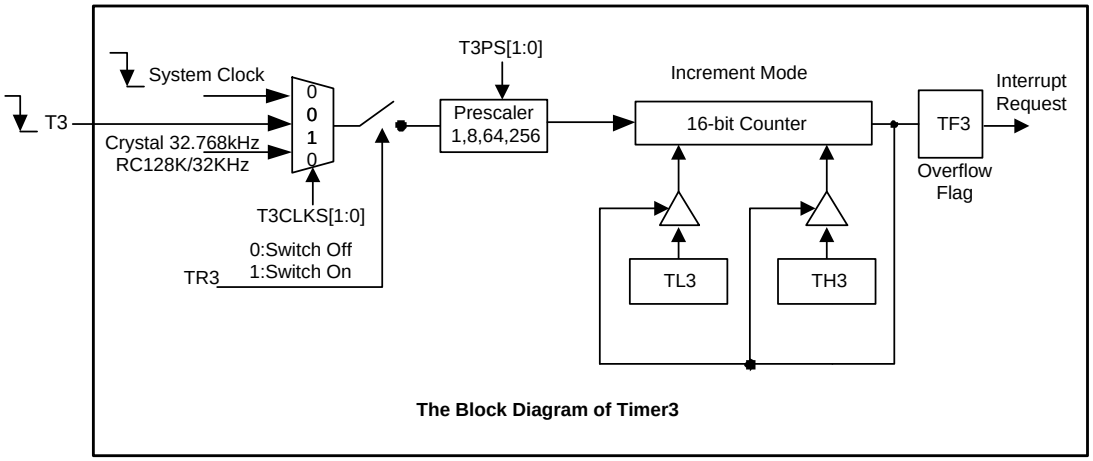
Timer3 has only one operating mode: 16-bit Counter/Timer with auto-reload. Timer3 also supports the following features: selectable pre-scaler setting and Operation during CPU Power-Down mode.

Timer3 consists of a 16-bit counter/reload register (TH3, TL3). When writing to TH3 and TL3, they are used as timer load register. When reading from TH3 and TL3, they are used as timer counter register. Setting the TR3 bit enables Timer 3 to count up. The Timer will overflow from 0xFFFF to 0x0000 and set the TF3 bit. This overflow also causes the 16-bit value written in timer load register to be reloaded into the timer counter register. Writing to TH3 also can cause the 16-bit value written in timer load register to be reloaded into the timer counter register.

Read or write operation to TH3 and TL3 should follow these steps:

Write operation: Low nibble first, High nibble to update the counter.

Read operation: High nibble first, Low nibble followed.



The Block Diagram of Timer3

When T3CLKS [1:0] is 00, Timer3 can't work in Power Down mode.

When T3CLKS [1:0] is 01, Timer3 can work in Power Down mode. Even if all the oscillators are turned off, Timer3 still can count the pulse on T3.

When T3CLKS [1:0] is10, Timer3 can work in Power Down mode. If LOSCCLK are all turned off in Power Down mode, Timer3 can't work.

It can be described in the following table:

T3CLKS[1:0]	Oscillator status	Can work in normal mode	Can work in Power Down mode
00	-	YES	NO
01	-	YES	YES
10	low frequency off in power-down	YES	NO
	low frequency on in power-down	YES	YES

Note:

(1) When TH3 and TL3 read or written, must make sure TR3 = 0.

(2) When T3 is selected as Timer3 clock source and after TR3 is set 0 to 1, T3 falling will be ignored during 1.5 system clock period

Registers

Table 7.29 Timer3 Control Register

CEH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T3CON	TF3	-	T3PS.1	T3PS.0	-	TR3	T3CLKS.1	T3CLKS.0
R/W	R/W	-	R/W	R/W	-	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	-	0	0	-	0	0	0

Bit Number	Bit Mnemonic	Description
7	**TF3**	**Timer3 overflow flag bit** 0: No overflow (cleared by hardware) 1: Overflow (Set by hardware)
5-4	**T3PS[1:0]**	**Timer3 input clock Prescaler Select bits** 00: 1/1 01: 1/8 10: 1/64 11: 1/256
2	**TR3**	**Timer3 start/stop control bit** 0: Stop Timer3 1: Start Timer3
1-0	**T3CLKS[1:0]**	**Timer3 Clock Source select bits** 00: System clock, T3 pin is used as I/O port 01: External clock from pin T3, auto pull-up 10: 32.768kHz from external Crystal or RC 128K/32KHz (Refer to code option section) 11: reserved

Table 7.30 Timer3 Reload/Counter Data Registers

91H-92H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TL3	TL3.7	TL3.6	TL3.5	TL3.4	TL3.3	TL3.2	TL3.1	TL3.0
TH3	TH3.7	TH3.6	TH3.5	TH3.4	TH3.3	TH3.2	TH3.1	TH3.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**TL3.x**	Timer3 Low & High byte counter, x = 0 - 7
	TH3.x	

7.8.3 Timer5

Timer5 is a 16-bit auto-reload timer. It is accessed as two cascaded data registers: TH5 and TL5. It is controlled by the T5CON register. The interrupt can be enabled by setting ET5 bit in IEN0 register (Refer to **interrupt** Section for details).

When writing to TH5 and TL5, they are used as timer load register. When reading from TH5 and TL5, they are used as timer counter register. Setting the TR5 bit enables Timer5 to count up. The timer will overflow from 0xFFFF to 0x0000 and set the TF5 bit. This overflow also causes the 16-bit value written in timer load register to be reloaded into the timer counter register. Writing to TH4 also can cause the 16-bit value written in timer load register to be reloaded into the timer counter register.

Read or write operation to TH5 and TL5 should follow these steps:

Write operation: Low bits first, High bits followed.

Read operation: High bits first, Low bits followed.

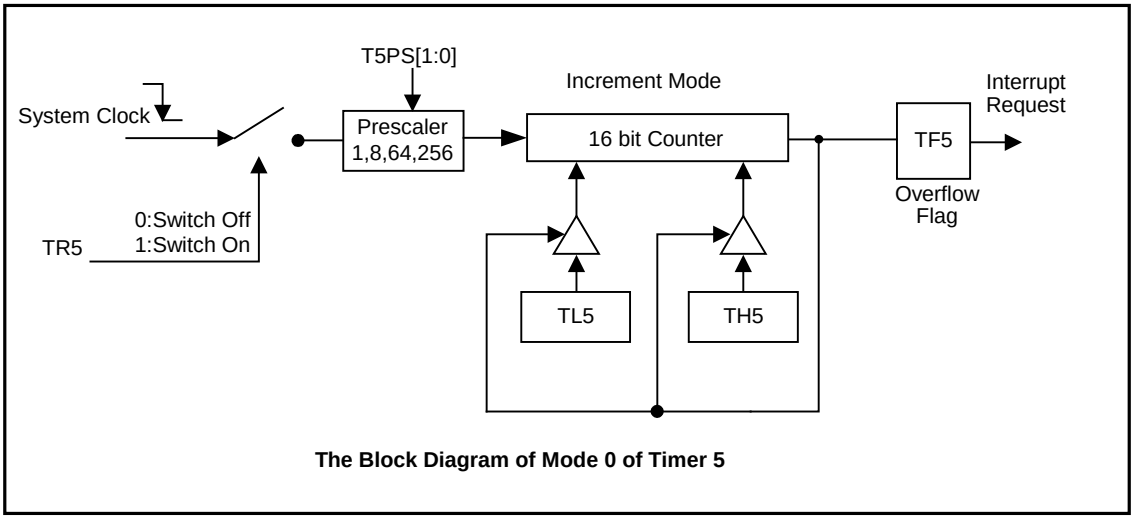
Timer5 Modes

Timer5 has one operating modes: 16-bit auto-reload timer.

16 bit Auto-Reload Counter/Timer

Timer5 operates as 16-bit counter/timer in Mode 0. The TH5 register holds the high eight bits of the 16-bit counter/timer, TL5 holds the low eight bits. As the 16-bit timer register increments and overflows from 0xFFFF to 0x0000, the timer overflow flag TF5 (T5CON.7) is set and the 16-bit value in timer load register are reloaded into timer counter register, and an interrupt will occur if Timer 5 interrupts is enabled.

Setting the TR5 bit (T5CON.1) enables the timer. Setting TR5 does not clear the counter data of Timer4. The timer load register should be loaded with the desired initial value before the timer is enabled.



The Block Diagram of Mode 0 of Timer 5

Registers

Table 7.31 Timer5 Control Register

C6H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
T5CON	TF5	-	T5PS1	T5PS0	-	-	TR5	-
R/W	R/W	-	R/W	R/W	-	-	R/W	-
Reset Value (POR/WDT/LVR/PIN)	0	-	0	0	-	-	0	-

Bit Number	Bit Mnemonic	Description
7	**TF5**	**Timer5 overflow flag bit** 0: No overflow (cleared by hardware) 1: Overflow (Set by hardware)
5-4	**T5PS[1:0]**	**Timer5 input clock Prescaler Select bits** 00: 1/1 01: 1/8 10: 1/64 11: 1/256
1	**TR5**	**Timer5 start/stop control bit** 0: Stop Timer5 1: Start Timer5

Table 7.32 Timer5 Reload/Count Data Register

C4H-C5H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TL5	TL5.7	TL5.6	TL5.5	TL5.4	TL5.3	TL5.2	TL5.1	TL5.0
TH5	TH5.7	TH5.6	TH5.5	TH5.4	TH5.3	TH5.2	TH5.1	TH5.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**TL5.x**	Timer5 Low & High byte counter, x = 0 - 7
	TH5.x	

7.9 Interrupt

7.9.1 Features

- 13 interrupt sources
- 4 interrupt priority levels

The SH79F3252 provides total 13 interrupt sources: 4 External interrupts(External interrupt0/2/3/4, interrupts INT4 including INT40-47),3 timer interrupts (Timer2/3/5), 1 EUART interrupt, 1PWM interrupt, REM interrupt , ADC interrupt, LPD interrupt and SCM interrupt.

7.9.2 Interrupt Enable Control

Each interrupt source can be individually enabled or disabled by setting or clearing the corresponding bit in the interrupt enable registers IEN0 or IEN1. The IEN0 register also contains global interrupt enable bit, EA, which can enable/disable all the interrupts at once. Generally, after reset, all interrupt enable bits are set to 0, which means that all the interrupts are disabled.

Table 7.33 Primary Interrupt Enable Register

A8H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IEN0	EA	EADC	ET2	ES0	ET5	-	EX2	-
R/W	R/W	R/W	R/W	R/W	R/W	-	R/W	-
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	-	0	-

Bit Number	Bit Mnemonic	Description
7	**EA**	**All interrupt enable bit** 0: Disable all interrupt 1: Enable all interrupt
6	**EADC**	**ADC interrupt enable bit** 0: Disable ADC interrupt 1: Enable ADC interrupt
5	**ET2**	**Timer2 overflow interrupt enable bit** 0: Disable Timer2 overflow interrupt 1: Enable Timer2 overflow interrupt
4	**ES0**	**EUART0 interrupt enable bit** 0: Disable EUART0 interrupt 1: Enable EUART0 interrupt
3	**ET5**	**Timer5 overflow interrupt enable bit** 0: Disable Timer5 overflow interrupt 1: Enable Timer5 overflow interrupt
1	**EX2**	**External interrupt2 enable bit** 0: Disable INT2 interrupt 1: Enable INT2 interrupt

Table 7.34 Interrupt Enable Register

A9H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IEN1	ESCM	EPWM1	ELPD	ET3	EX4	EX3	EREM	EX0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**ESCM**	**SCM interrupt enable bit** 0: Disable SCM interrupt 1: Enable SCM interrupt
6	**EPWM1**	**PWM1 interrupt enable bit** 0: Disable PWM1 interrupt 1: Enable PWM1 interrupt
5	**ELPD**	**LPD interrupt enable bit** 0: Disable LPD interrupt 1: Enable LPD interrupt
4	**ET3**	**Timer3 overflow interrupt enable bit** 0: Disable Timer3 overflow interrupt 1: Enable Timer3 overflow interrupt
3	**EX4**	**External interrupt4 enable bit** 0: Disable INT4 interrupt 1: Enable INT4 interrupt
2	**EX3**	**External interrupt3 enable bit** 0: Disable INT3 interrupt 1: Enable INT3 interrupt
1	**EREM**	**REM interrupt enable bit** 0: Disable REM interrupt 1: Enable REM interrupt
0	**EX0**	**External interrupt0 enable bit** 0: Disable INT0interrupt 1: Enable INT0 interrupt

***Note**:*
To enable External interrupt0/2/3/4, the corresponding port must be set to input mode before using it.

Table 7.35 Interrupt4 channel Enable Register

BAH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IENC	EXS47	EXS46	EXS45	EXS44	EXS43	EXS42	EXS41	EXS40
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**EXS4x** **x = 0 - 7**	**External interrupt4 channel select bit (x = 0-7)** 0: Disable External interrupt4x 1: Enable External interrupt4x

7.9.3 Interrupt Flag

Each Interrupt source has its own interrupt flag, when interrupt occurs, corresponding flag will be set by hardware, the interrupt flag bits are listed in Table bellow.

For **external interrupt0**, when an external interrupt0 is generated, if the interrupt was edge trigged, the flag IE0 that generated this interrupt is cleared by hardware when the service routine is vectored. If the interrupt was level trigged, then the requesting external source directly controls the request flag, if it is high level, the flag keep 1, otherwise clear it.

For **external interrupt (INT2/3)**, when an external interrupt2/3 is generated, if the interrupt was edge trigged, the flag(IE2/3)that generated this interrupt is cleared by hardware when the service routine is vectored. If the interrupt was level trigged, then the requesting external source directly controls the request flag, rather than the on-chip hardware.

When an **external interrupt4** is generated, the flag (IF4x (x = 0-7) in EXF1 register) that generated this interrupt should be cleared by user's program because the same vector entrance was used in INT4X. But if INT4 is setup as level trigged, the flag can't be cleared by user's program, it only be controlled by peripheral signal level that connect to INT4X source pin.

Note:all through external interrupt was forbidden, but interrupt flag still be controlled by peripheral signal level that connect to INT source pin, unless the input pin used as the other function.

The **Timer2 interrupt** is generated by the flag TF2 or EXF2 in T2CON register, which is set by hardware, and will be automatically cleared by hardware when the service routine is vectored. In fact, the service routine will normally have to determine whether it was the flag TF2 or the flag EXF2 that generated the interrupt, so the flag must be cleared by software.

The **Timer3 interrupt** is generated when they overflow, the flag TF3 in T3CON register, which is set by hardware, and will be automatically cleared by hardware when the service routine is vectored.

The **Timer5 interrupt** is generated when they overflow, the flag TF5 in T5CON register, which is set by hardware, and will be automatically cleared by hardware when the service routine is vectored.

The **EUART0 interrupt** is generated by flag RI and TI in SCON register, which is set by hardware. Neither of these flags can be cleared by hardware when the service routine is vectored. In fact, the service routine will normally have to determine whether it was the receive interrupt flag or the transmission interrupt flag that generated the interrupt, so the flag must be cleared by software.

The **ADC interrupt** is generated by ADCIF bit in ADCON. If an interrupt is generated, the converted result in ADCDH/ADCDL will be valid. If continuous compare function in ADC module is Enable, ADCIF will not be set at each conversion, but set if converted result is larger than compare value. The flag must be cleared by software.

The **SCM interrupt** is generated by SCMIF bit in SCM register, which is set by hardware.

The **PWM interrupt** is generated by PWM1IF bit in PWMCON register. The flag must be cleared by software.

The **REM interrupt** is generated by REMIF bit in REMCON register. And the flag can only be cleared by hardware.

Table 7.36 External Interrupt Flag Register

88H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TCON	-	-	-	-	-	-	IE0	IT0
R/W	-	-	-	-	-	-	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	-	-	0	0

Bit Number	Bit Mnemonic	Description
1	**IE0**	**INT0 request flag bit** 0: No interrupt pending 1: Interrupt is pending
0	**IT0**	**INT0 trigger mode selection bit** 0: Low Level trigger 1: Trigger on falling edge

Table 7.37 External Interrupt Flag Register

E8H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EXF0	IT4.1	IT4.0	IT3.1	IT3.0	IT2.1	IT2.0	IE3	IE2
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-6	**IT4[1:0]**	**External interrupt4 trigger mode selection bits** 00: Low Level trigger 01: Trigger on falling edge 10: Trigger on rising edge 11: Trigger on both edge IT4 [1:0] is effect on external interrupt 4 at the same mode
5-4	**IT3[1:0]**	**External interrupt3 trigger mode selection bits** 00: Low Level trigger 01: Trigger on falling edge 10: Trigger on rising edge 11: Trigger on both edge
3-2	**IT2[1:0]**	**External interrupt2 trigger mode selection bits** 00: Low Level trigger 01: Trigger on falling edge 10: Trigger on rising edge 11: Trigger on both edge
1	**IE3**	**INT3 request flag bit** 0: No interrupt pending 1: Interrupt is pending
0	**IE2**	**INT2 request flag bit** 0: No interrupt pending 1: Interrupt is pending

Table 7.38 External Interrupt4 Flag Register

D8H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EXF1	IF47	IF46	IF45	IF44	IF43	IF42	IF41	IF40
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**IF4x (x = 0 - 7)**	**INT4 request flag bit** 0: No interrupt pending 1: Interrupt is pending IF4x is cleared by software

7.9.4 Interrupt Vector

When an interrupt occurs, the program counter is pushed onto the stack and the corresponding interrupt vector address is loaded into the program counter. The interrupt vector addresses are listed in Interrupt Summary table.

7.9.5 Interrupt Priority

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing corresponding bits in the interrupt priority control registers IPL0, IPH0, IPL1, and IPH1. But the OVL NMI interrupt has the highest Priority Level (except RESET) of all the interrupt sources, with no IPH/IPL control. The interrupt priority service is described below.

An interrupt service routine in progress can be interrupted by a higher priority interrupt, but can not by another interrupt with the same or lower priority.

The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are received simultaneously, the request of higher priority level is serviced.

If requests of the same priority level are pending at the start of an instruction period, an internal polling sequence determines which request is serviced.

Interrupt Priority		
Priority bits		**Interrupt Lever Priority**
IPHx	IPLx	
0	0	Level 0 (lowest priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest priority)

Table 7.39 Interrupt Priority Control Registers

B8H, B4H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IPL0	-	PADCL	PT2L	PS0L	PT5L	-	PEX2L	-
IPH0	-	PADCH	PT2H	PS0H	PT5H	-	PEX2H	-
R/W	-	R/W	R/W	R/W	R/W	-	R/W	-
Reset Value (POR/WDT/LVR/PIN)	-	0	0	0	0	-	0	-

B9H, B5H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IPL1	PSCML	PPWML	PLPDL	PT3L	PX4L	PX3L	PREML	PX0L
IPH1	PSCMH	PPWMH	PLPDH	PT3H	PX4H	PX3H	PREMH	PX0H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7-0	**PxxxL/H**	Corresponding interrupt source xxx's priority level selection bits

7.9.6 Interrupt Handling

The interrupt flags are sampled and polled at the fetch period of each machine period. All interrupts are sampled at the rising edge of the clock. If one of the flags was set, the CPU will find it and the interrupt system will generate a LCALL to the appropriate service routine, provided this hardware-generated LCALL is not blocked by any of the following conditions:

An interrupt of equal or higher priority is already in progress.

The current period is not in the final period of the instruction in progress. This ensures that the instruction in progress is completed before vectoring to any service routine.

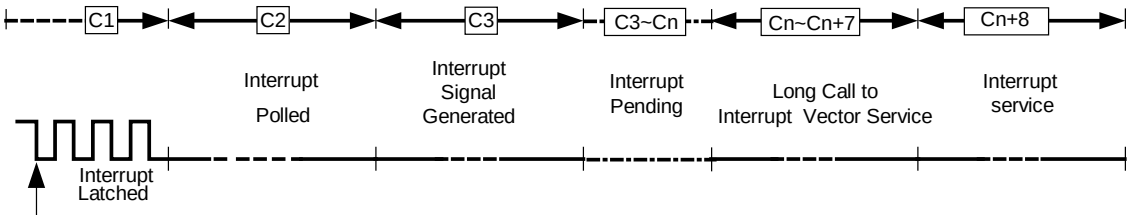
The instruction in progress is RETI. This ensures that if the instruction in progress is RETI then at least one more instruction except RETI will be executed before any interrupt is vectored to; this delay guarantees that the CPU can observe the changes of the interrupt status.

Note:

Since priority change normally needs 2 instructions, it is recommended to disable corresponding Interrupt Enable flag to avoid interrupt between these 2 instructions during the change of priority.

If the flag is no longer active when the blocking condition is removed, the denied interrupt will not be serviced. Every polling period interrogates only the valid interrupt requests.

The polling period/LCALL sequence is illustrated below:



Interrupt Response Timing

The hardware-generated LCALL pushes the contents of the program counter onto the stack (but it does not save the PSW) and reloads the program counter with corresponding address that depends on the source of the interrupt being vectored too, as shown in Interrupt Summary table.

Interrupt service execution proceeds from that location until the RETI instruction is encountered. The RETI instruction informs the processor that the interrupt routine is no longer in progress, and then pops the top two bytes from the stack and reloads the program counter. Execution of the interrupted program continues from the point where it was stopped. Note that the RETI instruction is very important because it informs the processor that the program left the current interrupt service. A simple RET instruction would also have returned execution to the interrupted program, but it would have left the interrupt control system thinking an interrupt with this priority was still in progress. In this case, no interrupt of the same or lower priority level would be acknowledged.

7.9.7 Interrupt Response Timing

If an interrupt is recognized, its request flag is set in every machine period after recognize. The value will be polled by the circuitry until the next machine period; the CPU will generate an interrupt at the third machine period. If the request is active and conditions are right for it to be acknowledged, hardware LCALL to the requested service routine will be the next instruction to be executed. Else the interrupt will pending. The call itself takes 7 machine periods. Thus a minimum of 3+7 complete machine periods will elapse between activation and external interrupt request and the beginning of execution of the first instruction of the service routine.

A longer response time would be obtained if the request was blocked by one of the above three previously listed conditions. If an interrupt of equal or higher priority is already in progress, the additional wait time obviously depends on the nature of the other interrupt's service routine.

If the instruction in progress is not in its final period and the instruction in progress is RETI, the additional wait time is 8 machine periods. For a single interrupt system, if the next instruction is 20 machine periods long (the longest instructions DIV & MUL are 20 machine periods long for 16-bit operation), adding the LCALL instruction 7 machine periods the total response time is 2+8+20+7 machine periods.

Thus interrupt response time is always more than 10 machine periods and less than 37 machine periods.

7.9.8 External Interrupt Input

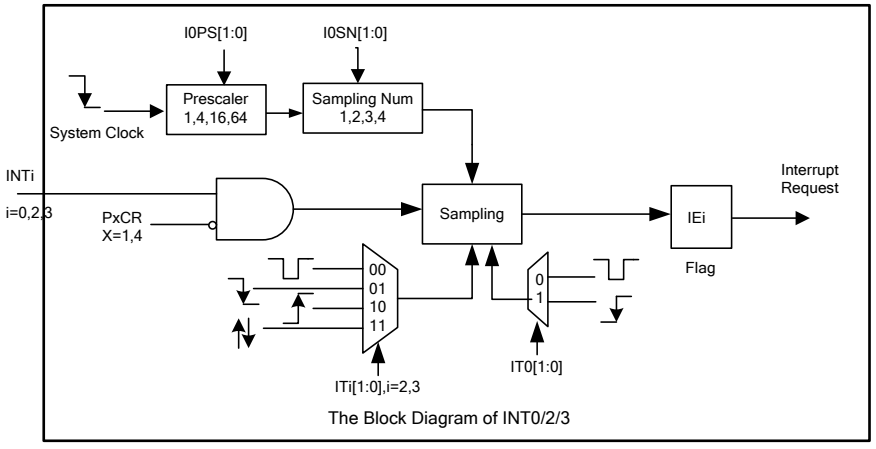
The SH79F3252 has 4 external interrupt inputs. External interrupt0/2/3 every has one vector address. External interrupt 4 has 8 inputs, all of them share one vector address. External interrupt0 can be programmed to be level-triggered or edge-triggered by clearing or setting bit IT0 in register TCON. If IT0 = 0, external interrupt 0 is triggered by a low level detected at the INT0 pin. If IT0 = 1, external interrupt INT0 is edge triggered. In this mode if consecutive samples of the INT0pin show a high level in one period and a low level in the next period, interrupt request flag in register TCON is set, causing an interrupt request. Since the external interrupt pins are sampled once each machine period, an input high or low level should be held for at least one machine period to ensure proper sampling.

External interrupt2/3/4 can be programmed to be level-triggered or edge-triggered or double edge-triggered by clearing or setting bit ITx (x = 2, 3, 4) in register EXF0. If ITx = 00 (x = 2, 3, 4), INTx (x = 2, 3, 4) is triggered by a low level detected. If IT4x (x = 2, 3, 4) = 01 or 10, external interrupt INTx (x = 2, 3, 4) is single edge triggered. In this mode ,if consecutive samples of the INTx (x = 2, 3, 4) pin show a high level in one period and a low level in the next period, interrupt request flag in register EXF0/1 is set, causing an interrupt request. Since the external interrupt pins are sampled once each machine period, an input high or low level should be held for at least one machine period to ensure proper sampling. If ITx (x = 2, 3, 4) = 11, external interrupt INTx (x = 2, 3, 4) is double edge triggered, and any high level of conversion will trigger an interrupt request.

If the external interrupt is a falling edge or the rising edge is triggered, an external interrupt source should be kept at least a 1(INT4)/SN (INT2,3)cycle high (low) level, and then at least a 1 cycle low (high) level. This ensures that the edge can be detected in order to set IEx. After the call interrupt service routine, CPU automatically will clear IEx .

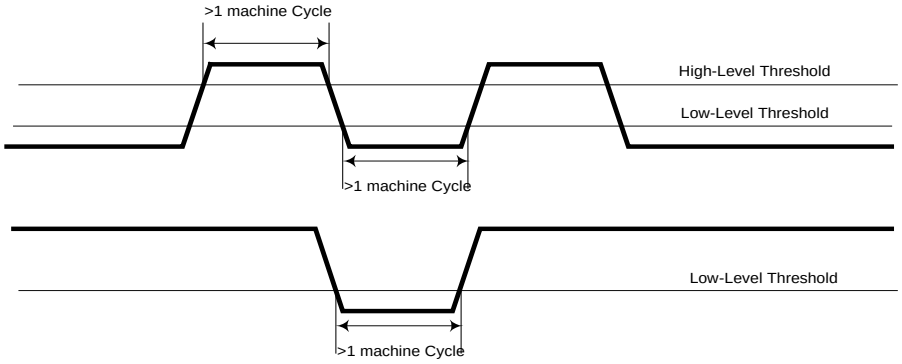
If the external interrupt is level-triggered, the external source must hold the request active until the requested interrupt is generated, which will take 2 machine periods (INT4)and 2 times the SN sampling period(INT2/3). If the external interrupt is still asserted when the interrupt service routine is completed, the next interrupt will be generated.. It is not necessary to clear the interrupt flag IEx (x = 2, 3, 4) when the interrupt is level sensitive, it simply tracks the input pin level.

When SH79F3252 put into IDLE mode or Power-Down mode, the interrupt occurrence will cause the processor to wake up and resume operation. refer to "**Power Management**" chapter for details.



The Block Diagram of INT0/2/3

***Note**: INT0/2/3 is automatically cleared by CPU when the service routine is called while IF40-47 should be cleared by software.*



External Interrupt Detecting

Table 7.40 External interrupt sample times control registrer

C7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EXCON	-	-	-	-	I0PS1	I0PS0	I0SN1	I0SN0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

Bit Number	Bit Mnemonic	Description
3-2	**I0PS[1:0]**	**INT0/2/3 sample clock Prescaler Select bits** 00: 1/1 01: 1/4 10: 1/16 11: 1/64
1-0	**I0SN[1:0]**	**INT0/2/3 sample times Select bits** 00: 1 01: 2 10: 3 11: 4

Note: *If I0SN[1:0] = 11, the INT0, 2, 3 (falling edge tiggle) need sample 4 times tah can be set the interrupt flag.*

7.9.9 Interrupt Summary

Source	Vector Address	Enable bits	Flag bits	Polling Priority	Interrupt No. (C51)
$\overline{\text{RESET}}$	0000H	-	-	0 (higest)	-
INT2	000BH	EX2	IE2	2	1
Timer5	001BH	ET5	TF5	4	3
EUART0	0023H	ES0	RI+TI	5	4
Timer2	002BH	ET2	TF2+EXF2	6	5
ADC	0033H	EADC	ADCIF	7	6
INT0	003BH	EX0	IE0	8	7
REM	0043H	EREM	REMIF	9	8
INT3	004BH	EX3	IE3	10	9
INT4	0053H	EX4+IENC	IF47-40	11	10
Timer3	005BH	ET3	TF3	12	11
LPD	0063H	ELPD	LPDIF	13	12
PWM1	006BH	EPWM1	PWM1IF	14	13
SCM	0073H	ESCM	SCMIF	15	14

8. Enhanced Function

8.1 LCD driver

8.1.1 Feature

- LCD driver support: 4 X 32 dots or 5 X 31 dots
- Support resistor and capacitor bias voltage generating circuit
- Resistor LCD driver support software contrast adjustment and fast charge mode to reduce power consumption
- Capacitor LCD driver contain capacitor bias voltage and buit-in voltage regulator

SH79F3252 provides two different ways of LCD driver: resistor LCD driver and capacitor LCD driver, which is selected by OP_LCDSEL (Refer to **code option** section for details). The capacitor LCD driver also contain capacitor bias voltage and built-in voltage regulator, which is selected thr ough TYPESEL bit in LCDCON register, in addition, only when the LCDON bit is set, the LCD function will be effective.

The LCD driver has two driving modes: 1/4duty - 1/3 bias or 1/5 duty - 1/3 bias, Driving mode is selected by DUTY bit in LCDCON register

When MCU enter idle or Power-Down mode in HRCCLK, LCD still work, RAM still hold data, otherwise, LCD dirve will be turned off.

LCD dirver will be turned off in POR/PIN/LVR/WDT.

When LCD turn to close (OFF), Common and segment output low level.

128K/32kHz RC or 32.768kHz is as the LCD clock source:

(1) If 32.768K crystal is selected by code option, LCD clock source is external 32.768K crystal oscillator, LCD frame is fixed to 64Hz.

(2) if code option selected internal RC of low frequency:

a. if the internal low frequency RC is 32K, the clock source of LCD is 32K RC, the fixed frame frequency is 64Hz, DISPCLK0 register invalid;

b. if the internal low frequency RC is 128K, t the clock source of LCD is 128K RC, set DCK[1:0] selects 1/4, 1/3, 1/2, 1/1 fraction frequency by DISPCLK0 register, and the corresponding LCD frame frequency is 256/4Hz, 56/3Hz, 256/2Hz, 256/1Hz.

(3) if the code option selects the high frequency single clock, the clock source of LCD is 128K RC.

The code selects high-frequency single clock (OP_OSC = 0000 or 1111), the STOP mode, the LCD clock off; code option selects double clock (OP_OSC is 0011, 1010), and work in the high frequency clock, in he STOP mode, the LCD clock to work; code option selects double clock (OP_OSC is 0011, 0110, 1010), and it working in low frequency, in the STOP mode, the LCD clock off; in the IDLE mode, the LCD clock keep working.

8.1.2 Resistor LCD Driver Mode

The resistor LCD driver contains a controller, a duty cycle generator, 4/5 Common signal pins and 32/31 Segment driver pins. Segment 1-32 and COM1-COM5 can also be used as I/O port, which is controlled by the P0SS, P1SS, P2SS, P3SS, P4SS and P5SS register. The 32 bytes display data RAM is addressed to 500H-51FH, which can be used as data memory if needed.

LCD bias resistor (R_{LCD}) can be configured to 60K, 900k or 1.5M by MOD[1:0] bits in the LCDCON register. 60K bias resistor can get better effect, but the current will be relatively large, not suitable for low power consumption application. when the MOD[1:0] bits in LCDON register is set to 1.5M bias resistor, the LCD display will become worse, although it can achieve lower power consumption.

Therefore, SH79F3252 provides both the low power consumption and display effect of the display mode: fast charge mode.

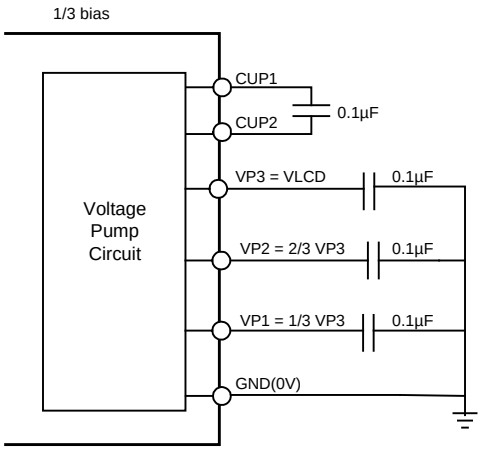
Set MOD[1:0] = 00-1x to select this mode. When refresh the display data 60k bias resistors are selected to provide larger current. When keep the display data 900K/1.5M bias resistors are selected to save drive current.

Charging time is selected as 1/8,1/16, 1/32 or 1/64 of LCD com period by FCCTL[1:0] in LCDCON1 register.

8.1.3 Capacitor LCD Driver Mode

Capacitor bias voltage LCD Driver

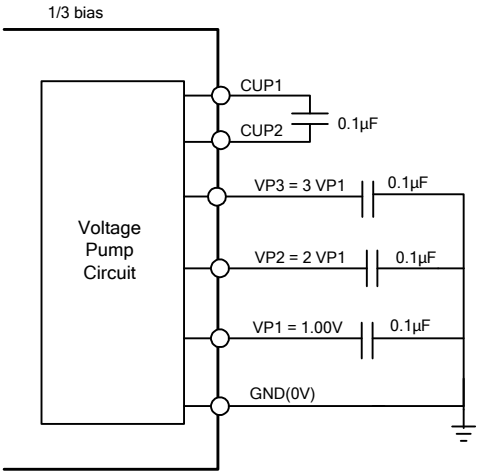
The LCD drive voltage (V_{LCD}) of Capacitor bias voltage mode is V_{DD}.



The capacitor bias voltage LCD driver contains a controller, a duty cycle generator, 4/5 Common signal pins and 32/31 Segment driver pins. Segment 1-32 and COM1-COM5 can also be shared as I/O port, it is controlled by the P0SS,P1SS, P2SS, P3SS, P4SS & P5SS register. The 32 bytes display data RAM is addressed to 500H-51FH, which could be used as data memory if needed.

Built-in voltage regulator LCD Driver

Buit-in voltage regulator, It's V_{DD} is between 1.8V and 3.6V, It can generate a stable voltage.



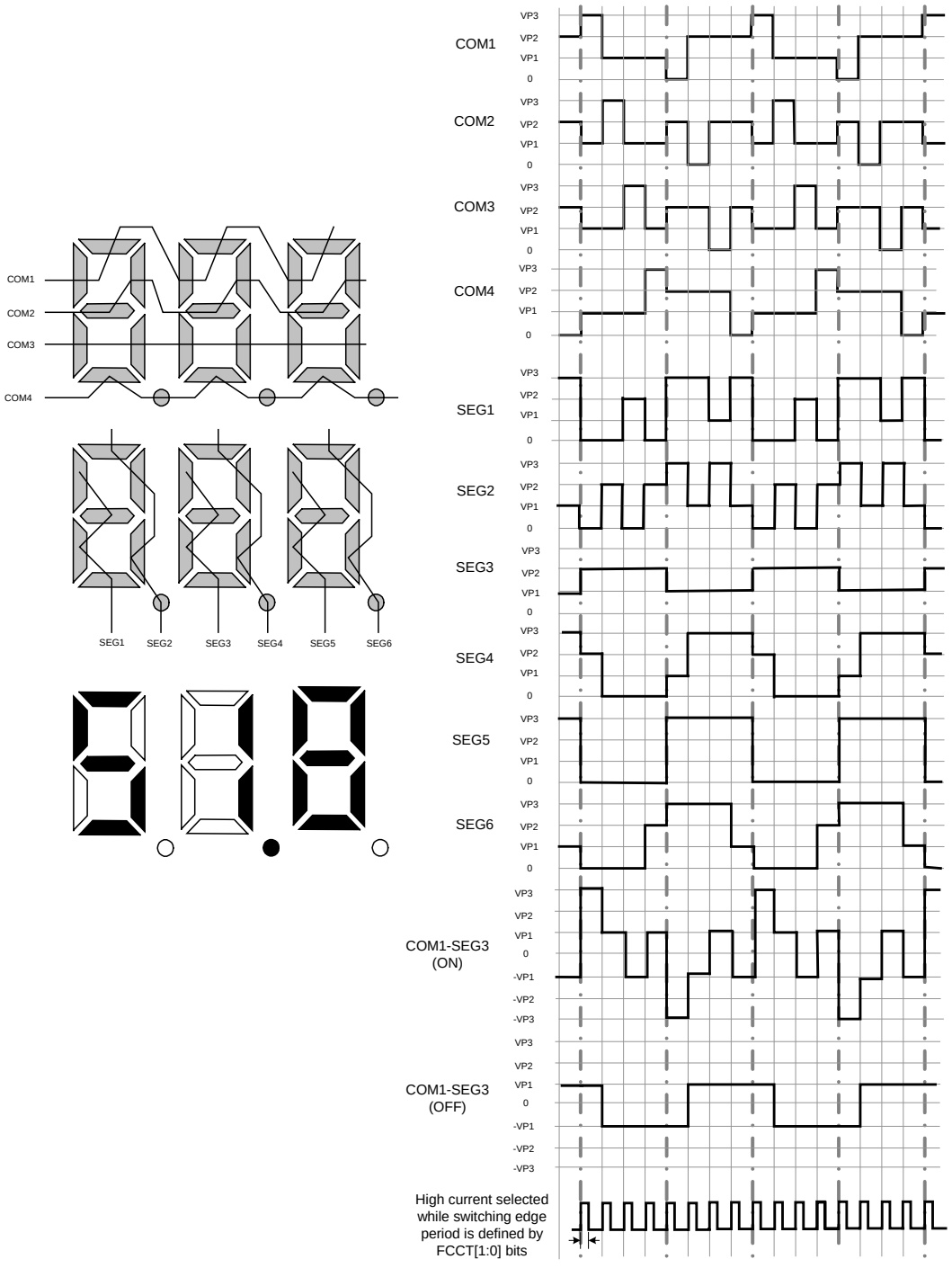
The capacitor LCD driver contains a controller,a voltage generator ,a duty cycle generator, 4/5 Common signal pins and 32/31 Segment driver pins. Segment 1-32 and COM1-COM5 can also be used as I/O port, it is controlled by the P0SS, P1SS, P2SS, P3SS, P4SS & P5SS register. The 32 bytes display data RAM is addressed to 500H-51FH, which could be used as data memory if needed.

Notes:

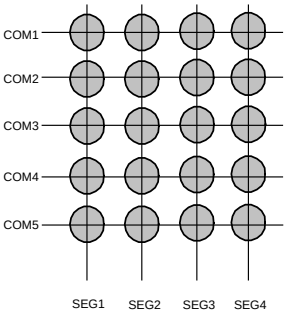
(1) When OP_LCDSEL = 1 and PUMPON = 1 in code option, P0.2 - P0.6 is LCD Pump port (VP1 - VP3、CUP1 - CUP2 function); otherwise P0.2 - P0.6 be used as I/O port.

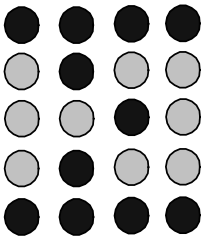
(2) For more efficient use of the capacitor LCD dirver, user must firstly set all control bit except PUMPON bit and LCDON bit, then set PUMPON bit, after delay of at least 50 ms, open LCD is that LCDON bit is set, light LCD panel.

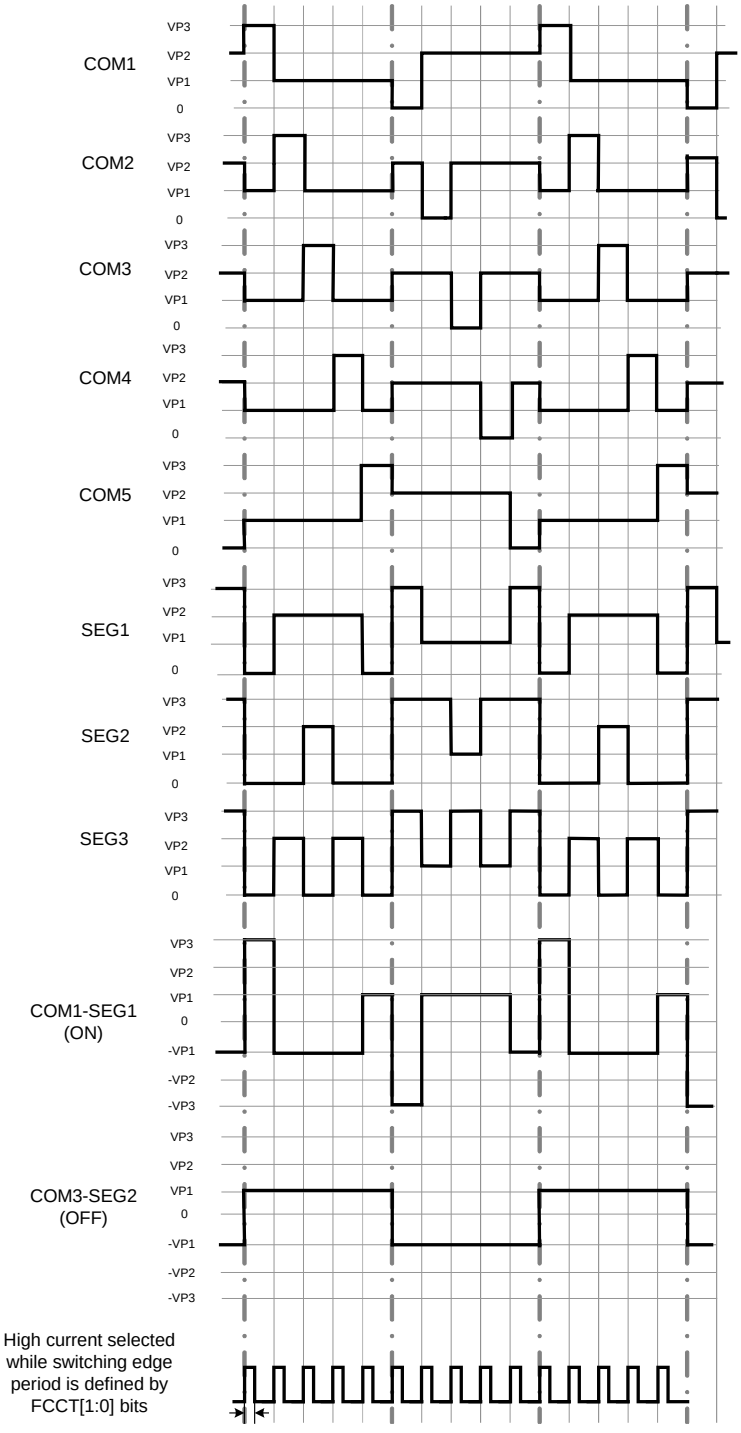
8.1.4 LCD Waveform



LCD display (1/4 duty, 1/3 bias)







LCD display ∑ (1/5 duty, 1/3 bias)

8.1.5 Register

Table 8.1 LCD Control Register

ABH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LCDCON	LCDON	PUMPON	DUTY	TYPESEL	VOL3	VOL2	VOL1	VOL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
7	**LCDON**	**LCD enable bit** 0: Disable LCD driver 1: Enable LCD driver
6	**PUMPON**	**PUMP on/off enable bit** 0: Disable LCD PUMP 1: Enable LCD PUMP ***Note:*** *capacitor bias and voltage regulator work when PUMPON = 1*
5	**DUTY**	**LCD duty selection bit** 0: 1/4 duty, 1/3 bias, P2.3 as segment or I/O 1: 1/5 duty, 1/3 bias, P2.3 as common
4	**TYPESEL**	**LCD capacitor drive mode selection bit** 0: capacitor bias voltage LCD drive mode 1: buit-in voltage regulator LCD drive mode
3-0	**VOL[3:0]**	**LCD contrast control bits** 0000: $V_{LCD} = 0.531V_{DD}$ 0001: $V_{LCD} = 0.563V_{DD}$ 0010: $V_{LCD} = 0.594V_{DD}$ 0011: $V_{LCD} = 0.625V_{DD}$ 0100: $V_{LCD} = 0.656V_{DD}$ 0101: $V_{LCD} = 0.688V_{DD}$ 0110: $V_{LCD} = 0.719V_{DD}$ 0111: $V_{LCD} = 0.750V_{DD}$ 1000: $V_{LCD} = 0.781V_{DD}$ 1001: $V_{LCD} = 0.813V_{DD}$ 1010: $V_{LCD} = 0.844V_{DD}$ 1011: $V_{LCD} = 0.875V_{DD}$ 1100: $V_{LCD} = 0.906V_{DD}$ 1101: $V_{LCD} = 0.938V_{DD}$ 1110: $V_{LCD} = 0.969V_{DD}$ 1111: $V_{LCD} = 1.000V_{DD}$ ***Note:*** *When capacitor LCD drive mode is selected, this four bits are invalid*

Table 8.2 LCD Control Register 1

AAH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LCDCON1	-	-	FCCTL1	FCCTL0	-	RLCD	MOD1	MOD0
R/W	-	-	R/W	R/W	-	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	0	0	-	0	0	0

Bit Number	Bit Name	Description
5-4	**FCCTL[1:0]**	**Fast charge time control bit** 00: 1/8 LCD com period 01: 1/16 LCD com period 10: 1/32 LCD com period 11: 1/64 LCD com period
2	**RLCD**	**LCD bias resistor control bit** 0: LCD bias resistor sum is 900K 1: LCD bias resistor sum is 1.5M
1-0	**MOD[1:0]**	**LCD Drive mode control bit** 00: traditional mode, bias resistor sum is 990K/1.5M 01: traditional mode, bias resistor sum is 60K 1x: fast charge mode, bias resistor sum switch between 60K and 990K/1.5M

Note: *When the capacitor LCD drive mode is selected, all bits in this register will be invalid.*

Table 8.3 LCD Control Register0

E7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DISPCLK0	-	-	-	-	-	-	DCK1	DCK0
R/W	-	-	-	-	-	-	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	-	-	0	0

Bit Number	Bit Name	Description
1-0	**DCK[1:0]**	**LCD clock frequency division selectiom bits** 00: divided by 4 01: divided by 3 10: divided by 2 11: divided by 1 ***Note:*** *only when the LCD clock selected 128K RC this register, this register is actived.*

Note:

(1) Option selected the dual clock, and the low frequency is 32.768K crystal, LCD clock source is external 32.768K crystal oscillator, fixed frame rate is 64Hz, DISPCLK0 register is invalid;

(2) Option selected the internal RC:

Option selected the32K RC, LCD clock source is 32K RC, fixed frame rate is 64Hz, DISPCLK0 register is invalid;

Option selected the other clock (include single high frequency clock), LCD clock source is 128K RC, set DCK[1:0] in DISPCLK0 register to select 1/4, 1/3, 1/2, 1/1 frequency diving ratio which corresponding 256/4Hz, 256/3Hz, 256/2Hz, 256/1Hz frame rate. Selected different duty, the frame rate will have a slight difference.

Table 8.4 LCD Pump clock Control Register

DFH (Bank0)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DISPCLK1	-	-	-	-	-	-	LCDPUMP1	LCDPUMP0
R/W	-	-	-	-	-	-	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	-	-	0	0

Bit Number	Bit Name	Description
1-0	**LCDPUMP[1:0]**	**LCD Pump clock Select bit** 00: 8KHz 01: 16KHz 10: 32KHz 11: 4KHz ***Note:*** *The faster the clock frequency, the stronger the LCD Pump drive power, the larger the power consumption.*

Table 8.5 P0 Mode Select Register

BFH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0SS	P0S7	-	-	-	-	-	P0S1	P0S0
R/W	R/W	-	-	-	-	-	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	-	-	-	-	-	0	0

Bit Number	Bit Name	Description
7	**P0SS.7**	**P0.7 port mode selection bit** 0: P0.7 is I/O 1: P0.7 is Segment (SEG13)
1-0	**P0SS[1-0]**	**P0.x port mode selection bit (x = 1/0)** 0: P0.1 - P0.0 is I/O 1: P0.1 - P0.0 is Segment (SEG14/15)

Table 8.6 P1 Mode Select Register

ADH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P1SS	P1S7	P1S6	P1S5	P1S4	P1S3	P1S2	P1S1	P1S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
7-0	**P1SS[7:0]**	**P1.x port mode selection bit (x = 7 - 0)** 0: P1.7 - P1.0 is I/O 1: P1.7 - P1.0 is segment (SEG12 - SEG5)

Table 8.7 P2 Mode Select Register

BBH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P2SS	P2S7	P2S6	P2S5	P2S4	P2S3	P2S2	P2S1	P2S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
7-0	**P2SS[7:0]**	**P2 port mode selection bit (x = 7 - 0)** 0: P2.7 - P2.0 is I/O 1: P2.3 - P2.0 is Segment (SEG1 - SEG4) P2.7 - P2.4 is Common (COM1 - COM4)

Note: *COM5 is selected through the DUTY bit in LCD Control Register.*

Table 8.8 P3 Mode Select Register

BCH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P3SS	P3S7	P3S6	P3S5	P3S4	P3S3	P3S2	P3S1	P3S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
7-0	**P3SS[7:0]**	**P3 port mode selection bit** 0: P3.7 - P3.0 is I/O 1: P3.7 - P3.0 is Segment (SEG25 - SEG32)

Table 8.9 P4 Mode Select Register

BDH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P4SS	-	P4S6	P4S5	P4S4	P4S3	P4S2	P4S1	P4S0
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
6-0	**P4SS[6:0]**	**P4 port mode selection bit** 0: P4.6 - P4.0 is I/O 1: P4.6 - P4.0 is Segment (SEG18 - SEG24)

Table 8.10 P5 Mode Select Register

BEH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P5SS	-	-	-	-	P5S3	P5S2	-	-
R/W	-	-	-	-	R/W	R/W	-	-
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	-	-

Bit Number	Bit Name	Description
3-2	**P5SS[3:2]**	**P5 port mode selection bit** 0: P5.3 - P5.2 is I/O 1: P5.3 - P5.2 is Segment (SEG16 - SEG17)

8.1.6 Configuration of LCD RAM

LCD 1/4 duty, 1/3 bias (COM1 - 4, SEG1 - 32)

Address	7	6	5	4	3	2	1	0
	-	-	-	-	COM4	COM3	COM2	COM1
500H	-	-	-	-	SEG1	SEG1	SEG1	SEG1
501H	-	-	-	-	SEG2	SEG2	SEG2	SEG2
502H	-	-	-	-	SEG3	SEG3	SEG3	SEG3
503H	-	-	-	-	SEG4	SEG4	SEG4	SEG4
504H	-	-	-	-	SEG5	SEG5	SEG5	SEG5
505H	-	-	-	-	SEG6	SEG6	SEG6	SEG6
506H	-	-	-	-	SEG7	SEG7	SEG7	SEG7
507H	-	-	-	-	SEG8	SEG8	SEG8	SEG8
508H	-	-	-	-	SEG9	SEG9	SEG9	SEG9
509H	-	-	-	-	SEG10	SEG10	SEG10	SEG10
50AH	-	-	-	-	SEG11	SEG11	SEG11	SEG11
50BH	-	-	-	-	SEG12	SEG12	SEG12	SEG12
50CH	-	-	-	-	SEG13	SEG13	SEG13	SEG13
50DH	-	-	-	-	SEG14	SEG14	SEG14	SEG14
50EH	-	-	-	-	SEG15	SEG15	SEG15	SEG15
50FH	-	-	-	-	SEG16	SEG16	SEG16	SEG16
510H	-	-	-	-	SEG17	SEG17	SEG17	SEG17
511H	-	-	-	-	SEG18	SEG18	SEG18	SEG18
512H	-	-	-	-	SEG19	SEG19	SEG19	SEG19
513H	-	-	-	-	SEG20	SEG20	SEG20	SEG20
514H	-	-	-	-	SEG21	SEG21	SEG21	SEG21
515H	-	-	-	-	SEG22	SEG22	SEG22	SEG22
516H	-	-	-	-	SEG23	SEG23	SEG23	SEG23
517H	-	-	-	-	SEG24	SEG24	SEG24	SEG24
518H	-	-	-	-	SEG25	SEG25	SEG25	SEG25
519H	-	-	-	-	SEG26	SEG26	SEG26	SEG26
51AH	-	-	-	-	SEG27	SEG27	SEG27	SEG27
51BH	-	-	-	-	SEG28	SEG28	SEG28	SEG28
51CH	-	-	-	-	SEG29	SEG29	SEG29	SEG29
51DH	-	-	-	-	SEG30	SEG30	SEG30	SEG30
51EH	-	-	-	-	SEG31	SEG31	SEG31	SEG31
51FH	-	-	-	-	SEG32	SEG32	SEG32	SEG32

LCD 1/5 duty, 1/3 bias (COM1 - 5, SEG2 - 32)

Address	7	6	5	4	3	2	1	0
	-	-	-	COM5	COM4	COM3	COM2	COM1
500H	-	-	-	-	-	-	-	-
501H	-	-	-	SEG2	SEG2	SEG2	SEG2	SEG2
502H	-	-	-	SEG3	SEG3	SEG3	SEG3	SEG3
503H	-	-	-	SEG4	SEG4	SEG4	SEG4	SEG4
504H	-	-	-	SEG5	SEG5	SEG5	SEG5	SEG5
505H	-	-	-	SEG6	SEG6	SEG6	SEG6	SEG6
506H	-	-	-	SEG7	SEG7	SEG7	SEG7	SEG7
507H	-	-	-	SEG8	SEG8	SEG8	SEG8	SEG8
508H	-	-	-	SEG9	SEG9	SEG9	SEG9	SEG9
509H	-	-	-	SEG10	SEG10	SEG10	SEG10	SEG10
50AH	-	-	-	SEG11	SEG11	SEG11	SEG11	SEG11
50BH	-	-	-	SEG12	SEG12	SEG12	SEG12	SEG12
50CH	-	-	-	SEG13	SEG13	SEG13	SEG13	SEG13
50DH	-	-	-	SEG14	SEG14	SEG14	SEG14	SEG14
50EH	-	-	-	SEG15	SEG15	SEG15	SEG15	SEG15
50FH	-	-	-	SEG16	SEG16	SEG16	SEG16	SEG16
510H	-	-	-	SEG17	SEG17	SEG17	SEG17	SEG17
511H	-	-	-	SEG18	SEG18	SEG18	SEG18	SEG18
512H	-	-	-	SEG19	SEG19	SEG19	SEG19	SEG19
513H	-	-	-	SEG20	SEG20	SEG20	SEG20	SEG20
514H	-	-	-	SEG21	SEG21	SEG21	SEG21	SEG21
515H	-	-	-	SEG22	SEG22	SEG22	SEG22	SEG22
516H	-	-	-	SEG23	SEG23	SEG23	SEG23	SEG23
517H	-	-	-	SEG24	SEG24	SEG24	SEG24	SEG24
518H	-	-	-	SEG25	SEG25	SEG25	SEG25	SEG25
519H	-	-	-	SEG26	SEG26	SEG26	SEG26	SEG26
51AH	-	-	-	SEG27	SEG27	SEG27	SEG27	SEG27
51BH	-	-	-	SEG28	SEG28	SEG28	SEG28	SEG28
51CH	-	-	-	SEG29	SEG29	SEG29	SEG29	SEG29
51DH	-	-	-	SEG30	SEG30	SEG30	SEG30	SEG30
51EH	-	-	-	SEG31	SEG31	SEG31	SEG31	SEG31
51FH	-	-	-	SEG32	SEG32	SEG32	SEG32	SEG32

8.2 PWM 1(Pulse Width Modulation)

8.2.1 Feature

- Support one 12-bit PWM1 output, can also be used as 12-bit timer or remote carrier generator
- Selectable output polarity

The SH79F3252 has one bult-in 12-bit PWM1 module, which can generate pulse width modulation waveform with an adjustable period or duty cycle. PWM1CON controls the clock source of PWM1of which period is controlled by PWM1PH/L and the duty cycle is controlled by PWM1DH/L.

8.2.2 Register

Table 8.11 PWM1 Control Register

DCH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM1CON	PWM1EN	PWM1S	PWM1CK2	PWM1CK1	PWM1CK0	PWM1IE	PWM1IF	PWM1SS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
7	**PWM1EN**	**PWM1 Control bit** 0: Disable PWM1 1: Enable PWM1
6	**PWM1S**	**PWM1 Output Mode** 0: high active, PWM1 output high during duty time, output low during remain period time 1: low active, PWM1 output low during duty time, output high during remain period time
5-3	**PWM1CK[2:0]**	**PWM1 clock selection bits** 000: System clock/1 001: System clock/2 010: System clock/4 011: System clock/8 100: System clock/16 101: System clock/32 110: System clock/64 111: System clock/128
2	**PWM1IE**	**PWMx interrupt enable bit（when set EPWM1 bit to 1 in IEN1 register）** 0: PWM1 period interrupt Disable 1: PWM1 period interrupt Enable
1	**PWM1IF**	**PWM1 interrupt flag** 0: the PWM1 period counter no overflow 1: the PWM1 period counter overflow, Set by hardware, cleared by software
0	**PWM1SS**	**PWMx pin output control bit** 0: PWM1output disable, PWM1 as I/O ***Note:*** *if this bit is 0 but PWMxEN = 1, the PWM1 timer can work normally, only can not output waveform, the PWM1 still can be used as a timer.* 1: PWM1 output enable ***Note****: if this bit is 1 but PWMxEN = 0, the PWM1 output unselected level (selected high, output low;selected low, output high).*

Table 8.12 PWM1 Control Register

DEH-DDH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM1PH	-	-	-	-	PWM1P.11	PWM1P.10	PWM1P.9	PWM1P.8
PWM1PL	PWM1P.7	PWM1P.6	PWM1P.5	PWM1P.4	PWM1P.3	PWM1P.2	PWM1P.1	PWM1P.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
3-0 7-0	**PWM1P[11:0]**	**12 bits PWM1 period register**

PWM1 output period cycle = [**PWM1PH**, **PWM1PL**] X PWM clock period

PWM1 counter arrived the value in PWM1PH/L, it will clear to 0. When PWM1PH/L = 0, if PWM1S is 0,the PWM1 output low; if PWM1S is 1, the PWM1 output high.

Note: *The modified reloading counter value will take effect in the next period. First set the low Byte, then the high Byte. Note that even if the high constant value keep unchanged, it also need to rewrite once, otherwise, the low modify is invalid.*

Table 8.13 PWM1 Duty Control Register

B7H-B6H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM1DH	-	-	-	-	PWM1D.11	PWM1D.10	PWM1D.9	PWM1D.8
PWM1DL	PWM1D.7	PWM1D.6	PWM1D.5	PWM1D.4	PWM1D.3	PWM1D.2	PWM1D.1	PWM1D.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
3-0 7-0	**PWM1D[11-0]**	**PWM1 Duty control bits, control the duty output time of PWM1** 1. When PWM1P ≤ PWM1D If PWM1S = 0, the PWM1 output high If PWM1S = 1, the PWM1 output low 2. When PWM1D = 00H If PWM1S = 0, the PWM1 output low If PWM1S = 1, the PWM1 output high

Note:

(1) The modified reloading counter value will take effect in the next period. First set the low Byte, then the high Byte. Note that even if the high constant value keep unchanged, it also need to rewrite once, otherwise, the low modify is invalid.

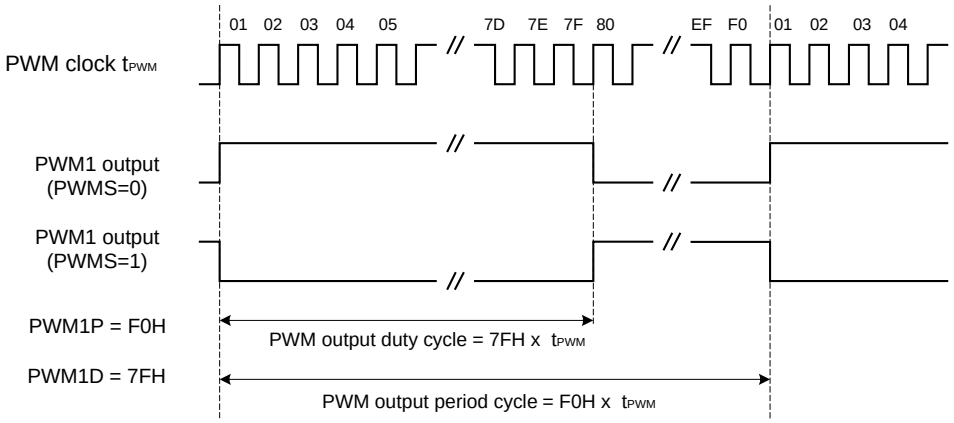
(2) PWM1EN bit can enable PWM1 modules.

(3) OP_PWM_REM_IOSEL can select whether P1.2 or P0.0 is used as IO port or PWM1 output port.

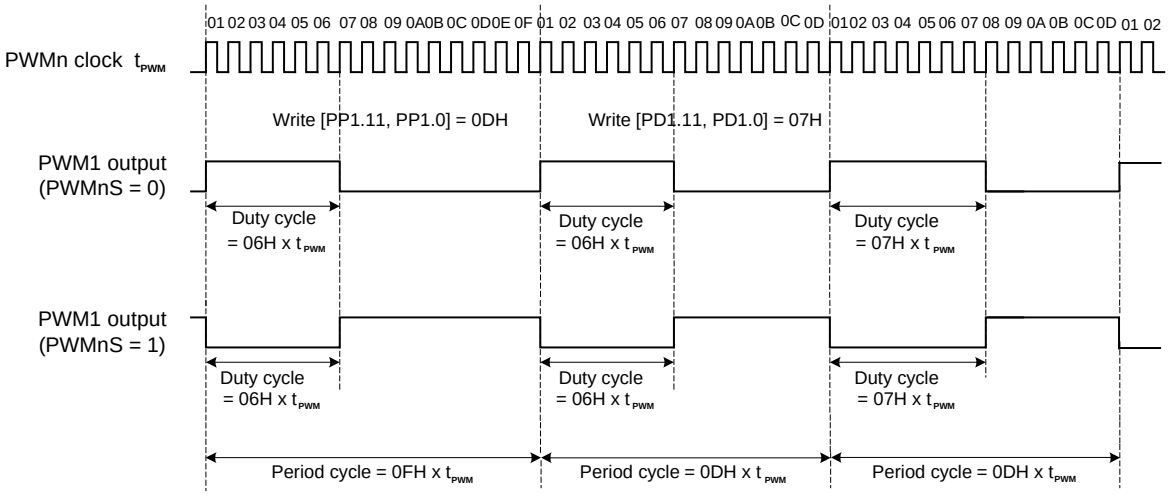
(4) PWM1SS bit can select whether P1.2 or P0.0 is used as IO port or PWM1 output port.

(5) The EPWM1 bit in IEN1 register and the PWM1IE bit in PWM1CON register can enable/disable the PWM1 interrupt.

(6) If set PWM1EN bit to 1, the PWM1 module active,but PWM1SS = 0, the PWM1 output closed, the PWM1 still can be used as a 12 bit timer, at this time, if the EPWM1bit in IEN1 register is 1, PWM1 interrupt will generate.



PWM Output Example



PWM Output Period or Duty Cycle Changing Example

8.3 The infrared module based on PWM1 (REM)

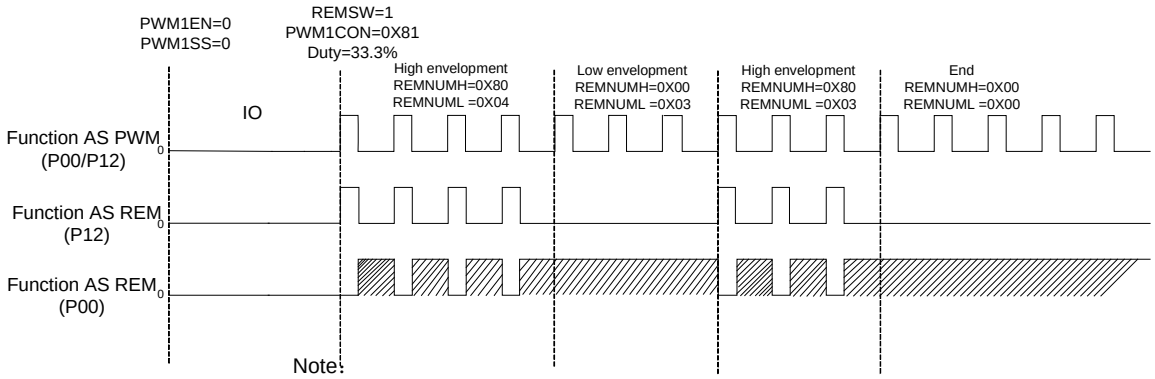
The infrared emission principle:

(1) Transmit envelope time of the infrared emission to carrier number (REMNUMH: REMNUML), set thecarrier number in the envelope register and start sending by software.

(2) Number of carriers in envelope will be sent by hardware, so MCU can do other tasks during the infrared emission.

(3) Hardware automatically load carrier number in the next envelope (REMNUMH: REMNUML) after transmission of carriers in this envelope.

(4) When hardware load REMNUMH[5:0] & REMNUML[7:0] which are 0, infrared diode can't generate REM wave.
If Option selected P0.0 as REM port, the P0.0 can output high resistance;
If Option selected P1.2 as REM port, the P1.2 can output Low level.



Note:
1.P00 can only output L level and High resistance(the shaded part is high resistance);
2.P12 can output L and H level.

Table 8.14 Infrared Emission Control Register

D9H (Bank0)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
REMCON	-	-	-	-	-	-	REMIF	REMSW
R/W	-	-	-	-	-	-	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	-	-	0	0

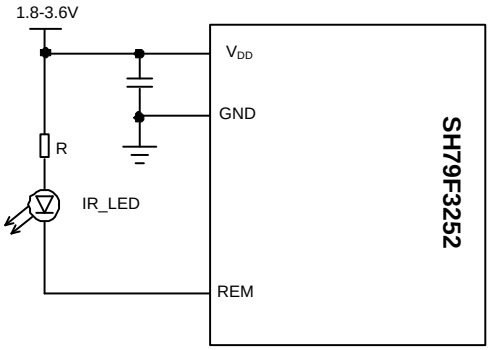
Bit Number	Bit Name	Description
1	**REMIF**	**Infrared Interrupt Flag** 0: REM envelope timer no overflow 1: REM envelope timer overflow, set by hardware, cleared by hardware
0	**REMSW**	**Infrared Enable bit (when PWM1SS is set to 1, this configuration bit will be valid)** 0: P0.0 (P1.2) as PWM1 output 1: P0.0 (P1.2) as infrared application ***Note:*** *P0.0 or P1.2 is selected as REM port by option.* *If P0.0 is selected as REM port, the port is high-impedance or low level;* *If P1.2 is selected as REM port, the port is high level or low level.*

Note: *according to the actual needs, REM ports choose different IO ports and current perfusion capability by Option option, P1.2 port is a common Sink current capability, and P0.0 can choose different Sink current capability.*

Table 8.15 Infrared Emission Envelope Carrier Number Register

DAH (Bank0)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
REMNUMH	REMHLSIGN	-	REMNUMH.5	REMNUMH.4	REMNUMH.3	REMNUMH.2	REMNUMH.1	REMNUMH.0
R/W	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	-	0	0	0	0	0	0
DBH (Bank0)	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
REMNUML	REMNUML.7	REMNUML.6	REMNUML.5	REMNUML.4	REMNUML.3	REMNUML.2	REMNUML.1	REMNUML.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
7	**REMHLSIGN**	**Infrared Diode Envelope Level Flag** 0: Low envelope (infrared diode is closed, time: carrier number X Tpwm1) 1: High envelope (infrared diode transmit, time: carrier number X Tpwm1, carrier number is up to RMMNUM, RENMNUL)
5-0	**REMNUMH.x**	**High byte of Infrared Diode Envelope Carrier Number Control, y = 0 - 5**
7-0	**REMNUML.x**	**Low byte of Infrared Diode Envelope Carrier Number Control, x = 0 - 7**



Typical Application Circuit

(R selection: please selecte according to infrared diode parameters and REM drive current configuration in code option)

Note:

(1) the upper REM port uses the large sink capability of P0.0.

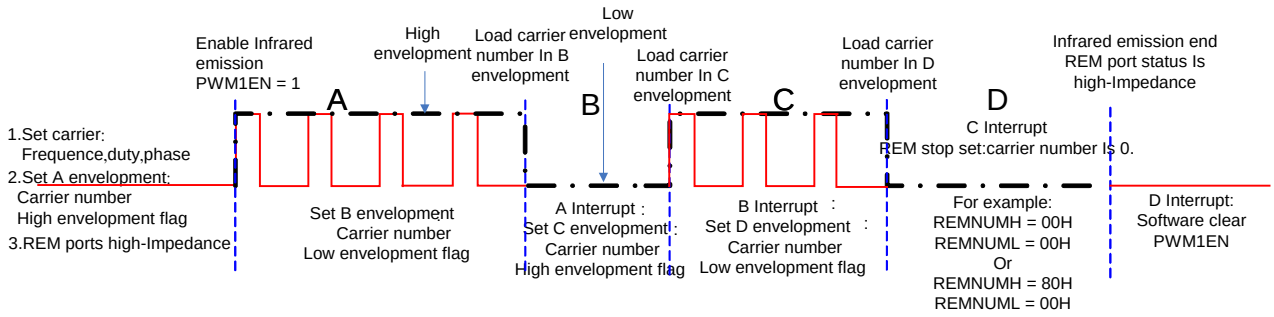
(2) when the application circuit is used, the P0.0 port should not be set to low output before the REM port is configured.

P0.0 as REM port, Reference program to generate 38KHZ carrier
REM ports transmit A B C D carrier (AS shown in **Infrared Diode Emission Voltage Waveform**)

```
/*Envelope carrier number in auiRemCod code:
High 8-bit: high 6-bit data and high/low envelope flag
Low 8-bit: low 8-bit data
*/
char g_auiRemCode[5][2] = {{0x80,0x04},{0x00,0x02},{0x80,0x03},{0x00,0x03},{0x00,0x00}};
                          /*  A          B          C          D          end  */

void REM_InitCarrier(void)
{
        REMCON      |= 0x01;                  // P0.0 as REM port
        PWM1CON     = 0x01;                  //high level drive, select REM function, select  system clock
        PWM1PL      = 0x69;
        PWM1PH      = 0x00;                  // Set carrier frequence to 38kHz
        PWM1DL      = 0x23;
        PWM1DH      = 0x00;                  // Set carrier duty to 33%
        REMNUMH      = g_auiRemCode[0][0];   // Set 38kHz carrier number in A envelope, high envelope flag
        REMNUML      = g_auiRemCode[0][1];
        IEN1         |= 0x02;                // Enable REM interrupt
        IEN0        |= 0x80;                 // Enable all interrupt
        PWM1CON      |= 0x80;                // PWM output
        REMNUMH     = g_auiRemCode[1][0];   // Set 38kHz carrier number in B envelope, low envelope flag
        REMNUML      = g_auiRemCode[1][1];
}
void REM_IntSetInfrared(void)  interrupt  8
{
    static unsigned  int i = 1;
        unsigned  int j = 0;
        i = i + 1;

        /*If REMNUMH and REMNUML are all 0, The infrared emission will end */
        if((REMNUML == 0x00)&&(REMNUMH == 0x00))
        {
                /*Software close PWM wave*/
                PWM1CON &= 0x7F ;
                i = 1;
        }
        else
        {
                /*Set carrier number in the next envelope and high envelope flag*/
                REMNUMH = g_auiRemCode[i][j];
                REMNUML = g_auiRemCode[i][j+1];
        }
}
```



Infrared Diode Emission Voltage Waveform

8.4 EUART0

8.4.1 Features

- The SH79F3252 has one enhanced EUART0
- 15-bit up counter withthe baud rate generator
- Enhancements over the standard 8051 the EUART include Framing Error detection and automatic address recognition
- The EUART0 can be operated in four modes

Note: *when EUART is used, system must switch to 8MHz.*

8.4.2 Mode Description

The EUARTx can be operated in 4 modes. Users must initialize the SCON before any communication can take place. This involves selection of the Mode and the baud rate.

In all of the 4 modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. This will generate a clock on the TxD pin and shift in 8 bits on the RxD pin. Reception is initiated in the other modes by the incoming start bit if RI = 0 and REN = 1. The external transmitter will start the communication by transmitting the start bit.

EUART Mode Summary

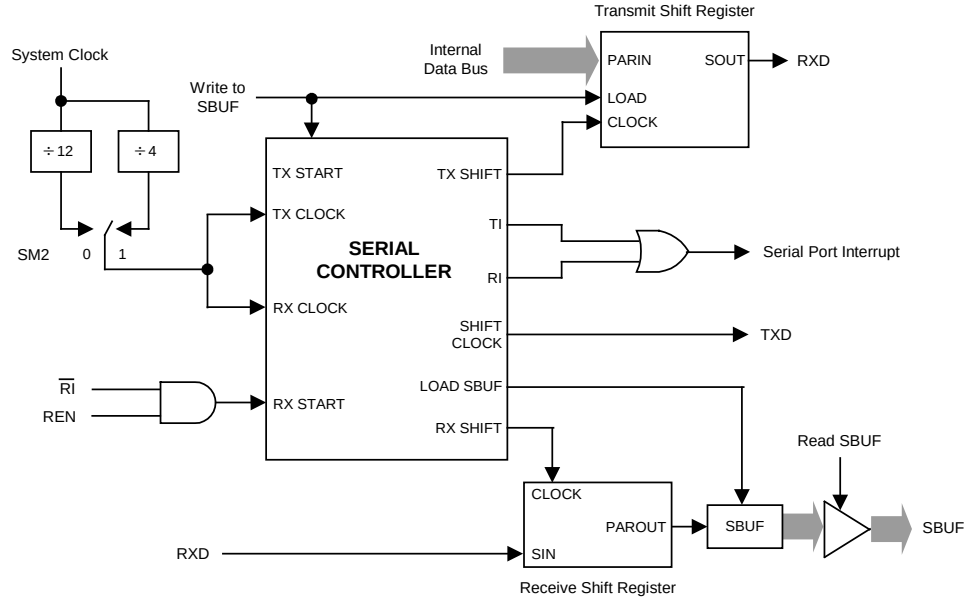
SM0	SM1	Mode	Type	Baud Clock	Frame Size	Start Bit	Stop Bit	9th bit
0	0	0	Sych	f_{SYS}/(4 or 12)	8 bits	NO	NO	None
0	1	1	Ansych	overflow rate of baud rate generator/16	10 bits	1	1	None
1	0	2	Ansych	f_{SYS}/(32 or 64)	11 bits	1	1	0, 1
1	1	3	Ansych	overflow rate of baud rate generator/16	11 bits	1	1	0, 1

Mode0: Synchronous Mode, Half duplex

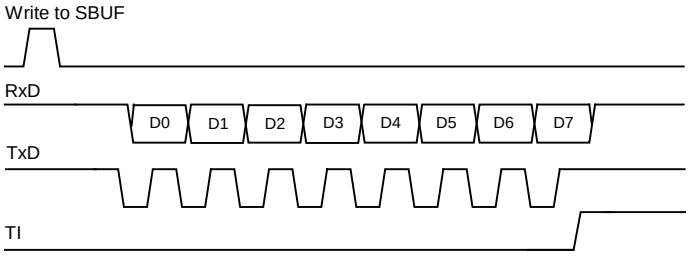
This mode provides synchronous communication with external devices. In this mode serial data is transmitted and received on the RxD line. TxD is used to output the shift clock. The TxD clock is provided by the SH79F3252 whether the device is transmitting or receiving. This mode is therefore a half duplex mode of serial communication. In this mode, 8 bits are transmitted or received per frame. The LSB is transmitted/received first.

The baud rate is programmable to either 1/12 or 1/4 of the system clock. This baud rate is determined in the SM2 bit (SCON.5). When this bit is set to 0, the serial port runs at 1/12 of the system clock. When set to 1, the serial port runs at 1/4 of the system clock.

The functional block diagram is shown below. Data enters and exits the serial port on the RxD line. The TxD line is used to output the SHIFT CLOCK. The SHIFT CLOCK is used to shift data into and out of the SH79F3252.

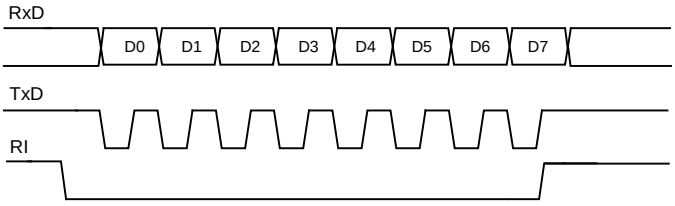


Any instruction that uses SBUF as a destination register ("write to SBUF" signal) will start the transmission. The next system clock tells the Tx control block to commence a transmission. The data shift occurs at the falling edge of the SHIFT CLOCK, and the contents of the transmit shift register is shifted one position to the right. As data bits shift to the right, zeros come in from the left. After transmission of all 8 bits in the transmit shift register, the Tx control block will deactivates SEND and sets TI (SCON.1) at the rising edge of the next system clock.



Send Timing of Mode 0

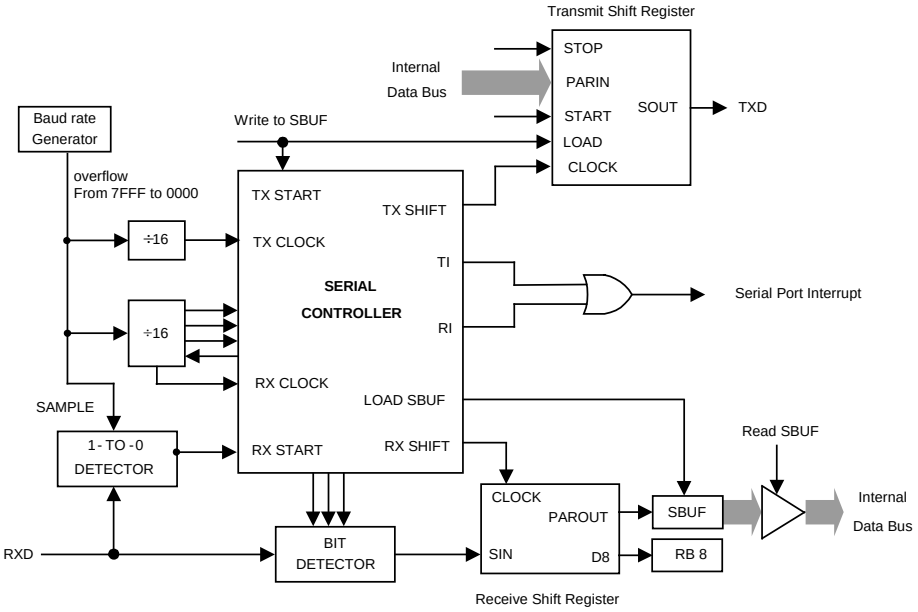
Reception is initiated by the condition REN (SCON.4) = 1 and RI (SCON.0) = 0. The next system clock activates RECEIVE. The data latch occurs at the rising edge of the SHIFT CLOCK, and the contents of the receive shift register are shifted one position to the left. After the receiving of all 8 bits into the receive shift register, the RX control block will deactivates RECEIVE and sets RI at the rising edge of the next system clock, and the reception will not be enabled till the RI is cleared by software.



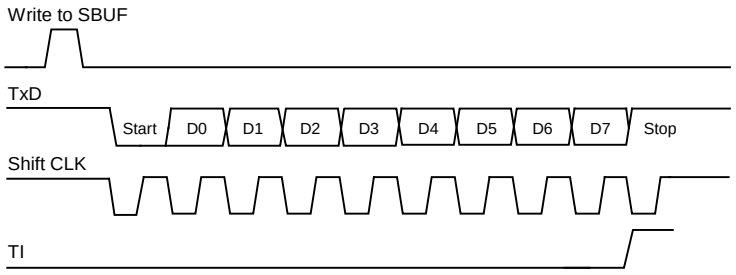
Receive Timing of Mode 0

Mode1: 8-Bit EUARTx, Variable Baud Rate, Asynchronous Full-Duplex

This mode provides the 10 bits full duplex asynchronous communication. The 10 bits consist of a start bit (logical 0), 8 data bits (LSB first), and a stop bit (logical 1). When receiving, the eight data bits are stored in SBUF and the stop bit goes into RB8 (SCON.2). The baud rate in mode1 is its own baud rate generator overflow rate/16. The functional block diagram is shown below.



Transmission begins with a “write to SBUF” signal, and it actually commences at the next system clock following the next rollover in the divide-by-16 counter (divide baud-rate by 16), thus, the bit times are synchronized to the divide-by-16 counter, not to the “write to SUBF” signal. The start bit is firstly put out on TxD pin, then are the 8 bits of data. After all 8 bits of data in the transmit shift register are transmitted, the stop bit is put out on the TxD pin, and the TI flag is set at the same time that the stop is send.



Send Timing of Mode 1

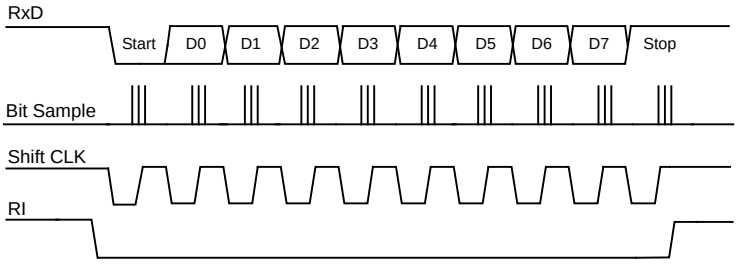
Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data with the detection of a falling edge on the RxD pin. For this purpose RxD is sampled at the rate of 16 times baud rate. When a falling edge is detected, the divide-by-16 counter is immediately reset. This helps to align the bit boundaries with the rollovers of the divide-by-16 counter.The 16 states of the counter divide each bit time into 16ths. The bit detector samples the value of RxD at the 7^{th}, 8^{th} and 9^{th} counter states of each bit time. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done for noise rejection. If the first bit after the falling edge of RxD pin is not 0, which indicates an invalid start bit, and the reception is immediately aborted. The receive circuits are reset and again waiting for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the shift register. After shifting in 8 data bits and the stop bit, the SBUF and RB8 are loaded and RI are set if the following conditions are met:

(1) RI must be 0

(2) Either SM2 = 0, or the received stop bit = 1

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost.

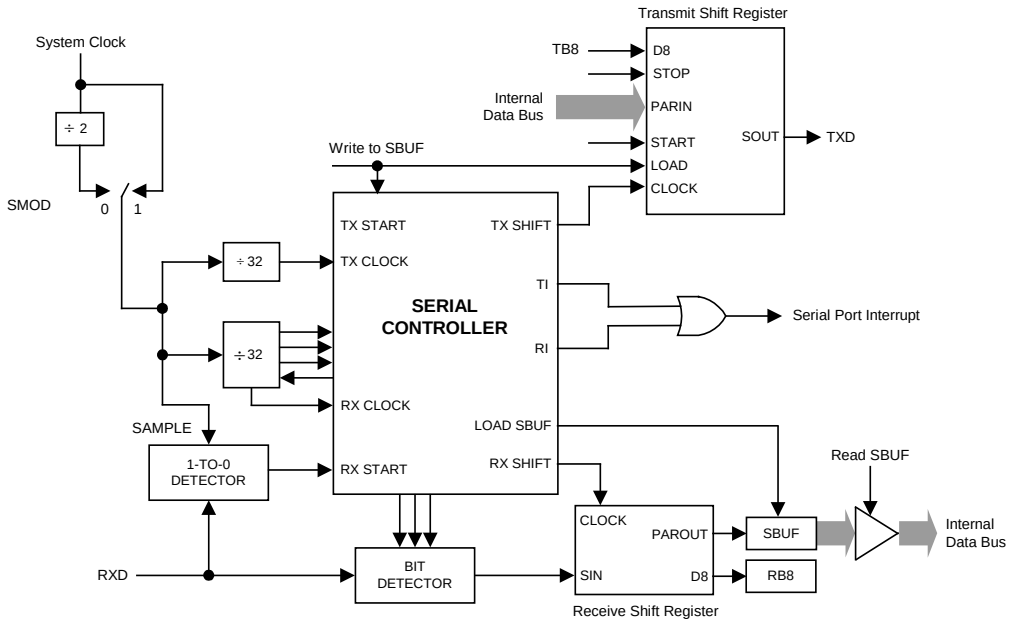
At the time, the receiver goes back to looking for another falling edge on the RxD pin. And the user should clear RI by software for further reception.



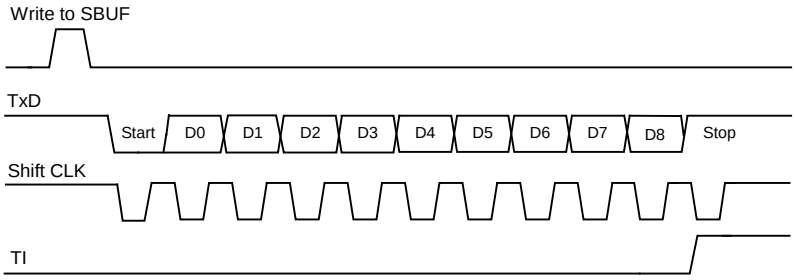
Receive Timing of Mode 1

Mode2: 9-Bit EUART, Fixed Baud Rate, Asynchronous Full-Duplex

This mode provides the 11 bits full duplex asynchronous communication. The 11 bit consists of one start bit (logical 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logical 1). Mode 2 supports multiprocessor communications and hardware address recognition (Refer to Multiprocessor Communication Section for details). When data is transmitted, the 9th data bit (TB8 in SCON) can be assigned the value of 0 or 1, for example, the parity bit P in the PSW or used as data/address flag in multiprocessor communications. When data is received, the 9th data bit goes into RB8 and the stop bit is not saved. The baud rate is programmable to either 1/32 or 1/64 of the system working frequency, as determined by the SMOD bit in PCON. The functional block diagram is shown below.



Transmission begins with a “write to SBUF” signal, the “write to SBUF” signal also loads TB8 into the 9th bit position of the transmit shift register. Transmission actually commences at the next system clock following the next rollover in the divide-by-16 counter (thus, the bit times are synchronized to the divide-by-16 counter, not to the “write to SUBF” signal). The start bit is firstly put out on TxD pin, then are the 9 bits of data. After all 9 bits of data in the transmit shift register are transmitted, the stop bit is put out on the TxD pin, and the TI flag is set at the same time, this will be at the 11th rollover of the divide-by-16 counter after a write to SBUF.



Send Timing of Mode 2

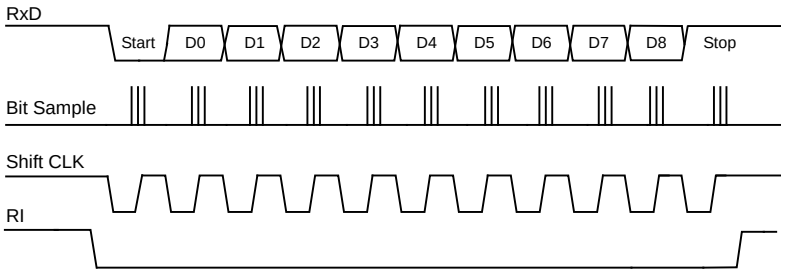
Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. For this purpose RxD is sampled at the rate of 16 times baud rate. When a falling edge is detected, the divide-by-16 counter is immediately reset. This helps to align the bit boundaries with the rollovers of the divide-by-16 counter. The 16 states of the counter divide each bit time into 16ths. The bit detector samples the value of RxD at the 7th, 8th and 9th counter state of each bit time. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done for noise rejection. If the first bit detected after the falling edge of RxD pin is not 0, which indicates an invalid start bit, and the reception is immediately aborted. The receive circuits are reset and again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the shift register. After shifting in 9 data bits and the stop bit, the SBUF and RB8 are loaded and RI is set if the following conditions are met:

(1) RI must be 0

(2) Either SM2 = 0, or the received 9th bit = 1 and the received byte accords with Given Address

If these conditions are met, then the 9th bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost.

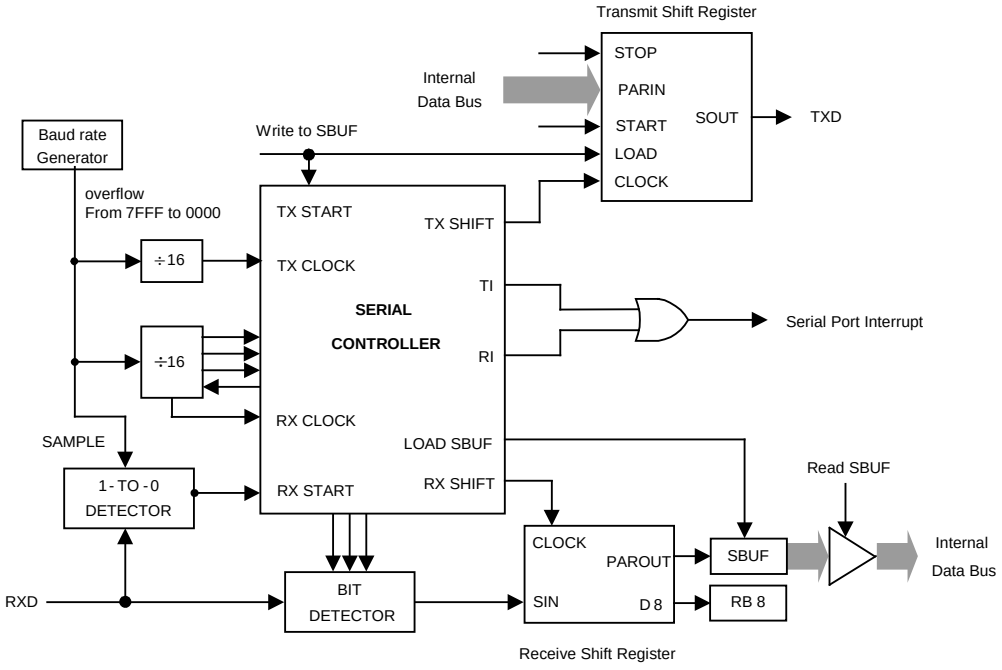
At the time, the receiver goes back to looking for another falling edge on the RxD pin. And the user should clear RI by software for further reception.



Receive Timing of Mode 2

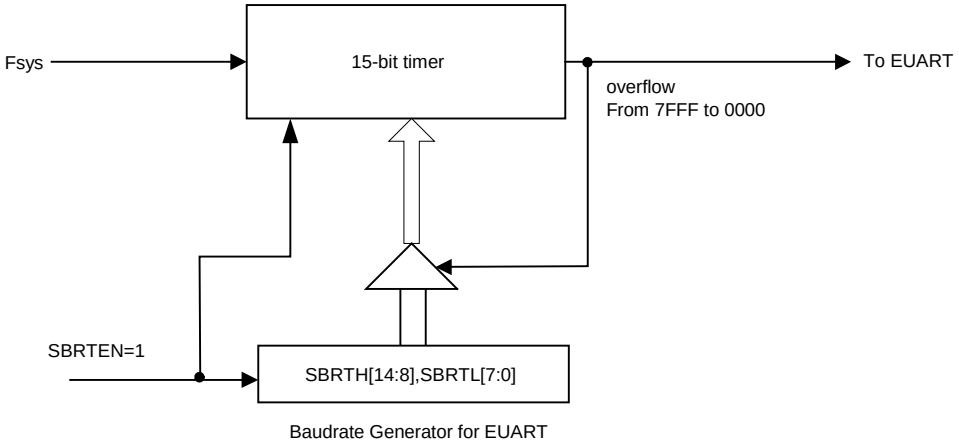
Mode3: 9-Bit EUARTx, Variable Baud Rate, Asynchronous Full-Duplex

Mode3 uses transmission protocol of the Mode2 and baud rate generation of the Mode1.



8.4.3 Adjustable Baud Rate

EUART has its own baud rate generator, which is actually a 15-bit up counter.



Baudrate Generator for EUART

From the figure, the baud rate generator overflow rate:

$$\text{SBRToverflowrate} = \frac{\text{Fsys}}{32768 - \text{SBRT}}, \text{SBRT} = [\text{SBRTH}, \text{SBRTL}]。$$

Therefore, EUARTx baud rate calculation formula in each mode is as follows:

In Mode0, the baud rate is programmable to be either 1/12 or 1/4 of the system frequency. This baud rate is determined by SMx2 bit. When set to 0, the serial port runs at 1/12 of the system clock. When set to 1, the serial port runs at 1/4 of the system clock.

The baud rate can be adjust at a accuracy of one system clock period in Mode1 & Mode3, the formula is as follows:

$$\text{BaudRate} = \frac{\text{Fsys}}{16 \times \left(32768 - \text{SBRT}\right) + \text{BFINE}}$$

For example: If you want to get the baud rate of 19200Hz in condition of Fsys = 4MHz, SBRT and SFINE value is calculated as follows:

4000000/16/19200 = 13.02

SBRT = 32768 - 13 = 32755

19200 = 4000000/(16 X 13 + SFINE)

SFINE = 0.33 $\approx$ 0

The actual baud calculated according to this fine-tuning mode is 19230 with 0.16% error which will be 8.5% in the past.

In Mode2, the baud rate is programmable to either 1/32 or 1/64 of the system clock. This baud rate is determined by the SMOD bit (PCON.7). When this bit is set to 0, the serial port runs at 1/64 of the clock. When set to 1, the serial port runs at 1/32 of the clock.

8.4.4 Multi-Processor Communicatio

Software Address Recognition

Modes 2 and 3 of the EUART have a special provision for multi-processor communication. In these modes, 9 data bits are received. The 9th bit goes into RB8. Then a stop bit follows. The EUART can be programmed such that when the stop bit is received, the EUART interrupt will be activated (i.e. the request flag RI is set) only if RB8 = 1. This feature is enabled by setting the bit SM2 in SCON.

A way to use this feature in multiprocessor communications is as follows. If the master processor wants to transmit a block of data to one of the several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte.

With SM2 = 1, no other slave will be interrupted by a data byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will be coming. After having received a complete message, the slave sets SM2 again. The slaves that were not addressed leave their SM2 set, ignoring the incoming data bytes.

Note: *In Mode0, SM2 is used to select baud rate doubling. In Mode1, SM2 can be used to check the validity of the stop bit. If SM2 = 1 in Mode1, the receive interrupt will not be activated unless a valid stop bit is received.*

Automatic (Hardware) Address Recognition

In Mode2 & 3, setting the SM2 bit will configure EUART act as following: when a stop bit is received, EUART will generate an interrupt only if the 9th bit that goes into RB8 is logic 1 (address byte) and the received data byte matches the EUART slave address. Following the received address interrupt, the slave should clear its SM2 bit to enable interrupts on the reception of the following data byte(s).

The 9-bit mode requires that the 9th information bit is a 1 to indicate that the received information is an address and not data. When the master processor wants to transmit a block of data to one of the slaves, it first sends out the address of the targeted slave (or slaves). All the slave processors should have their SM2 bit set high when waiting for an address byte, which ensures that they will be interrupted only by the reception of an address byte. The Automatic address recognition feature further ensures that only the addressed slave will be interrupted. The address comparison is done by hardware not software.

After being interrupted, the addressed slave clears the SM2 bit to receive data bytes. The un-addressed slaves will be unaffected, as they will be still waiting for their address. Once the entire message is received, the addressed slave should set its SM2 bit to ignore all transmissions until it receives the next address byte.

The Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given Address. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave's address, SADDR, and the address mask, SADEN. The slave address is an 8-bit value specified in the SADDR register. The SADEN register is actually a mask for the byte value in SADDR. If a bit position in SADEN is 0, then the corresponding bit position in SADDR is don't care. Only those bit positions in SADDR whose corresponding bits in SADEN are 1 are used to obtain the Given Address. This gives the user flexibility to address multiple slaves without changing the slave address in SADDR.

	Slave 1	**Slave 2**
SADDR	10100100	10100111
SADEN (0 mask)	11111010	11111001
Given Address	10100x0x	10100xx1
Broadcast Address (SADDR or SADEN)	1111111x	11111111

The Given address for slave 1 and 2 differ in the LSB. For slave 1, it doesn't care, while for slave 2 it is 1. Thus to communicate only with slave 1, the master must send an address with LSB = 0 (10100000). Similarly the bit 1 is 0 for slave 1 and don't care for slave 2. Hence to communicate only with slave 2 the master has to transmit an address with bit 1 = 1 (1010 0011). If the master wishes to communicate with both slaves simultaneously, then the address must have bit 0 = 1 and bit 1 = 0. The bit 2 position is don't care for both the slaves. This allows two different addresses to select both slaves (1010 0001 and 1010 0101).

The master can communicate with all the slaves simultaneously with the Broadcast Address. This address is formed from the logical OR of the SADDR and SADEN. The zeros in the result are defined as don't cares. In most cases, the Broadcast Address is FFh, this address will be acknowledged by all slaves.

On reset, the SADDR and SADEN are initialized to 00h. This results in Given Address and Broadcast Address being set as XXXXXXXX (all bits don't care). This effectively removes the multiprocessor communications feature, since any selectivity is disabled. This ensures that the EUARTx will reply to any address, which it is backwards compatible with the 80C51 microcontrollers that do not support automatic address recognition. So the user may implement multiprocessor by software address recognition mentioned above.

8.4.5 Error Detection

Error detection is available when the SSTAT bit in register PCON is set to logic 1.The SSTAT bit must be logic 1 to access any of the status bits (FE, RXOV, and TXCOL). The SSTAT bit must be logic 0 to access the Mode Select bits (SM0, SM1, and SM2).All the 3 bits should be cleared by software after they are set, even when the following frames received without any error will not be cleared automatically.

Transmit Collision

The Transmit Collision bit (TXCOL bit in register SCON) reads '1' if RI is set 0 and user software writes data to the SBUF register while a transmission is still in progress. If this occurs, the new data will be ignored and the transmit buffer will not be written.

Receive Overrun

The Receive Overrun bit (RXOV in register SCON) reads '1' if a new data byte is latched into the receive buffer before software has read the previous byte. The previous data is lost when this happen.

Frame Error

The Frame Error bit (FE in register SCON) reads '1' if an invalid (low) STOP bit is detected.

Stop Detection

When detectied 11 bits low continuously, considered a pause has been detected. Because the condition of pause can satisfied the condition of frame error , the frame error flag will be set to 1 when detected a pause. Once pause condition has been detected, the UART will enter the idle state and keep it until receive an active stop bit (a rising edge in RXDx pin).

8.4.6 Register

Table 8.16 EUART Control & Status Register

98H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SCON	SM0 /FE	SM1 /RXOV	SM2 /TXCOL	REN	TB8	RB8	TI	RI
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
7-6	**SM[0:1]**	**EUART0 Serial mode control bit, when SSTAT = 0** 00: mode 0, Synchronous Mode, fixed baud rate 01: mode 1, 8 bit Asynchronous Mode, variable baud rate 10: mode 2, 9 bit Asynchronous Mode, fixed baud rate 11: mode 3, 9 bit Asynchronous Mode, variable baud rate
7	**FE**	**EUART0 Frame Error flag, when FE bit is read, SSTAT bit must be set 1** 0: No Frame Error, clear by software 1: Frame error occurs, set by hardware
6	**RXOV**	**EUART0 Receive Over flag, when RXOV bit is read, SSTAT bit must be set 1** 0: No Receive Over, clear by software 1: Receive over occurs, set by hardware
5	**SM2**	**EUART0 Multi-processor communication enable bit (9th bit '1' checker), when SSTAT = 0** 0: In Mode0, baud-rate is 1/12 of system clock In Mode1, disable stop bit validation check, any stop bit will set RI to generate interrupt In Mode2 & 3, any byte will set RI to generate interrupt 1: In Mode0, baud-rate is 1/4 of system clock In Mode1, Enable stop bit validation check, only valid stop bit (1) will set RI to generate interrupt In Mode2 & 3, only address byte (9th bit = 1) will set RI to generate interrupt
5	**TXCOL**	**EUART0 Transmit Collision flag, when TXCOL bit is read, SSTAT bit must be set 1** 0: No Transmit Collision, clear by software 1: Transmit Collision occurs, set by hardware
4	**REN**	**EUART0 Receiver enable bit** 0: Receive Disable 1: Receive Enable
3	**TB8**	**The 9th bit to be transmitted in Mode2 & 3 of EUART0, set or clear by software**
2	**RB8**	**The 9th bit to be received in Mode1, 2 & 3 of EUART0** In Mode0, RB8 is not used In Mode1, if receive interrupt occurs, RB8 is the stop bit that was received In Modes2 & 3 it is the 9th bit that was received
1	**TI**	**Transmit interrupt flag of EUART0** 0: cleared by software 1: Set by hardware
0	**RI**	**Receive interrupt flag of EUART0** 0: cleared by software 1: Set by hardware

Table 8.17 EUART0 Data Buffer Register

99H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SBUF	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
7-0	**SBUF[7:0]**	This SFR accesses two registers; a transmit shift register and a receive latch register A write of SBUF will send the byte to the transmit shift register and then initiate a transmission A read of SBUF returns the contents of the receive latch

Table 8.18 Power Control Register

87H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCON	SMOD	SSTAT	-	-	GF1	GF0	PD	IDL
R/W	R/W	R/W	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	-	-	0	0	0	0

Bit Number	Bit Name	Description
7	**SMOD**	**Baud rate doubler** 0: In mode 2, the baud rate is system clock1/64 1: In mode 2, the baud rate is system clock1/32
6	**SSTAT**	**SCON[7:5] function select bit** 0: SCON[7:5] operates as SM0, SM1, SM2 1: SCON[7:5] operates as FE, RXOV, TXCOL
3-2	**GF[1:0]**	**Software General Flag**
1	**PD**	**Power Down Mode Control bit**
0	**IDL**	**Idle Mode Control bit**

Table 8.19 EUART0 Slave Address & Address Mask Register

9AH-9BH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SADDR (9AH)	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0
SADEN (9BH)	SADEN.7	SADEN.6	SADEN.5	SADEN.4	SADEN.3	SADEN.2	SADEN.1	SADEN.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
7-0	**SADDR[7:0]**	**SFR SADDR defines the EUART's slave address**
7-0	**SADEN[7:0]**	**SFR SADEN is a bit mask to determine which bits of SADDR are checked against a received address** 0: Corresponding bit in SADDR is a "don't care" 1: Corresponding bit in SADDR is checked against a received address

Table 8.20 EUART0 Baud Rate Generator Register

9CH-9DH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SBRTH (9DH)	SBRTEN	SBRT.14	SBRT.13	SBRT.12	SBRT.11	SBRT.10	SBRT.9	SBRT.8
SBRTL (9CH)	SBRT.7	SBRT.6	SBRT.5	SBRT.4	SBRT.3	SBRT.2	SBRT.1	SBRT.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
7	**SBRTEN**	**EUART0 Baud Rate Generator Enable bit** 0: Off (default) 1: On
6-0 **7-0**	**SBRT[14:0]**	**EUART0 Baud Rate Generator Counter High 7-bit & Low 8-bit Register**

Table 8.21 EUART0 Baud Rate Generator Fine-Tune Register

9EH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SFINE	-	-	-	-	SFINE.3	SFINE.2	SFINE.1	SFINE.0
R/W	-	-	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	0	0	0	0

Bit Number	Bit Name	Description
3-0	**SFINE[3:0]**	**EUART0 Baud Rate Generator Fine Tune Data Register**

8.5 Analog Digital Converter (ADC)

8.5.1 Feature

- 10-bit Resolution
- Selectable external or built-in V_{REF}
- 9 Multiplexed Input Channels, and one channel connected to the internal reference voltage (1.00V) to detect battery voltage

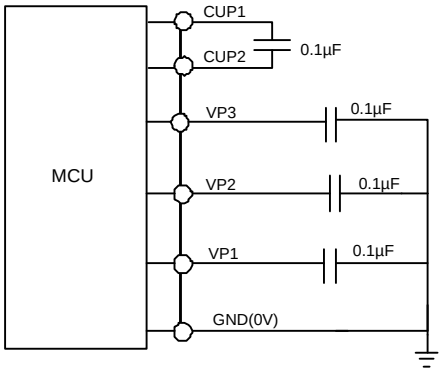
The SH79F3252 include a 10-bit Σ-Δ Analog to Digital Converter (ADC) with build in reference voltage connected to the V_{DD}, users also can select the V_{REF} pin input reference voltage. The 9 ADC channels are shared with 1 ADC module; each channel can be programmed to connect with the analog input individually. Only one channel can be available at one time. There is one channel connected to the internal refence voltage through RGON bit. GO/$\overline{DONE}$ signal is available to start convert, and indicate end of convert. When the conversion is completed, the data in AD convert data register will be updated and ADCIF bit in ADCON register will be set. If ADC Interrupt is enabled, the ADC interrupt will generate.

The ADC integrates a digital compare function to compare the value of analog input with the digital value in the AD converter. If this function is enabled (set EC bit in ADCON register) and ADC module is enabled (set ADON bit in ADCON register). When the corresponding digital value of analog input is larger than the value in compare value register (ADDH/L), the ADC interrupt will occur, otherwise no interrupt will be generated. The digital comparator can work continuously when GO/$\overline{DONE}$ bit is set until software clear, which behaviors different with the AD converter operation mode.

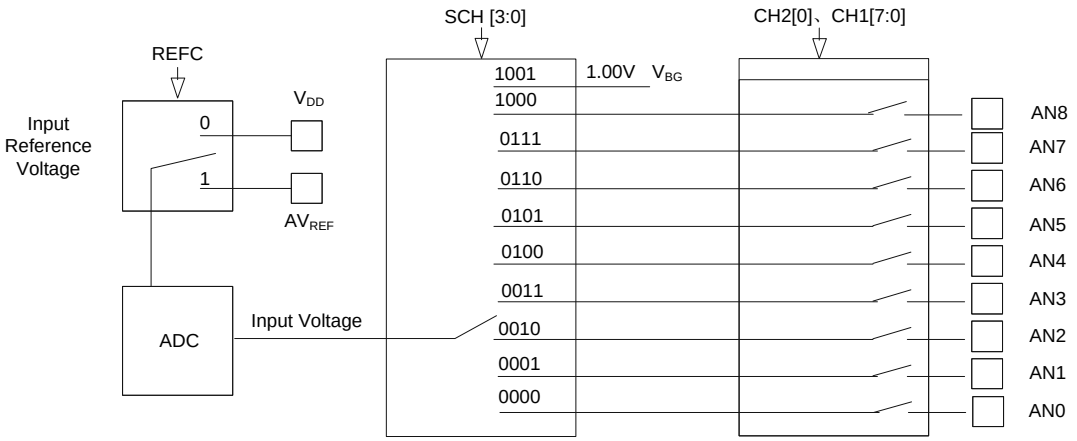
The ADC module including digital compare module can wok in Idle mode which can be waken up by the ADC interrupt. In Power-Down mode and the ADC interrupt will wake up the Idle mode, ADC module is disabled.

The ADC module can work in the 1.8V - 3.6V voltage range. When the V_{DD} voltage is less than 3.1V, in order to ensure ADC conversion performance, the ADC Pump circuit must be opened. When the V_{DD} voltage is larger than or equal to 3.1V, it is not necessary to turn on the ADC Pump circuit. If the ADC Pump circuit is opened, the ADC module can be opened at least 50ms.

When ADCPUMP = 1, the P0.2~P0.6 port is used as the ADC Pump port (VP1 - VP3, CUP1 - CUP2 function); otherwise, P0.2 - P0.6 is used as a IO port. The following is as follows:



8.5.2 ADC Diagram



8.5.3 Register

Table 8.22 ADC Control Register

93H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCON	ADON	ADCIF	EC	REFC	-	-	-	GO/$\overline{\text{DONE}}$
R/W	R/W	R/W	R/W	R/W	-	-	-	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	-	-	-	0

Bit Number	Bit Name	Description
7	**ADON**	**ADC Enable bit** 0: Disable the ADC module 1: Enable the ADC module
6	**ADCIF**	**ADC Interrupt Flag bit** 0: No ADC interrupt, cleared by software. 1: Set by hardware to indicate that the AD Convert has been completed, or analog input is larger than ADDH/ADDL if compare is enabled
5	**EC**	**Compare Function Enable bit** 0: Compare function disabled 1: Compare function enabled
4	**REFC**	**Reference Voltage Select bit** 0: the reference voltage connected to V_{DD} 1: the reference voltage input from V_{REF} pin
0	**GO/$\overline{\text{DONE}}$**	**ADC status flag bit** 0: Automatically cleared by hardware when AD conversion is completed. Clearing this bit during converting time will stop current conversion. If Compare function is enabled, this bit will not be cleared by hardware until software clear. 1: Set to start AD convert or digital compare.

Notes:

(1) When select the reference voltage input from V_{REF} pin (REFC = 1), the P3.1 is shared as V_{REF} input.

*(2) before the ADC conversion, it is best to open the ADON 20us and then set **GO/$\overline{\text{DONE}}$ and convert**, because the ADC module has a stable time after it is opened.*

Table 8.23 ADC Control Register 1

8FH (Bank0)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCON1	VBG	ALR	ADCPUMP	-	SCH3	SCH2	SCH1	SCH0
R/W	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	-	0	0	0	0

Bit Number	Bit Name	Description
7	**VBG**	**Reference source switch bit** 0: Disable 1.00V Reference 1: Enable 1.00V Reference
6	**ALR**	**ADC result left & right aligned selection bit** 0: The 10-bits result stored in result register ADDL/H are stored in left aligned. High 8 bits are stored in ADDxH, Low 2 bits are stored in the high 2 bits of ADDxL. 1: The 10-bits result stored in result register ADD0L/H are stored in right aligned. High 2 bits stored in low 2 bits of ADDxH, low 8 bits stored in ADDxL. ***Note:** This flag only can be changed when GO/$\overline{\text{DONE}}$ = 0. If **GO/$\overline{\text{DONE}}$** = 1 (during ADC conversion), the flag can't be changed.*

(to be continued)

(continue)

5	**ADCPUMP**	**ADC Pump circuit enabled switch:** 0: disable ADC Pump circuits 1: enable ADC Pump circuit ***Note:*** *When the V_{DD} operating voltage is less than 3.1V, it is necessary to enable the ADC Pump circuit.* *When the V_{DD} operating voltage is greater than 3.1V, the ADC Pump circuit does not need to be opened.*
3-0	**SCH[3:0]**	**ADC Channel Select bits** 0000: ADC channel AN0 0001: ADC channel AN1 0010: ADC channel AN2 0011: ADC channel AN3 0100: ADC channel AN4 0101: ADC channel AN5 0110: ADC channel AN6 0111: ADC channel AN7 1000: ADC channel AN8 1001: VBG (1.00V) (Other values are invalid) ***Note:*** *100us ahead of time to open the 1.0V reference source, if the V_{BG} in the sequence.*

Notes:

(1) When the VBG is 1, and the ADC channel is set to VBG, it can be used as the power supply voltage monitoring.

(2) When the ADC Pump circuit is opened, the ADC module should be reopened after at least 50ms.

Table 8.24 ADC Timer Control Register

94H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADT	TADC7	TADC6	TADC5	TADC4	TADC3	TADC2	TADC1	TADC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
7-0	**TADC[7:0]**	**ADC Timer Control Register** ADC clock = f_{SYS}/2/ (256 - TADC[7:0])

Note:

(1) f_{SYS} is system clock, so the system clock division will affect the ADC clock;

(2) set the ADC working clock by the ADT register;

(3) the ADC clock calculation formula is: ADC clock = f_{SYS}/2/ (256-TADC[7:0]);

(4) the ADC conversion frequency is: the ADC clock /26; in order to ensure performance, the ADC conversion frequency is recommended in 1K - 50K sps when configuring.

Table 8.25 ADC Channel Configure Register1

95H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCH1	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
7-0	**CH[7:0]**	**Channel Configuration bits** 0: P4.4,P3.6 - P3.0 are I/O port 1: P4.4,P3.6 - P3.0 are ADC input port

Table 8.26 ADC Channel Configure Register2

C2H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCH2	-	-	-	-	-	-	-	CH8
R/W	-	-	-	-	-	-	-	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	-	-	-	0

Bit Number	Bit Name	Description
0	**CH8**	**Channel Configuration bits** 0: P4.5 are I/O port 1: P4.5 are ADC input port

Table 8.27 ADConverter Data Register (Compare Value Register)

Left alignment mode:

96H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADDxL	A1	A0	-	-	-	-	-	-
R/W	R/W	R/W	-	-	-	-	-	-
Reset Value (POR/WDT/LVR/PIN)	0	0	-	-	-	-	-	-
97H	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
ADDxH	A9	A8	A7	A6	A5	A4	A3	A2
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Right alignment mode:

96H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADDxL	A7	A6	A5	A4	A3	A2	A1	A0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0
97H	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
ADDxH	-	-	-	-	-	-	A9	A8
R/W	-	-	-	-	-	-	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	-	-	-	-	-	-	0	0

Bit Number	Bit Name	Description
7-0, 7-6/ 2-0, 7-0	**A9-A0**	**Left alignment mode (ALR = 0)** After the conversion of a channel, the data updated immediately and stored in ADDL/H High 8 bits are stored in ADDH, the low 2 bits are stored in the high 2 bits in ADDL register. If ADC Compare function is enabled (EC = 1), this is the value to be compared with he analog input **Right alignment mode (ALR = 1)** After the conversion of a channel, the data updated immediately and stored in ADDxL/H(x = 0 - 7) High 2 bits are stored in the low 2 bits in ADDH, the low 8 bits are stored in the in ADDL register. If ADC Compare function is enabled (EC = 1), this is the value to be compared with he analog input

The Approach for AD Conversion:

(1) Choosing whether to trun on the ADC Pump circuit according to the actual working voltage range;
(2) select the right ADC clock;
(3) Select the analog input channels;
(4) If the ADC Pump circuit is opened, it will wait for more than 50ms to make the ADC module;
(5) Set GO/$\overline{\text{DONE}}$ = 1 to start the AD conversion;
(6) Wait until GO/$\overline{\text{DONE}}$ = 0 or ADCIF = 1, if the ADC interrupt is enabled, the ADC interrupt will occur, user need clear ADCIF by software;
(7) Acquire the converted data from ADDH/ADDL;
(8) Repeat step 3-5 if another conversion is required.

The Approach for Digital Compare Function:

(1) Choosing whether to trun on the ADC Pump circuit according to the actual working voltage range
(2) select the right ADC clock
(3) Select the analog input channels
(4) Set ADDH/ADDL to the compare value;
(5) Set EC = 1 to enable compare function;
(6) If the ADC Pump circuit is opened, it will wait for more than 50ms to make the ADC module
(7) Set GO/$\overline{\text{DONE}}$ = 1 to start the compare function;
(8) If the analog input is lager than compare value set in ADDH/ADDL, the ADCIF will be set to 1. if the ADC interrupt is enabled, the ADC interrupt will occur,user need clear ADCIF by software;
(9) The compare function will continue work until the GO/$\overline{\text{DONE}}$ bit is cleared to 0.

8.6 Low Power Detect (LPD)

8.6.1 Feature

- An internal flag indicates low power is detected
- LPD detect voltage is selectable
- LPD the time jitter is 30-60μs of T_{LPD}

Low Power Detect(LPD) function is used to monitor the supply voltage and generate an internal flag if the voltage decrease below the specified value. It is used to inform CPU whether the power is shut off or the battery is used out, so the software may do some protection action before the voltage drop down to the minimal operation voltage.

LPD interrupt can wake the Power-down mode

8.6.2 Register

Table 8.28 Low Power Detection Control Register

B3H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LPDCON	LPDEN	LPDF	LPDMD	LPDIF	LPDS3	LPDS2	LPDS1	LPDS0
R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Mnemonic	Description
7	**LPDEN**	**LPD Enable bit** 0: Disable lower power detection 1: Enable lower power detection
6	**LPDF**	**LPD status Flag bit** 0: no LPD occurred, clear to 0 by the hardware 1: LPD interrupt occurred ,set to one by the hardware
5	**LPDMD**	**LPD mode selection control bit** 0: when the V_{DD} voltage is smaller than the LPD detect voltage setting, the LPDIF flag is set to 1. 1: when the V_{DD} voltage is larger than the LPD detect voltage setting, the LPDIF flag
4	**LPDIF**	**LPD interrupt flag bit** 0: no LPD interrupt occurred, clear to 0 by the software 1: LPD interrupt occurred ,set to one by the hardware
3-0	**LPDS[3:0]**	**LPD Voltage Select Bit** 0000: 1.90V 0001: 2.05V 0010: 2.20V 0011: 2.35V 0100: 2.50V 0101: 2.65V 0110: 2.80V 0111: 2.95V 1000: 3.10V 1001: 3.25V 1010: 3.40V other: invalid

Note: *when the user selects the LPD voltage level, the invalid file can not be selected.*

8.7 Low Voltage Reset (LVR)

8.7.1 Features

- Enabled by the code option and VLVR is 1.9V
- LVR de-bounce timer TLVR is about 30-60μs
- An internal reset flag indicates low voltage reset generates

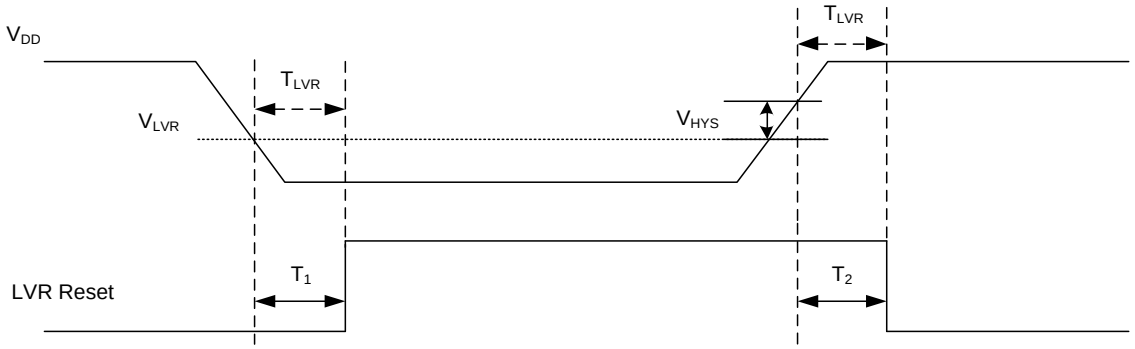
The LVR function is used to monitor the supply voltage and generate an internal reset in the device when the supply voltage below the specified valueV_{LVR}. The LVR de-bounce timer V_{LVR} is about 30μs-60μs.

The LVR circuit has the following functions when the LVR function is enabled: (t means the time of the supply voltage below V_{LVR}):

Generates a system reset when $V_{DD} \leq V_{LVR}$ and $t \geq T_{LVR}$

When $V_{DD} > V_{LVR} + V_{HYS}$, release system reset.

When $V_{DD} > V_{LVR}$ or $V_{DD} < V_{LVR}$ and T1 < TLVR, system reset can not occur.



Here, V_{DD} is the power supply voltage, V_{LVR} is LVR detection voltage, V_{HYS} is the hysteresis voltage of low voltage reset.

The LVR function is enabled by the code option.

It is typically used in AC line or large battery supplier applications, where heavy loads may be switched on and cause the MCU supply-voltage temporarily falls below the minimum specified operating voltage. This feature can protect system from working under bad power supply environment.

8.8 Watchdog Timer (WDT) and Reset State

8.8.1 Features

- Auto detect Program Counter(PC) over range, and generate OVL Reset
- WDT runs even in the Power-Down mode
- Selectable different WDT overflow frequency

OVL Reset

To enhance the anti-noise ability, SH79F3252 built in Program Counter (PC) over range detect circuit, if program counter value is larger than flash romsize, or detect operation code equal to A5H which is not exist in 8051 instruction set, a OVL reset will be generate to reset CPU, and set WDOF bit. So, to make use of this feature, you should fill unused flash rom with A5H.

Watchdog Timer

The watchdog timer is a increase counter, and its clock source is an independent built-in RC oscillator, so it always runs even in the Power-Down mode. The watchdog timer will generate a device reset when it overflows. It can be enabled or disabled permanently by the code option.

The watchdog timer control bits (WDT.2-0) are used to select different overflow frequency. The watchdog timer overflow flag (WDOF) will be automatically set to “1” by hardware when overflow happens. To prevent overflow happen, by reading or writing the WDT register RSTSTAT, the watchdog timer should re-count before the overflow happens.

8.8.2 Registers

Table 8.29 Reset Control Register

B1H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RSTSTAT	WDOF	-	PORF	LVRF	CLRF	WDT.2	WDT.1	WDT.0
R/W	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR)	0	-	1	0	0	0	0	0
Reset Value (WDT)	1	-	u	u	u	0	0	0
Reset Value (LVR)	u	-	u	1	u	0	0	0
Reset Value (PIN)	u	-	u	u	1	0	0	0

Bit Number	Bit Mnemonic	Description
7	**WDOF**	**Watch Dog Timer Overflow or OVL Reset Flag** Set by hardware when WDT overflow or OVL reset happened, cleared by software or Power On Reset 0: Watch Dog not overflows and no OVL reset generated 1: Watch Dog overflow or OVL reset occurred
5	**PORF**	**Power On Reset Flag** Set only by Power On Reset, cleared only by software 0: No Power On Reset 1: Power On Reset occurred
4	**LVRF**	**Low Voltage Reset Flag** Set only by Low Voltage Reset, cleared by software or Power On Reset 0: No Low Voltage Reset occurs 1: Low Voltage Reset occurred
3	**CLRF**	**Pin Reset Flag** Set only by pin reset, cleared by software or Power On Reset 0: No Pin Reset occurs 1: Pin Reset occurred
2-0	**WDT[2:0]**	**WDT Overflow period control bits** 000 - 001: Overflow period minimal value = 1024ms 010: Overflow period minimal value = 256ms 011: Overflow period minimal value = 128ms 100: Overflow period minimal value = 64ms 101: Overflow period minimal value = 16ms 110: Overflow period minimal value = 4ms 111: Overflow period minimal value = 1ms ***Notes:*** *If WDT_opt is enable in application, you must clear WatchDog periodically, and the interval must be less than the value list above.*

8.9 Power Management

8.9.1 Feature

- Two power saving modes: Idle mode and Power-Down mode
- Two ways to exit Idle and Power-Down mode: interrupt and reset

To reduce power consumption, SH79F3252 supplies two power saving modes: Idle mode and Power-Down mode. These two modes are controlled by PCON & SUSLO register.

8.9.2 Idle Mode

In this mode, the clock to CPU is frozen, the program execution is halted, and the CPU will stop at a defined state. But the peripherals continue to be clocked. When entering idle mode, all the CPU status before entering will be preserved. Such as: PSW, PC, SFR & RAM are all retained.

By two consecutive instructions: setting SUSLO register as 0x55, and immediately followed by setting the IDL bit in PCON register, will make SH79F3252 enter Idle mode. If the consecutive instruction sequence requirement is not met, the CPU will clear either SUSLO register or IDL bit in the next machine cycle. And the CPU will not enter Idle mode.

The setting of IDL bit will be the last instruction that CPU executed.

There are two ways to exit Idle mode:

(1) An interrupt generated. CPU clock will be restored, and the hardware will clear IDL bit in CON register and SUSLO register. Then the program will execute the interrupt service routine, and then jumps to the instruction following the instruction that activated Idle mode.

(2) After reset signal (logic low on the RESET pin, WDT RESET, LVR REST) happen, CPU clock will be restored, the hardware will clear IDL bit in CON register and SUSLO register. SH79F3252 will finally be reset. And the program will execute from address 0000H. The RAM will keep unchanged and the SFR value might be changed according to different function module.

8.9.3 Power-Down Mode

The Power-Down mode places the SH79F3252 in a very low power consumption state.

If system clock selects 32.768kHz crystal or the internal 128K/32kHz RC, power-Down mode will stop all the clocks including CPU and peripherals.

If system clock selects internal 8MHz RC, power-Down mode will stop all the clocks including CPU and peripherals (except 128K/32kHz/32.768KHz used to LCD and Timer3).

If WDT is enabled by code option, WDT module will keep on working in Power-Down mode. All the CPU status will be preserved before entering Power-Down mode. Such as: PSW, PC, SFR & RAM.

Two consecutive instructions: first setting SUSLO register as 0x55, then setting the PD bit of PCON register immediately, make SH79F3252 enter Power-Down mode. If the consecutive instruction sequence requirement is not met, the CPU will clear either SUSLO register or PD bit in the next machine cycle. Otherwise CPU will not enter Power-Down mode.

Note: *If IDL bit and PD bit are set simultaneously, the* SH79F3252 *enters Power-Down mode. The CPU will not go in Idle mode when exiting from Power-Down mode, and the hardware will clear both IDL & PD bit after exit form Power-Down mode.*

There are three ways to exit the Power-Down mode:

(1) An effective external Interrupt and LPD interrupt makes SH79F3252 exit Power-Down mode. The high frequence oscillator restarts after interrupt occurs. After warm-up time, the clocks of the CPU and peripheral are restored, and the SUSLO register and PD bit are cleared by hardware. Then the CPU executes the corresponding interrupt service program. After that, program execution resumes with the instruction immediately following the instruction that activated Power-Down mode.

(2) The 32.768kHz crystal, 128K/32kHz RC or T3 port input external clock is used as timer3 clock, Timer3 interrupt makes SH79F3252 exit Power-Down mode. The high frequence oscillator restarts after the interrupt ocurrs, After warm-up time, the clocks of the CPU and peripheral are restored, and the SUSLO register and PD bit are cleared by hardware. Then the CPU executes the corresponding interrupt service program. After that, program execution resumes with the instruction immediately following the instruction that activated Power-Down mode.

(3) Reset signal (logic low on the RESET pin, WDT RESET if enabled, LVR REST if enabled). The low frequence oscillator restarts after reset signal occurs. After warm-up time, the clocks of the CPU and peripheral are restored, and the SUSLO register and PD bit are cleared by hardware. Then the SH79F3252 is reset. And the program executes from 0000H address. The RAM keeps their values and the SFR values might be changed according to different modules.

Note: *In order to entering Idle/Power-Down, it is necessary to add 3 NOPs after setting IDL/PD bit in PCON.*

8.9.4 Register

Table 8.30 Power Control Register

87H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCON	SMOD	SSTAT	-	-	GF1	GF0	PD	IDL
R/W	R/W	R/W	-	-	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	-	-	0	0	0	0

Bit Number	Bit Name	Description
7	**SMOD**	**Baud rate double bit**
6	**SSTAT**	**SCON[7:5] function selection bit**
3-2	**GF[1:0]**	**General purpose flags for software use**
1	**PD**	**Power-Down mode control bit** 0: Cleared by hardware when an interrupt or reset occurs 1: Set by software to activate the Power-Down mode
0	**IDL**	**Idle mode control bit** 0: Cleared by hardware when an interrupt or reset occurs 1: Set by software to activate the Idle mode

Table 8.31 Suspend Mode Control Register

8EH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SUSLO	SUSLO.7	SUSLO.6	SUSLO.5	SUSLO.4	SUSLO.3	SUSLO.2	SUSLO.1	SUSLO.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR/WDT/LVR/PIN)	0	0	0	0	0	0	0	0

Bit Number	Bit Name	Description
7-0	**SUSLO[7:0]**	This register is used to control the CPU enter suspend mode (Idle or Power-Down). Only consecutive instructions like below will make CPU enter suspend mode. Other wise the either SUSLO, IDL or PD bit will be cleared by hardware in the next machine cycle.

Example:

```
IDLE_MODE:
        MOV     SUSLO, #55H
        ORL     PCON, #01H
        NOP
        NOP
        NOP

POWERDOWN_MODE:
        MOV     SUSLO, #55H
        ORL     PCON, #02H
        NOP
        NOP
        NOP
```

8.10 Warm-up Timer

8.10.1 Feature

- Built-in power on warm-up counter to eliminate unstable state of power on
- Built-in oscillator warm-up counter to eliminate unstable state when oscillation startup

SH79F3252 has a built-in power warm-up counter; it is designed to eliminate unstable state after power on or to do some internal initial operation such as read customer option etc.

SH79F3252 has also a built-in oscillator warm-up counter, it is designed to eliminate unstable state when oscillator starts oscillating in the following conditions: Power-on reset, Pin reset, LVR reset, Watchdog Reset and Wake up from Power-down mode.

After power-on, SH79F3252 will start power warm-up procedure first, and then oscillator warm-up procedure.

Power Warm-up Time

Power On Reset/ Pin Reset/ Low Voltage Reset		**WDT Reset (Not in Power-Down Mode)**		**WDT Reset (Wakeup from Power-Down Mode)**		**Wakeup from Power-Down Mode (Only for interrupt)**	
TPWRT**	OSC Warm up*	TPWRT**	OSC Warm up*	TPWRT**	OSC Warm up*	TPWRT**	OSC Warm up*
11ms	YES	≈1ms	NO	≈1ms	YES	≈200us	YES

OSC Warm-up Time

Oscillator Type	**OSC Warm-up Time**
32.768kHz Crystal	2^{13} X Tosc
Internal RC	2^{7} X Tosc

8.11 Code Option

OP_WDT:

0101: Disable WDT function
Other: Enable WDT function (default)

OP_WDTPD:

0: Disable WDT function in Power-Down mode (default)
1: Enable WDT function in Power-Down mode

OP_SCMEN:

0: Enable SCM function (default)
1: Disable SCM function

OP_OSC:

0000: OSC1CLK is Internal 8MHz RC oscillator, OSC2CLK closed
0011: OSC1CLK is internal low fenquency oscillator, OSC2CLK is internal 8MHz RC oscillator (default)
0110: OSC1CLK is internal 128KHz RC oscillator, OSC2CLK is 2M - 16M crystal/ceramic oscillator
1010: OSC1CLK is 32.768kHz crystal, OSC2CLK is internal 8MHz RC oscillator
1111: OSC1CLK is external clock from XTAL1, OSC2CLK closed
Other: OSC1CLK is internal low fenquency oscillator, OSC2CLK is Internal 8MHz RC oscillator

OP_LRCSEL:

0: internal low fenquency oscillator is 32KHz (default)
1: internal low fenquency oscillator is 128KHz

OP_AHRV:

0: AHUM reset value = 0 of the 32.768kHz crystal Humidity resistance function control bit
1: AHUM reset value = 1 of the 32.768kHz crystal Humidity resistance function control bit (default)

OP_PWM_REM_IOSEL:

0: P1.2 as PWM1/REM port(default)
1: P0.0 asPWM1/REM port

OP_REM_CURRENT: (REM drive current selection)

00:125mA
01: 250mA
10: 350Ma (default)
11: 450mA

OP_LVREN:

0: Disable LVR function (default)
1: Enable LVR function

OP_SCM:

0: SCM is off during warm-up time
1: SCM is on during warm-up time(default)

OP_RST:

0: P4.7 as reset pin (default)
1: P4.7 as I/O

OP_LCDSEL:

0: Select resistor LCD driver
1: Select capacitor LCD driver(default)

OP_P0:

0: Port0 (0 - 7) sink ability normal mode (default)
1: Port0 (0 - 7) sink ability large mode

OP_P1:

0: Port1 (0 - 7) sink ability normal mode (default)
1: Port1 (0 - 7) sink ability large mode

OP_P2:

0: Port2 (0 - 7) sink ability normal mode (default)
1: Port2 (0 - 7) sink ability large mode

OP_P3:

0: Port3 (0 - 7) sink ability normal mode (default)
1: Port3 (0 - 7) sink ability large mode

OP_P4:

0: Port4 (0 - 7) sink ability normal mode (default)
1: Port4 (0 - 7) sink ability large mode

OP_P5:

0: Port5 (0 - 4) sink ability normal mode (default)
1: Port5 (0 - 4) sink ability large mode

OP_EEPROMSIZE:

0000: 8 X 512Bytes (default)
0001: 7 X 512Bytes
0010: 6 X 512Bytes
0011: 5 X 512Bytes
0100: 4 X 512Bytes
0101: 3 X 512Bytes
0110: 2 X 512Bytes
0111: 1 X 512Bytes
1000: 0Bytes
other: 0Bytes

9. Instruction Set

ARITHMETIC OPERATIONS				
Opcode	**Description**	**Code**	**Byte**	**Cycle**
ADD A, Rn	Add register to accumulator	0x28-0x2F	1	1
ADD A, direct	Add direct byte to accumulator	0x25	2	2
ADD A, @Ri	Add indirect RAM to accumulator	0x26-0x27	1	2
ADD A, #data	Add immediate data to accumulator	0x24	2	2
ADDC A, Rn	Add register to accumulator with carry flag	0x38-0x3F	1	1
ADDC A, direct	Add direct byte to A with carry flag	0x35	2	2
ADDC A, @Ri	Add indirect RAM to A with carry flag	0x36-0x37	1	2
ADDC A, #data	Add immediate data to A with carry flag	0x34	2	2
SUBB A, Rn	Subtract register from A with borrow	0x98-0x9F	1	1
SUBB A, direct	Subtract direct byte from A with borrow	0x95	2	2
SUBB A, @Ri	Subtract indirect RAM from A with borrow	0x96-0x97	1	2
SUBB A, #data	Subtract immediate data from A with borrow	0x94	2	2
INC A	Increment accumulator	0x04	1	1
INC Rn	Increment register	0x08-0x0F	1	2
INC direct	Increment direct byte	0x05	2	3
INC @Ri	Increment indirect RAM	0x06-0x07	1	3
DEC A	Decrement accumulator	0x14	1	1
DEC Rn	Decrement register	0x18-0x1F	1	2
DEC direct	Decrement direct byte	0x15	2	3
DEC @Ri	Decrement indirect RAM	0x16-0x17	1	3
INC DPTR	Increment data pointer	0xA3	1	4
MUL AB 8 X 8 16 X 8	Multiply A and B	0xA4	1	11 20
DIV AB 8 / 8 16 / 8	Divide A by B	0x84	1	11 20
DA A	Decimal adjust accumulator	0xD4	1	1

LOGIC OPERATIONS				
Opcode	**Description**	**Code**	**Byte**	**Cycle**
ANL A, Rn	AND register to accumulator	0x58-0x5F	1	1
ANL A, direct	AND direct byte to accumulator	0x55	2	2
ANL A, @Ri	AND indirect RAM to accumulator	0x56-0x57	1	2
ANL A, #data	AND immediate data to accumulator	0x54	2	2
ANL direct, A	AND accumulator to direct byte	0x52	2	3
ANL direct, #data	AND immediate data to direct byte	0x53	3	3
ORL A, Rn	OR register to accumulator	0x48-0x4F	1	1
ORL A, direct	OR direct byte to accumulator	0x45	2	2
ORL A, @Ri	OR indirect RAM to accumulator	0x46-0x47	1	2
ORL A, #data	OR immediate data to accumulator	0x44	2	2
ORL direct, A	OR accumulator to direct byte	0x42	2	3
ORL direct, #data	OR immediate data to direct byte	0x43	3	3
XRL A, Rn	Exclusive OR register to accumulator	0x68-0x6F	1	1
XRL A, direct	Exclusive OR direct byte to accumulator	0x65	2	2
XRL A, @Ri	Exclusive OR indirect RAM to accumulator	0x66-0x67	1	2
XRL A, #data	Exclusive OR immediate data to accumulator	0x64	2	2
XRL direct, A	Exclusive OR accumulator to direct byte	0x62	2	3
XRL direct, #data	Exclusive OR immediate data to direct byte	0x63	3	3
CLR A	Clear accumulator	0xE4	1	1
CPL A	Complement accumulator	0xF4	1	1
RL A	Rotate accumulator left	0x23	1	1
RLC A	Rotate accumulator left through carry	0x33	1	1
RR A	Rotate accumulator right	0x03	1	1
RRC A	Rotate accumulator right through carry	0x13	1	1
SWAP A	Swap nibbles within the accumulator	0xC4	1	4

DATA TRANSFERS				
Opcode	**Description**	**Code**	**Byte**	**Cycle**
MOV A, Rn	Move register to accumulator	0xE8-0xEF	1	1
MOV A, direct	Move direct byte to accumulator	0xE5	2	2
MOV A, @Ri	Move indirect RAM to accumulator	0xE6-0xE7	1	2
MOV A, #data	Move immediate data to accumulator	0x74	2	2
MOV Rn, A	Move accumulator to register	0xF8-0xFF	1	2
MOV Rn, direct	Move direct byte to register	0xA8-0xAF	2	3
MOV Rn, #data	Move immediate data to register	0x78-0x7F	2	2
MOV direct, A	Move accumulator to direct byte	0xF5	2	2
MOV direct, Rn	Move register to direct byte	0x88-0x8F	2	2
MOV direct1, direct2	Move direct byte to direct byte	0x85	3	3
MOV direct, @Ri	Move indirect RAM to direct byte	0x86-0x87	2	3
MOV direct, #data	Move immediate data to direct byte	0x75	3	3
MOV @Ri, A	Move accumulator to indirect RAM	0xF6-0xF7	1	2
MOV @Ri, direct	Move direct byte to indirect RAM	0xA6-0xA7	2	3
MOV @Ri, #data	Move immediate data to indirect RAM	0x76-0x77	2	2
MOV DPTR, #data16	Load data pointer with a 16-bit constant	0x90	3	3
MOVC A, @A+DPTR	Move code byte relative to DPTR to A	0x93	1	7
MOVC A, @A+PC	Move code byte relative to PC to A	0x83	1	8
MOVX A, @Ri	Move external RAM (8-bit address) to A	0xE2-0xE3	1	5
MOVX A, @DPTR	Move external RAM (16-bit address) to A	0xE0	1	6
MOVX @Ri, A	Move A to external RAM (8-bit address)	0xF2-F3	1	4
MOVX @DPTR, A	Move A to external RAM (16-bit address)	0xF0	1	5
PUSH direct	Push direct byte onto stack	0xC0	2	5
POP direct	Pop direct byte from stack	0xD0	2	4
XCH A, Rn	Exchange register with accumulator	0xC8-0xCF	1	3
XCH A, direct	Exchange direct byte with accumulator	0xC5	2	4
XCH A, @Ri	Exchange indirect RAM with accumulator	0xC6-0xC7	1	4
XCHD A, @Ri	Exchange low-order nibble indirect RAM with A	0xD6-0xD7	1	4

PROGRAM BRANCHES					
Opcode		**Description**	**Code**	**Byte**	**Cycle**
ACALL addr11		Absolute subroutine call	0x11-0xF1	2	7
LCALL addr16		Long subroutine call	0x12	3	7
RET		Return from subroutine	0x22	1	8
RETI		Return from interrupt	0x32	1	8
AJMP addr11		Absolute jump	0x01-0xE1	2	4
LJMP addr16		Long jump	0x02	3	5
SJMP rel		Short jump (relative address)	0x80	2	4
JMP @A+DPTR		Jump indirect relative to the DPTR	0x73	1	6
JZ rel	(not taken) (taken)	Jump if accumulator is zero	0x60	2	3 5
JNZ rel	(not taken) (taken)	Jump if accumulator is not zero	0x70	2	3 5
JC rel	(not taken) (taken)	Jump if carry flag is set	0x40	2	2 4
JNC rel	(not taken) (taken)	Jump if carry flag is not set	0x50	2	2 4
JB bit, rel	(not taken) (taken)	Jump if direct bit is set	0x20	3	4 6
JNB bit, rel	(not taken) (taken)	Jump if direct bit is not set	0x30	3	4 6
JBC bit, rel	(not taken) (taken)	Jump if direct bit is set and clear bit	0x10	3	4 6
CJNE A, direct, rel	(not taken) (taken)	Compare direct byte to A and jump if not equal	0xB5	3	4 6
CJNE A, #data, rel	(not taken) (taken)	Compare immediate to A and jump if not equal	0xB4	3	4 6
CJNE Rn, #data, rel	(not taken) (taken)	Compare immediate to reg. and jump if not equal	0xB8-0xBF	3	4 6
CJNE @Ri, #data, rel	(not taken) (taken)	Compare immediate to Ri and jump if not equal	0xB6-0xB7	3	4 6
DJNZ Rn, rel	(not taken) (taken)	Decrement register and jump if not zero	0xD8-0xDF	2	3 5
DJNZ direct, rel	(not taken) (taken)	Decrement direct byte and jump if not zero	0xD5	3	4 6
NOP		No operation	0	1	1

BOOLEAN MANIPULATION				
Opcode	**Description**	**Code**	**Byte**	**Cycle**
CLR C	Clear carry flag	0xC3	1	1
CLR bit	Clear direct bit	0xC2	2	3
SETB C	Set carry flag	0xD3	1	1
SETB bit	Set direct bit	0xD2	2	3
CPL C	Complement carry flag	0xB3	1	1
CPL bit	Complement direct bit	0xB2	2	3
ANL C, bit	AND direct bit to carry flag	0x82	2	2
ANL C, /bit	AND complement of direct bit to carry	0xB0	2	2
ORL C, bit	OR direct bit to carry flag	0x72	2	2
ORL C, /bit	OR complement of direct bit to carry	0xA0	2	2
MOV C, bit	Move direct bit to carry flag	0xA2	2	2
MOV bit, C	Move carry flag to direct bit	0x92	2	3

10. Electrical Characteristics

Absolute Maximum Ratings*

DC Supply Voltage. . . . . .-0.3V to +3.6V

Input/Output Voltage.. . . . . .GND-0.3V to V_{DD}+0.3V

Operating Ambient Temperature. . . . . .-10℃ to +70℃

Storage Temperature. . . ..-55℃ to +125℃

Flash memory program/erase operation. . . . . 0℃ to +70℃

***Comments**

Stresses exceed those listed under "**Absolute Maximum Ratings**" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 1.8V - 3.6V, GND = 0V, T_A = +25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.*	Max.	Unit	Condition
Operating Voltage	V_{DD}	1.8	3.0	3.6	V	30kHz ≤ f_{OSC} ≤ 8MHz
Operating Current	I_{OP1}	-	1.2	1.5	mA	f_{OSC} = RC 4MHz, V_{DD} = 3.0V All output pins unload (including all digital input pins unfloating) CPU on (execute NOP instruction), WDT on, all other function block off
Stand by Current (IDLE)	I_{SB1}	-	11	13	μA	f_{OSC} = RC 32kHz, V_{DD} = 3.0V, the high frequency oscillator closed, All output pins unload (including all digital input pins unfloating) CPU off (idle), The WDT turn off, SCM off, LVR off, LCD turn on (V_{LCD} = V_{DD}, LCD bias resistor sum is 1.5M, not including LCD panel), all other function block off
	I_{SB2}	-	10	12	μA	f_{OSC} = RC 32kHz, V_{DD} = 3.0V, the high frequency oscillator closed, All output pins unload (including all digital input pins unfloating); CPU off (idle), The WDT turn off, SCM off, LVR off, LCD bias capacitance mode, LCD turn on (not including LCD panel), all other function block off
Stand by Current (power-down)	I_{SB3}	-	-	2.5	μA	f_{OSC} closed, V_{DD} = 3.0V All output pins unload (including all digital input pins unfloating); CPU off (power-down); LCD off, WDT off, SCM off, LVR off, all other function block off
	I_{SB4}	-	2.5	3.5	μA	f_{OSC} = RC 32kHz, the high frequency oscillator closed, V_{DD} = 3.0V All output pins unload (including all digital input pins unfloating); CPU off (power-down); LCD off, WDT off, SCM off, LVR off, all other function block off
	I_{SB5}	-	3.5	5.0	μA	f_{OSC} = RC 32kHz, the high frequency oscillator closed, V_{DD} = 3.0V All output pins unload (including all digital input pins unfloating); CPU off (power-down); WDT off, SCM off, LVR off, LCD bias capacitance mode, LCD turn on (not including LCD panel), all other function block off
	I_{SB6}	-	2.8	3.8	μA	f_{OSC} = 32.768kHz (AHUM = 0 of the CLKCON regisrer), the high frequency oscillator closed, V_{DD} = 3.0V All output pins unload (including all digital input pins unfloating); CPU off (power-down); LCD off, WDT off, SCM off, LVR off, all other function block off
	I_{SB7}	-	3.8	5.3	μA	f_{OSC} = 32.768kHz (AHUM = 0 of the CLKCON regisrer), the high frequency oscillator closed, V_{DD} = 3.0V All output pins unload (including all digital input pins unfloating); CPU off (power-down); WDT off, SCM off, LVR off, LCD bias capacitance mode, LCD turn on (not including LCD panel), all other function block off

(to be continued)

(continue)

Parameter	Symbol	Min.	Typ.*	Max.	Unit	Condition
LCD Current 1	I_{LCD1}	-	0.7	1.2	μA	V_{DD} = 3.0V, buit-in capacitance voltage regulator (not include LCD panel)
LCD Current 2	I_{LCD2}	-	2	3	μA	V_{DD} = 3.0V, bias resistance mode, bias resistance sum 1.5M, LCD on (not include LCD panel), V_{LCD} = V_{DD}
LCD Current 3	I_{LCD3}	-	0.4	0.7	μA	V_{DD} = 3.0V, bias capacitance mode (not include LCD panel)
WDT Current	I_{WDT}	-	-	0.4	μA	V_{DD} = 3.0V, WDT turn on
LPD Current	I_{LPD}	-	-	1.0	μA	V_{DD} = 1.8 - 3.6V, only LPD turn on
Input Low Voltage 1	V_{IL1}	GND	-	0.3 X V_{DD}	V	I/O port
Input High Voltage 1	V_{IH1}	0.7 X V_{DD}	-	V_{DD}	V	I/O port
Input Low Voltage 2	V_{IL2}	GND	-	0.2 X V_{DD}	V	$\overline{\text{RESET}}$, T2 - 3, INT0, INT2 - 4, T2EX, RXD0 V_{DD} = 1.8 - 3.6V, P17/P40, TTL turn off
Input High Voltage 2	V_{IH2}	0.8 X V_{DD}	-	V_{DD}	V	$\overline{\text{RESET}}$, T2 - 3, INT0, INT2 - 4, T2EX, RXD0 V_{DD} = 1.8 - 3.6V, P17/P40, TTL turn off
Input Low Voltage 3	V_{IL3}	GND	-	0.15 XV_{DD}	V	V_{DD} = 1.8 - 3.6V, P17/P40, TTL turn on
Input High Voltage 3	V_{IH3}	0.25 X V_{DD}+0.8	-	V_{DD}	V	V_{DD} = 1.8 - 3.6V, P17/P40, TTL turn on
Input Leakage Current	I_{IL}	-1	-	1	μA	Input port, V_{IN} = V_{DD} or GND
Output Leakage Current	I_{OL}	-1	-	1	μA	Open-drain output, (OP_PWM_REM_IOSEL select P0.0 as PWM/REM port by Option; REM turn on); V_{DD} = 3.0V, V_{OUT} = V_{DD} or GND
Rest pin Pull-up Resistor	R_{RPH}	-	50	-	kΩ	V_{DD} = 3.0V, V_{IN} = GND
Pull-up Resistor	R_{PH}	-	50	-	kΩ	V_{DD} = 3.0V, V_{IN} = GND
Output High Voltage 1	V_{OH1}	V_{DD} - 0.7	-	-	V	I/O port, I_{OH} = -5mA, V_{DD} = 3.0V
Output Low Voltage 1	V_{OL1}	-	-	GND +0.6	V	I/O port, I_{OL} = 10mA, V_{DD} = 3.0V (Select sink current normal)
Output Low Voltage 1	V_{OL2}	-	-	GND +0.6	V	I/Oport, I_{OL} = 20mA, V_{DD} = 3.0V (Select large sink current normal)
REM Sink Current	I_{REML}	-	450	-	mA	REM (OP_REM_IOSEL = 1, P0.0), V_{DD} = 3.0V, V_{OL} = GND + 1.2V (Select REM drive current is 450mA)
VP1 Voltage	VP1	0.98	1.0	1.02	V	Select capacitor LCD driver, SEG1 - 31, COM1 - 5, V_{DD} = 1.8V - 3.6V
VP3 Voltage	VP3	2.92	3.0	3.06	V	Select capacitor LCD driver lcdSEG1 - 31, COM1 - 5, V_{DD} = 1.8V - 3.6V
LCD Resistor	R_{ON}	-	5	-	kΩ	SEG1 - 31, COM1 - 5, V_{DD} = 1.8V - 3.6V

Note:

(1) "" Data in "Typ." Column is at 3.0V, 25°C, unless otherwise specified.*

(2) Maximum value of the supply current to V_{DD} is 100mA.

(3) Maximum value of the output current from GND is 600mA.

A/D Converter Electrical Characteristics
(1LSB = V_{DD}/1024) (V_{DD} = 1.8 - 3.6V, GND = 0V, T_A = +25°C, Unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply Voltage	V_{AD}	1.8	3.0	3.6	V	
A/D Referance Voltage	V_{REF}	1.8	-	V_{DD}	V	
Resolution	N_R	-	10	-	bit	GND ≤ V_{AIN} ≤ V_{REF}
A/D Input Voltage	V_{AIN}	GND	-	V_{REF}	V	
A/D Input Resistor	R_{AIN}	2	-	-	MΩ	V_{IN} = 3.0V
ADC Internal reference source	V_{BG}	0.97	1.00	1.03	V	V_{DD} = 1.8V - 3.6V
Build time of ADC internal reference source	T_{VBG}	-	-	10	μs	V_{DD} = 2.7V - 3.6V, T_A = 25°C, VBG Build (0.1%)
		-	-	50		V_{DD} = 1.8V - 2.7V, T_A = 25°C, VBG Build (0.1%)
Channel switching settling time of ADC internal reference source	T_{CBG}	-	-	3	μs	V_{DD} = 2.7V - 3.6V, VBG Build (0.1%)
		-	-	10		V_{DD} = 1.8V - 2.7V, VBG Build (0.1%)
Recommended impedance of analog voltage source	Z_{AIN}	-	-	0.75	kΩ	V_{DD} = 1.8V - 3.6V, switching channel sampling precision is 1LSB
A/D conversion current	I_{AD}	-	0.5	1	mA	ADC model working, V_{DD} = 3.0V
Differential linearity error	D_{LE}	-	-	±1	LSB	V_{DD} = 3.0V, V_{REF} = V_{DD}, 50Ksps
Integral linearity error	I_{LE}	-	-	±2	LSB	V_{DD} = 3.0V, V_{REF} = V_{DD}, 50Ksps
Full scale error	E_F	-	-	±2	LSB	V_{DD} = 3.0V, V_{REF} = V_{DD}, 50Ksps
Offset error	E_Z	-	-	±3	LSB	V_{DD} = 3.0V, V_{REF} = V_{DD}, 50Ksps
Total Absolute error	E_{AD}	-	-	±3	LSB	V_{DD} = 3.0V, V_{REF} = V_{DD}, 50Ksps
Total Conversion time	T_{CON}	20	-	1000	μs	10bit, V_{DD} = 3.0V

AC Electrical Characteristics (V_{DD} = 1.8V - 3.6V, GND = 0V, T_A = +25°C, f_{OSC} = 8MHz, Unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Oscillator start time	T_{OSC}	-	-	1.5	s	f_{OSC} = 32.768kHz
RESET pulse width	t_{RESET}	10	-	-	μs	
WDT RC Frequency	f_{WDT}	0.7	-	2	kHz	V_{DD} = 3.0V
128K RC Frequency	f_{128}	108.8	128	147.2	kHz	V_{DD} = 1.8V - 3.6V, T_A = -10°C ~ +70°C
	f_{128K}	125.44	128	130.56	kHz	V_{DD} = 1.8V - 3.6V, T_A = +25°C
Built-in 8MHZ RC Frequency Stability	F_{RC1}	7.92	8.00	8.08	MHz	Built-in RC oscillator, V_{DD} = 1.8V - 3.6V, T_A = -10°C ~ +70°C
	F_{RC2}	7.96	8.00	8.04	MHz	Built-in RC oscillator, V_{DD} = 1.8V - 3.6V, T_A = +25°C

Low Voltage Reset Electrical Characteristics (V_{DD} = 1.8V - 3.6V, GND = 0V, T_A = +25°C, Unless otherwise specified)

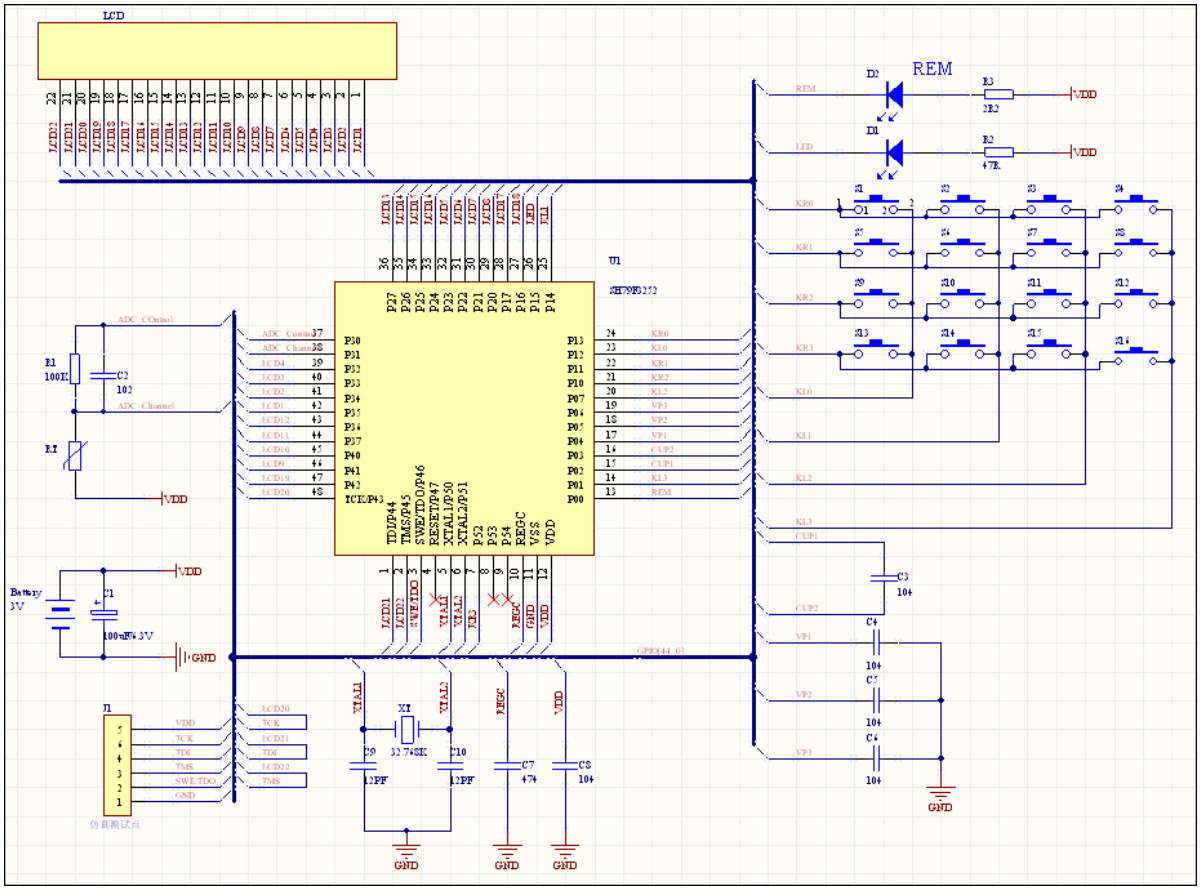
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
LVR Voltage	V_{LVR}	1.8	1.9	2.0	V	LVR enable,V_{DD} = 1.8V - 3.6V
LVR Voltage detection hysteresis window	V_{SMTLV}	-	50	-	mV	
LVR low reset pulse width	T_{LVR}	-	60	-	μs	

Power-on Reset Electrical Characteristics (V_{DD} = 1.8V - 3.6V, GND = 0V, T_A = 25°C, Unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Power supply voltage rise slope	S_{VDD} (1)	0.005	-	1000	V/ms	LVR enable, V_{DD} = 1.8 V - 3.6V

Note: *The project is only guaranteed in design, mass production dose not do the full slope range test.*

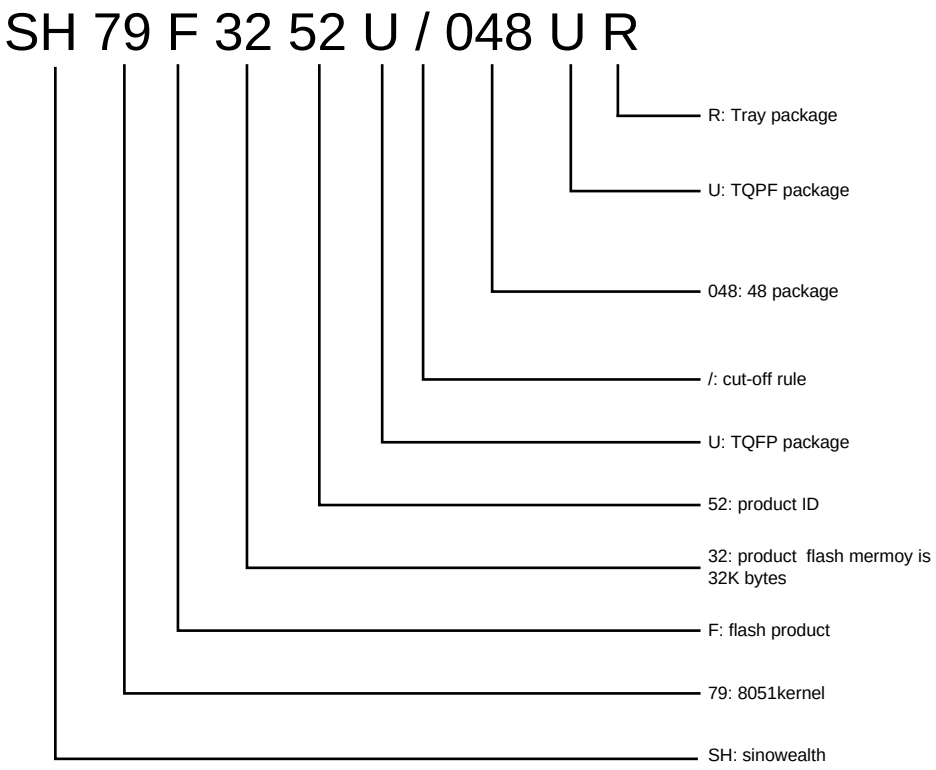
11. Application



12. Ordering Information

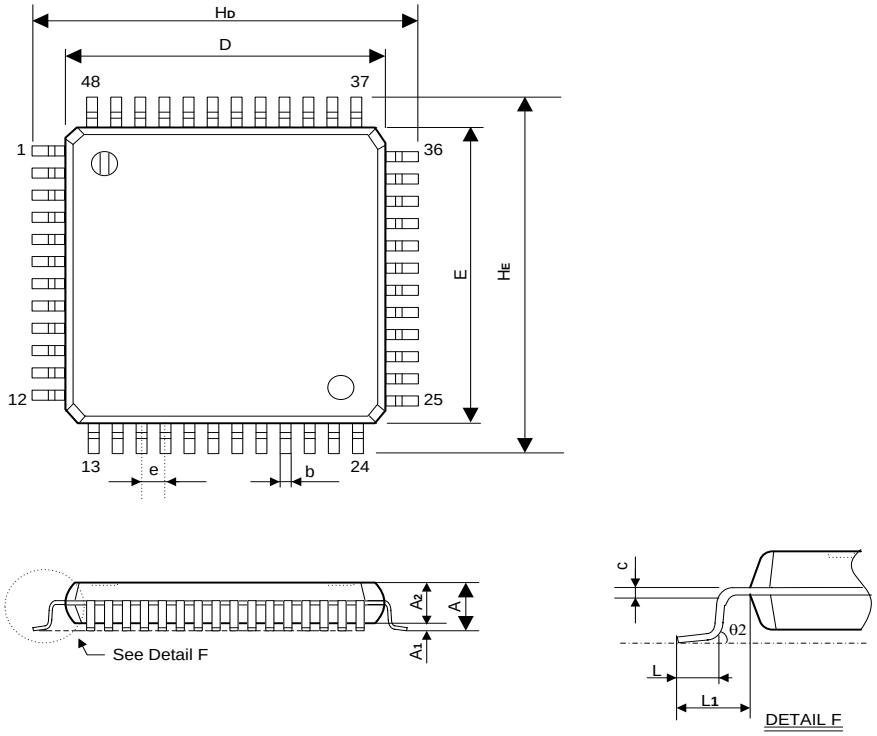
Part No.	Package
SH79F3252U/048UR	TQFP48

13. Product Naming Rules



14. Package Information

TQFP 48L Outline Dimensions unit:inches/mm



Symbol	Dimensions in inches		Dimensions in mm	
	MIN	MAX	MIN	MAX
A	---	0.047	---	1.2
A1	0.002	0.006	0.05	0.15
A2	0.035	0.041	0.9	1.05
D	0.270	0.281	6.85	7.15
E	0.270	0.281	6.85	7.15
H_D	0.346	0.362	8.8	9.2
H_E	0.346	0.362	8.8	9.2
b	0.005	0.011	0.15	0.27
e	0.020 TYP		0.500 TYP	
c	0.004	0.008	0.090	0.200
L	0.018	0.030	0.45	0.75
L1	0.033	0.045	0.85	1.15
θ2	0°	10°	0°	10°

Notice:

(1) Both package length and width do not include mold flash.

(2) Tolerance is ±0.1mm if not specified.

(3) Coplanarity: 0.1mm max.

(4) Controlling dimension: mm.

15. Product SPEC. Change Notice

Version	Content	Date
2.0	Add description of power-on reset electrical characteristics	Aug. 2020
1.0	Original	May. 2019

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