LM8261 Single RRIO High Output Current & Unlimited Cap Load Op Amp

1 Features

- (V_S = 5 V, T_A = 25°C, Typical Values Unless Specified)
- GBWP 21 MHz
- Wide Supply Voltage Range 2.5 V to 30 V
- Slew Rate 12 V/µs
- Supply Current 0.97 mA
- Cap Load Limit Unlimited
- Output Short Circuit Current 53 mA/ −75 mA
- ±5% Settling Time 400 ns (500 pF, 100 mV_{PP} Step)
- Input Common Mode Voltage 0.3 V Beyond Rails
- Input Voltage Noise 15nV/$\sqrt{Hz}$
- Input Current Noise 1pA/$\sqrt{Hz}$
- THD+N < 0.05%

2 Applications

- TFT-LCD Flat Panel V_{COM} Driver
- A/D Converter Buffer
- High Side/low Side Sensing
- Headphone Amplifier

3 Description

The LM8261 is a Rail-to-Rail input and output Op Amp which can operate with a wide supply voltage range. This device has high output current drive, greater than Rail-to-Rail input common mode voltage range, unlimited capacitive load drive capability, and provides tested and guaranteed high speed and slew rate while requiring only 0.97 mA supply current. It is specifically designed to handle the requirements of flat panel TFT panel V_{COM} driver applications as well as being suitable for other low power, and medium speed applications which require ease of use and enhanced performance over existing devices.

Greater than Rail-to-Rail input common mode voltage range with 50 dB of Common Mode Rejection allows high side and low side sensing, among many applications, without concern over exceeding the range and with no compromise in accuracy. Exceptionally wide operating supply voltage range of 2.5 V to 30 V alleviates any concerns over functionality under extreme conditions and offers flexibility for use in multitude of applications. In addition, most device parameters are insensitive to power supply variations; this design enhancement is yet another step in simplifying its usage. The output stage has low distortion (0.05% THD+N) and can supply a respectable amount of current (15 mA) with minimal headroom from either rail (300 mV).

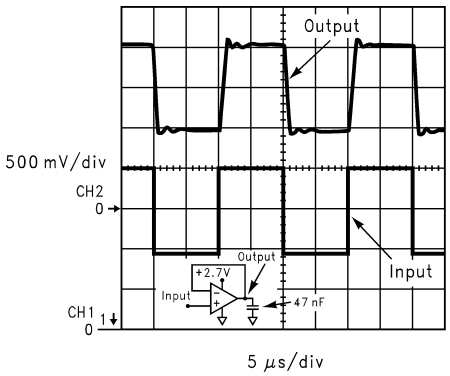
The LM8261 is offered in the space-saving SOT-23-5 package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM8261	SOT-23 (5)	2.9 mm × 1.6 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Output Response with Heavy Capacitive Load



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4 Revision History

Changes from Revision I (March 2013) to Revision J **Page**

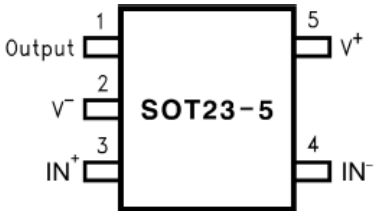
- Added, updated, or revised the following sections: *Pin Configuration and Functions*, *Specifications*, *Detailed Description* , *Application and Implementation*, *Power Supply Recommendations* , *Layout* , *Device and Documentation Support* , and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed from -1.0 V to -0.8 V in *Specifications* ... 4

Changes from Revision H (March 2013) to Revision I **Page**

- Changed layout of National Data Sheet to TI format ... 1

5 Pin Configuration and Functions

5-Pin SOT-23
Package DBV
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NUMBER	NAME		
1	Output	O	Output
2	V-	I	Negative Supply
3	IN+	I	Non-inverting input
4	IN-	I	Inverting Input
5	V+	I	Positive Supply

6 Specifications

6.1 Absolute Maximum Ratings[1]

		MIN	MAX	UNIT
V_{IN} Differential			±10	V
Output Short Circuit Duration		See[2][3]		
Supply Voltage (V^+ - V^-)			32	V
Voltage at Input/Output pins			V^+ +0.8 V, V^- −0.8 V	V
Storage Temperature Range		−65	+150	°C
Junction Temperature[4]			150	°C
Soldering Information:	Infrared or Convection (20 sec.)		235	°C
	Wave Soldering (10 sec.)		260	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Rating indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see *Electrical Characteristics 2.7 V*.
(2) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(3) Allowable Output Short Circuit duration is infinite for $V_S \leq 6$ V at room temperature and below. For $V_S > 6$ V, allowable short circuit duration is 1.5 ms.
(4) The maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1][2]	±2000	V
		Machine model (MM)[3]	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 2000-V HBM is possible with the necessary precautions. Pins listed as ±200 V may actually have higher performance.
(2) Human Body Model is 1.5 kΩ in series with 100 pF.
(3) Machine Model, 0 Ω is series with 200 pF.

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Supply Voltage (V^+ - V^-)	2.5	30	V
Temperature Range[1]	−40	+85	°C

(1) The maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board.

6.4 Thermal Information

THERMAL METRIC[1][2]		DBV (5 PINS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	325	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ R_{\theta JA}$. All numbers apply for packages soldered directly onto a PC board.

6.5 Electrical Characteristics 2.7 V

Unless otherwise specified, all limits guaranteed for T_A = 25°C, V^+ = 2.7 V, V^- = 0 V, V_{CM} = 0.5 V, V_O = V^+/2, and R_L > 1 MΩ to V^-.(1)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX(3)	UNIT
V_{OS}	Input Offset Voltage	V_{CM} = 0.5 V & V_{CM} = 2.2 V			+/−0.7	+/−5	mV
			−65°C ≤ T_J ≤ +150°C			+/−7	
TC V_{OS}	Input Offset Average Drift	V_{CM} = 0.5 V & V_{CM} = 2.2 V(4)			+/−2		µV/C
I_B	Input Bias Current	V_{CM} = 0.5 V(5)			−1.20	−2.00	µA
			−65°C ≤ T_J ≤ +150°C			−2.70	
		V_{CM} = 2.2 V(5)			+0.49	+1.00	
			−65°C ≤ T_J ≤ +150°C			+1.60	
I_{OS}	Input Offset Current	V_{CM} = 0.5 V & V_{CM} = 2.2 V			20	250	nA
			−65°C ≤ T_J ≤ +150°C			400	
CMRR	Common Mode Rejection Ratio	V_{CM} stepped from 0 V to 1.0 V			100	76	dB
			−65°C ≤ T_J ≤ +150°C	60			
		V_{CM} stepped from 1.7 V to 2.7 V			100		
		V_{CM} stepped from 0 V to 2.7 V			70	58	
			−65°C ≤ T_J ≤ +150°C	50			
+PSRR	Positive Power Supply Rejection Ratio	V^+ = 2.7 V to 5 V			104	78	dB
			−65°C ≤ T_J ≤ +150°C	74			
CMVR	Input Common-Mode Voltage Range	CMRR > 50 dB			−0.3	−0.1	V
			−65°C ≤ T_J ≤ +150°C			0.0	
					3.0	2.8	V
			−65°C ≤ T_J ≤ +150°C	2.7			
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5 to 2.2 V, R_L = 10K to V^-			78	70	dB
			−65°C ≤ T_J ≤ +150°C	67			
		V_O = 0.5 to 2.2 V, R_L = 2K to V^-			73	67	dB
			−65°C ≤ T_J ≤ +150°C	63			
V_O	Output Swing High	R_L = 10K to V^-			2.59	2.49	V
			−65°C ≤ T_J ≤ +150°C	2.46			
		R_L = 2K to V^-			2.53	2.45	
			−65°C ≤ T_J ≤ +150°C	2.41			
	Output Swing Low	R_L = 10K to V^-			90	100	mV
			−65°C ≤ T_J ≤ +150°C			120	
I_{SC}	Output Short Circuit Current	Sourcing to V^- V_{ID} = 200 mV(6)(7)			48	30	mA
			−65°C ≤ T_J ≤ +150°C	20			
		Sinking to V^+ V_{ID} = −200 mV(6)(7)			65	50	mA
			−65°C ≤ T_J ≤ +150°C	30			

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that TJ = TA. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self heating where TJ > TA.
(2) Typical Values represent the most likely parametric norm.
(3) All limits are guaranteed by testing or statistical analysis.
(4) Offset voltage average drift determined by dividing the change in VOS at temperature extremes into the total temperature change.
(5) Positive current corresponds to current flowing into the device.
(6) Production Short Circuit test is a momentary test. See Note 7.
(7) Allowable Output Short Circuit duration is infinite for VS ≤ 6V at room temperature and below. For VS > 6V, allowable short circuit duration is 1.5 ms.

Electrical Characteristics 2.7 V (continued)

Unless otherwise specified, all limits guaranteed for T_A = 25°C, V^+ = 2.7 V, V^- = 0 V, V_{CM} = 0.5 V, V_O = V^+/2, and R_L > 1 MΩ to V^-.(1)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX(3)	UNIT
I_S	Supply Current	No load, V_{CM} = 0.5 V			0.95	1.20	mA
			−65°C ≤ T_J ≤ +150°C			1.50	
SR	Slew Rate(8)	A_V = +1,V_I = 2 V_{PP}			9		V/µs
f_u	Unity Gain-Frequency	V_I = 10 mV, R_L = 2 KΩ to V^+/2			10		MHz
GBWP	Gain Bandwidth Product	f = 50 KHz			21	15.5	MHz
			−65°C ≤ T_J ≤ +150°C	14			
Phi_m	Phase Margin	V_I = 10 mV			50		Deg
e_n	Input-Referred Voltage Noise	f = 2 KHz, R_S = 50 Ω			15		nV/ √Hz
i_n	Input-Referred Current Noise	f = 2 KHz			1		pA/ √Hz
f_{MAX}	Full Power Bandwidth	Z_L = (20 pF || 10 KΩ) to V^+/2			1		MHz

(8) Slew rate is the slower of the rising and falling slew rates. Connected as a Voltage Follower.

6.6 Electrical Characteristics 5 V[1]

Unless otherwise specified, all limited guaranteed for T_A = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = 1 V, V_O = V^+/2, and R_L > 1 MΩ to V^-.

PARAMETER		TEST CONDITIONS		MIN	TYP[2]	MAX[3]	UNIT
V_{OS}	Input Offset Voltage	V_{CM} = 1 V & V_{CM} = 4.5 V			+/−0.7	+/−5	mV
			−65°C ≤ T_J ≤ +150°C			+/− 7	
TC V_{OS}	Input Offset Average Drift	V_{CM} = 1 V & V_{CM} = 4.5 V[4]			+/−2		µV/°C
I_B	Input Bias Current	V_{CM} = 1 V[5]			−1.18	−2.00	µA
			−65°C ≤ T_J ≤ +150°C			−2.70	
		V_{CM} = 4.5 V[5]			+0.49	+1.00	
			−65°C ≤ T_J ≤ +150°C			+1.60	
I_{OS}	Input Offset Current	V_{CM} = 1 V & V_{CM} = 4.5 V			20	250	nA
			−65°C ≤ T_J ≤ +150°C			400	
CMRR	Common Mode Rejection Ratio	V_{CM} stepped from 0 V to 3.3 V			110	84	dB
			−65°C ≤ T_J ≤ +150°C	72			
		V_{CM} stepped from 4 V to 5 V			100		
		V_{CM} stepped from 0 V to 5 V			80	64	
			−65°C ≤ T_J ≤ +150°C	61			
+PSRR	Positive Power Supply Rejection Ratio	V^+ = 2.7 V to 5 V, V_{CM} = 0.5 V			104	78	dB
			−65°C ≤ T_J ≤ +150°C	74			
CMVR	Input Common-Mode Voltage Range	CMRR > 50 dB			−0.3	−0.1	V
			−65°C ≤ T_J ≤ +150°C			0.0	
					5.3	5.1	V
			−65°C ≤ T_J ≤ +150°C	5.0			
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5 to 4.5 V, R_L = 10 K to V^-			84	74	dB
			−65°C ≤ T_J ≤ +150°C	70			
		V_O = 0.5 to 4.5 V, R_L = 2 K to V^-			80	70	
			−65°C ≤ T_J ≤ +150°C	66			
V_O	Output Swing High	R_L = 10 K to V^-			4.87	4.75	V
			−65°C ≤ T_J ≤ +150°C	4.72			
		R_L = 2 K to V^-			4.81	4.70	
			−65°C ≤ T_J ≤ +150°C	4.66			
	Output Swing Low	R_L = 10 K to V^-			86	125	mV
			−65°C ≤ T_J ≤ +150°C			135	
I_{SC}	Output Short Circuit Current	Sourcing to V^-, V_{ID} = 200 mV[6][7]			53	35	mA
			−65°C ≤ T_J ≤ +150°C	20			
		Sinking to V^+, V_{ID} = −200 mV[6][7]			75	60	
			−65°C ≤ T_J ≤ +150°C	50			

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that TJ = TA. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self heating where TJ > TA.
(2) Typical Values represent the most likely parametric norm.
(3) All limits are guaranteed by testing or statistical analysis.
(4) Offset voltage average drift determined by dividing the change in VOS at temperature extremes into the total temperature change.
(5) Positive current corresponds to current flowing into the device.
(6) Production Short Circuit test is a momentary test. See Note 7.
(7) Allowable Output Short Circuit duration is infinite for VS ≤ 6V at room temperature and below. For VS > 6V, allowable short circuit duration is 1.5ms.

Electrical Characteristics 5 V[1] (continued)

Unless otherwise specified, all limited guaranteed for T_A = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = 1 V, V_O = V^+/2, and R_L > 1 MΩ to V^-.

PARAMETER		TEST CONDITIONS		MIN	TYP[2]	MAX[3]	UNIT
I_S	Supply Current	No load, V_{CM} = 1 V			0.97	1.25	mA
			−65°C ≤ T_J ≤ +150°C			1.75	
SR	Slew Rate[8]	A_V = +1, V_I = 5 V_{PP}			12	10	V/µs
			−65°C ≤ T_J ≤ +150°C	7			
f_u	Unity Gain Frequency	V_I = 10 mV, R_L = 2 KΩ to V^+/2			10.5		MHz
GBWP	Gain-Bandwidth Product	f = 50 KHz			21	16	MHz
			−65°C ≤ T_J ≤ +150°C	15			
Phi_m	Phase Margin	V_I = 10 mV			53		Deg
e_n	Input-Referred Voltage Noise	f = 2 KHz, R_S = 50 Ω			15		nV/ $\sqrt{hZ}$
i_n	Input-Referred Current Noise	f = 2 KHz			1		pA/ $\sqrt{hZ}$
f_{MAX}	Full Power Bandwidth	Z_L = (20 pF || 10 kΩ) to V^+/2			900		KHz
t_S	Settling Time (±5%)	100 mV_{PP} Step, 500 pF load			400		ns
THD+N	Total Harmonic Distortion + Noise	R_L = 1 KΩ to V^+/2 f = 10 KHz to A_V= +2, 4 V_{PP} swing			0.05%		

(8) Slew rate is the slower of the rising and falling slew rates. Connected as a Voltage Follower.

6.7 Electrical Characteristics ±15 V(1)

Unless otherwise specified, all limited guaranteed for T_A = 25°C, V^+ = 15 V, V^- = −15 V, V_{CM} = 0 V, V_O = 0 V, and R_L > 1 MΩ to 0 V.

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX(3)	UNIT
V_{OS}	Input Offset Voltage	V_{CM} = −14.5 V & V_{CM} = 14.5 V			+/−0.7	+/−7	mV
			−65°C ≤ T_J ≤ +150°C			+/− 9	
TC V_{OS}	Input Offset Average Drift	V_{CM} = −14.5 V & V_{CM} = 14.5 V(4)			+/−2		µV/°C
I_B	Input Bias Current	V_{CM} = −14.5 V(5)			−1.05	−2.00	µA
			−65°C ≤ T_J ≤ +150°C			−2.80	
		V_{CM} = 14.5 V(5)			+0.49	+1.00	
			−65°C ≤ T_J ≤ +150°C			+1.50	
I_{OS}	Input Offset Current	V_{CM} = −14.5 V & V_{CM} = 14.5 V			30	275	nA
			−65°C ≤ T_J ≤ +150°C			550	
CMRR	Common Mode Rejection Ratio	V_{CM} stepped from −15 V to 13 V			100	84	dB
			−65°C ≤ T_J ≤ +150°C	80			
		V_{CM} stepped from 14 V to 15 V			100		
		V_{CM} stepped from −15 V to 15 V			88	74	
			−65°C ≤ T_J ≤ +150°C	72			
+PSRR	Positive Power Supply Rejection Ratio	V^+ = 12 V to 15 V			100	70	dB
			−65°C ≤ T_J ≤ +150°C	66			
−PSRR	Negative Power Supply Rejection Ratio	V^- = −12 V to −15 V			100	70	dB
			−65°C ≤ T_J ≤ +150°C	66			
CMVR	Input Common-Mode Voltage Range	CMRR > 50 dB			−15.3	−15.1	V
			−65°C ≤ T_J ≤ +150°C			−15.0	
					15.3	15.1	V
			−65°C ≤ T_J ≤ +150°C	15.0			
A_{VOL}	Large Signal Voltage Gain	V_O = 0 V to ±13 V, R_L = 10 KΩ			85	78	dB
			−65°C ≤ T_J ≤ +150°C	74			
		V_O = 0 V to ±13 V, R_L = 2 KΩ			79	72	
			−65°C ≤ T_J ≤ +150°C	66			
V_O	Output Swing High	R_L = 10 KΩ			14.83	14.65	V
			−65°C ≤ T_J ≤ +150°C	14.61			
		R_L = 2 KΩ			14.73	14.60	
			−65°C ≤ T_J ≤ +150°C	14.55			
	Output Swing Low	R_L = 10 KΩ			−14.91	−14.75	V
			−65°C ≤ T_J ≤ +150°C			−14.65	
		R_L = 2 KΩ			−14.83	−14.65	
			−65°C ≤ T_J ≤ +150°C			−14.60	
I_{SC}	Output Short Circuit Current	Sourcing to ground V_{ID} = 200 mV(6)(7)			60	40	mA
			−65°C ≤ T_J ≤ +150°C	25			
		Sinking to ground V_{ID} = 200 mV(6)(7)			100	70	
			−65°C ≤ T_J ≤ +150°C	60			

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self heating where $T_J > T_A$.
(2) Typical Values represent the most likely parametric norm.
(3) All limits are guaranteed by testing or statistical analysis.
(4) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(5) Positive current corresponds to current flowing into the device.
(6) Production Short Circuit test is a momentary test. See Note 7.
(7) Allowable Output Short Circuit duration is infinite for V_S ≤ 6 V at room temperature and below. For V_S > 6 V, allowable short circuit duration is 1.5 ms.

Electrical Characteristics ±15 V(1) (continued)

Unless otherwise specified, all limited guaranteed for T_A = 25°C, V^+ = 15 V, V^- = −15 V, V_{CM} = 0 V, V_O = 0 V, and R_L > 1 MΩ to 0 V.

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX(3)	UNIT
I_S	Supply Current	No load, V_{CM} = 0 V			1.30	1.50	mA
			−65°C ≤ T_J ≤ +150°C			1.90	
SR	Slew Rate(8)	A_V = +1, V_I = 24 V_{PP}			15	10	V/µs
			−65°C ≤ T_J ≤ +150°C	8			
f_u	Unity Gain Frequency	V_I = 10 mV, R_L = 2 KΩ			14		MHz
GBWP	Gain-Bandwidth Product	f = 50 KHz			24	18	MHz
			−65°C ≤ T_J ≤ +150°C	16			
Phi_m	Phase Margin	V_I = 10 mV			58		Deg
e_n	Input-Referred Voltage Noise	f = 2 KHz, R_S = 50 Ω			15		nV/ √hZ
i_n	Input-Referred Current Noise	f = 2 KHz			1		pA/ √hZ
f_{MAX}	Full Power Bandwidth	Z_L = 20 pF || 10 KΩ			160		KHz
t_s	Settling Time (±1%, A_V = +1)	Positive Step, 5 V_{PP}			320		ns
		Negative Step, 5 V_{PP}			600		
THD+N	Total Harmonic Distortion +Noise	R_L = 1 KΩ, f = 10 KHz, A_V = +2, 28V_{PP} swing			0.01%		

(8) Slew rate is the slower of the rising and falling slew rates. Connected as a Voltage Follower.

6.8 Typical Characteristics

T_A = 25°C, Unless Otherwise Noted

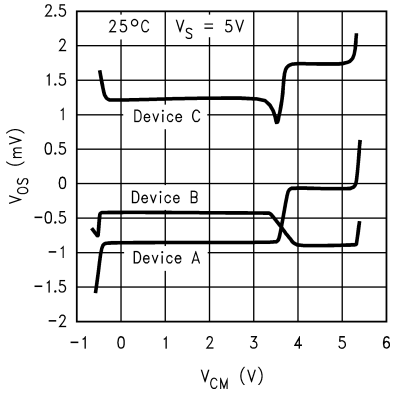


Figure 1. V_{OS} vs. V_{CM} for 3 Representative Units

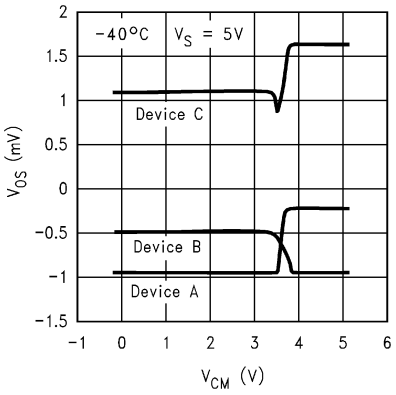


Figure 2. V_{OS} vs. V_{CM} for 3 Representative Units

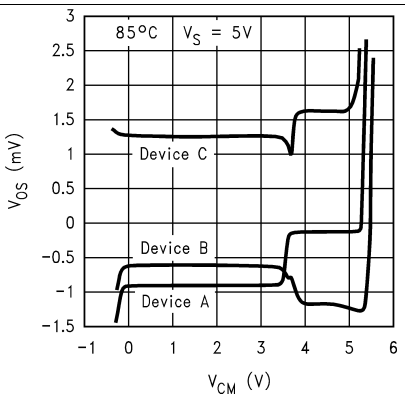


Figure 3. V_{OS} vs. V_{CM} for 3 Representative Units

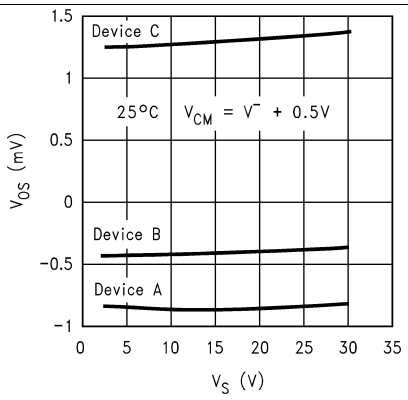


Figure 4. V_{OS} vs. V_S for 3 Representative Units

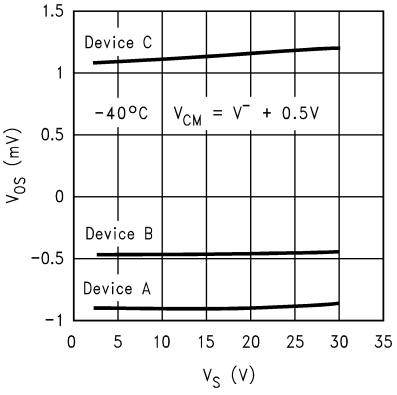


Figure 5. V_{OS} vs. V_S for 3 Representative Units

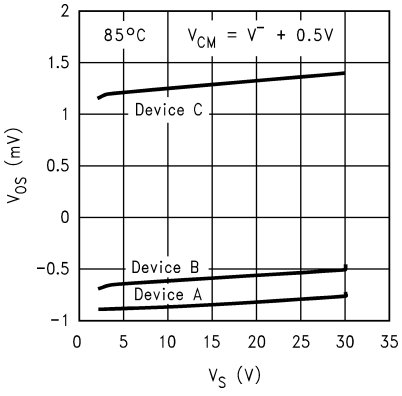


Figure 6. V_{OS} vs. V_S for 3 Representative Units

Typical Characteristics (continued)

T_A = 25°C, Unless Otherwise Noted

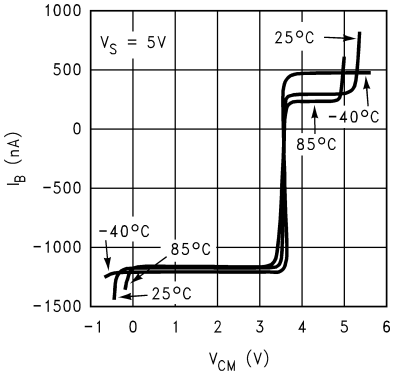


Figure 7. I_B vs. V_{CM}

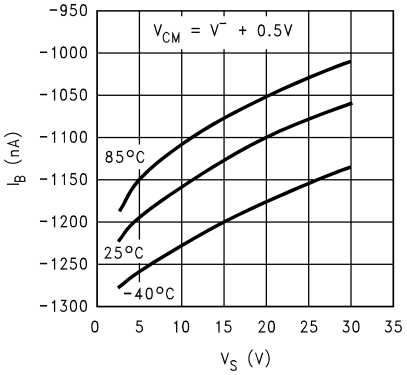


Figure 8. I_B vs. V_S

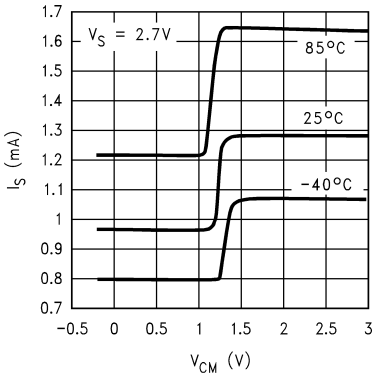


Figure 9. I_S vs. V_{CM}

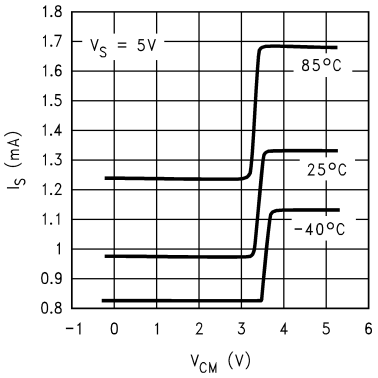


Figure 10. I_S vs. V_{CM}

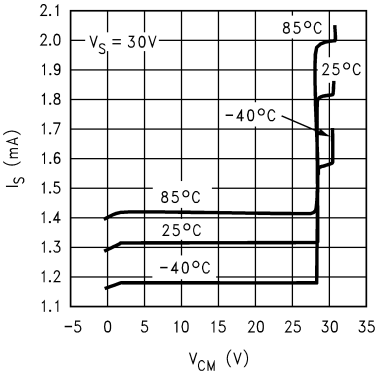


Figure 11. I_S vs. V_{CM}

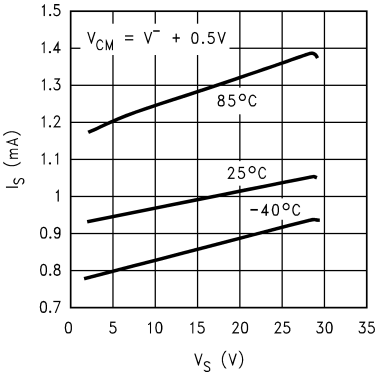


Figure 12. I_S vs. V_S (PNP side)

Typical Characteristics (continued)

T_A = 25°C, Unless Otherwise Noted

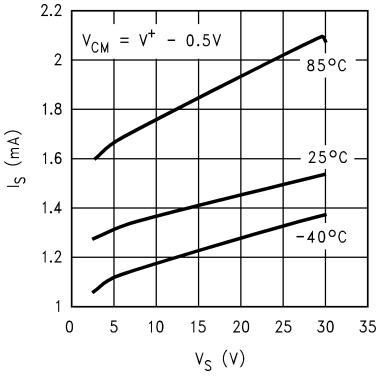


Figure 13. I_S vs. V_S (NPN side)

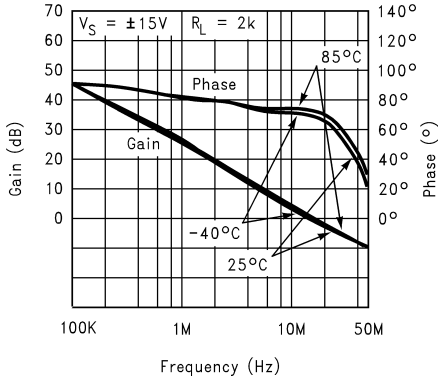


Figure 14. Gain/Phase vs. Frequency

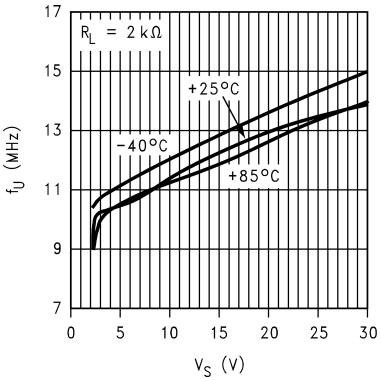


Figure 15. Unity Gain Frequency vs. V_S

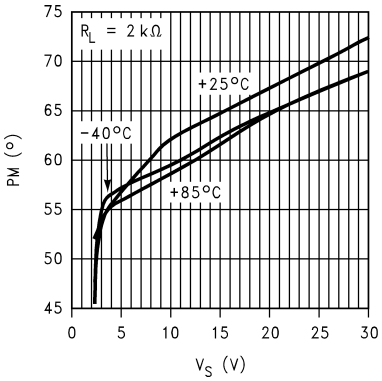


Figure 16. Phase Margin vs. V_S

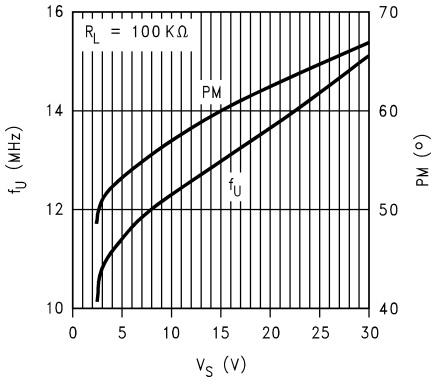


Figure 17. Unity Gain Freq. and Phase Margin vs. V_S

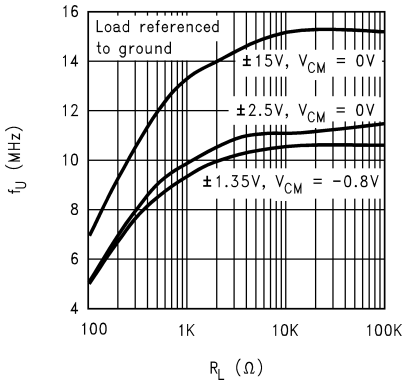


Figure 18. Unity Gain Frequency vs. Load

Typical Characteristics (continued)

T_A = 25°C, Unless Otherwise Noted

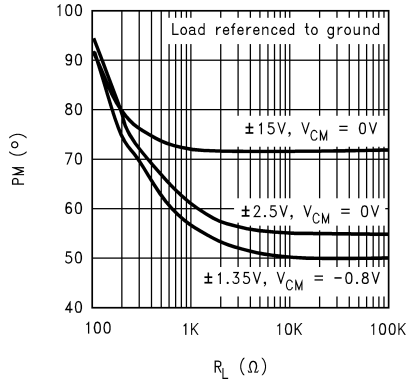


Figure 19. Phase Margin vs. Load

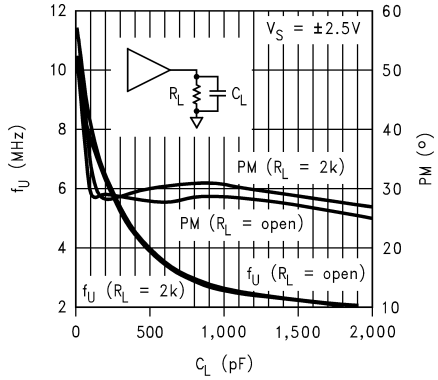


Figure 20. Unity Gain Freq. and Phase Margin vs. C_L

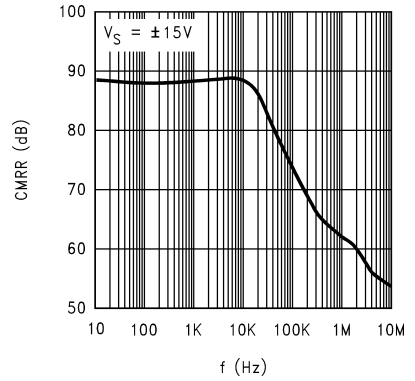


Figure 21. CMRR vs. Frequency

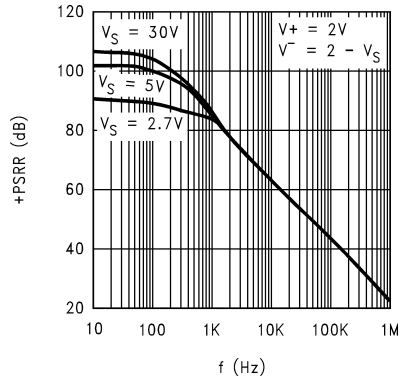


Figure 22. +PSRR vs. Frequency

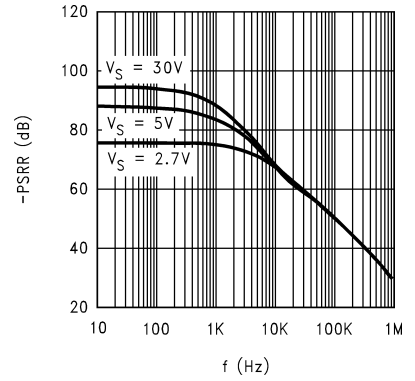


Figure 23. −PSRR vs. Frequency

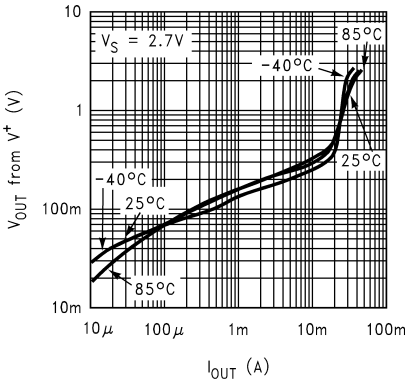


Figure 24. Output Voltage vs. Output Sourcing Current

Typical Characteristics (continued)

T_A = 25°C, Unless Otherwise Noted

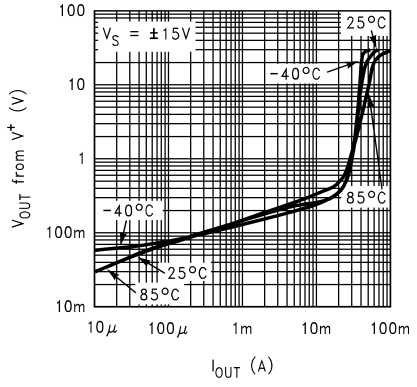


Figure 25. Output Voltage vs. Output Sourcing Current

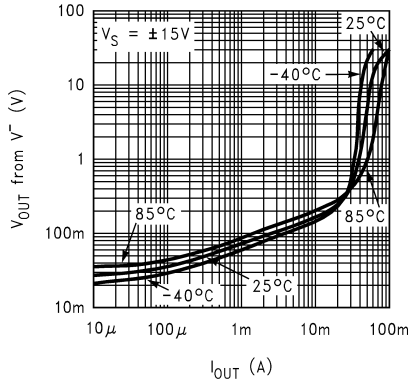


Figure 26. Output Voltage vs. Output Sinking Current

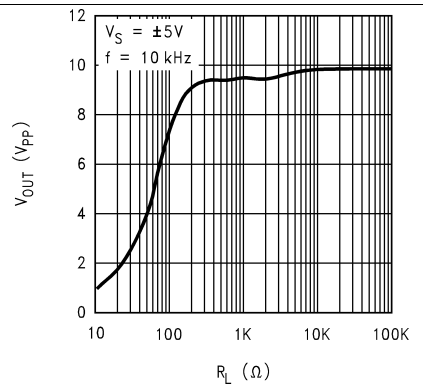


Figure 27. Max Output Swing vs. Load

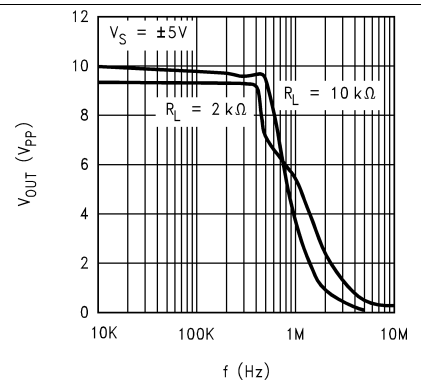


Figure 28. Max Output Swing vs. Frequency

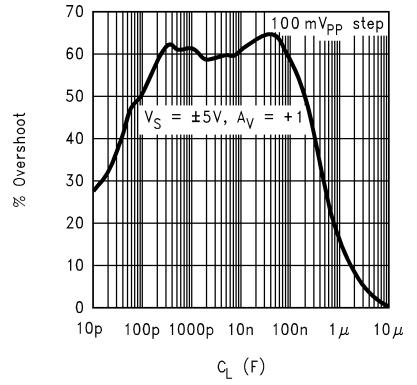


Figure 29. % Overshoot vs. Cap Load

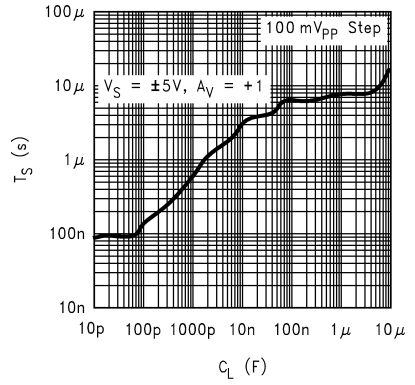


Figure 30. ±5% Settling Time vs. Cap Load

Typical Characteristics (continued)

T_A = 25°C, Unless Otherwise Noted

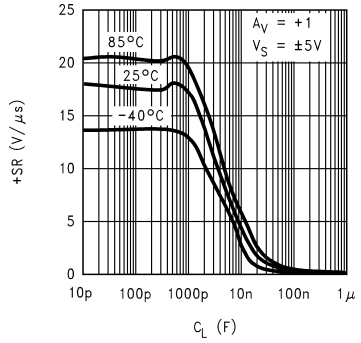


Figure 31. +SR vs. Cap Load

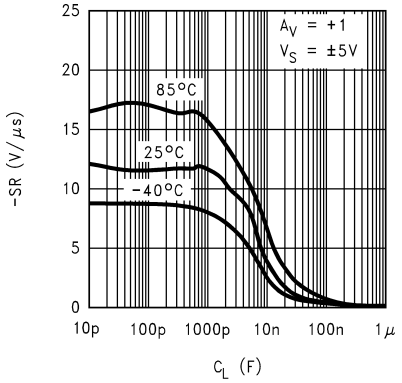


Figure 32. −SR vs. Cap Load

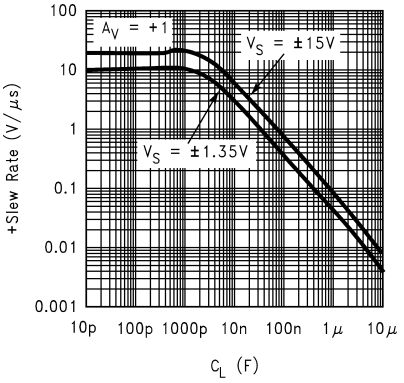


Figure 33. +SR vs. Cap Load

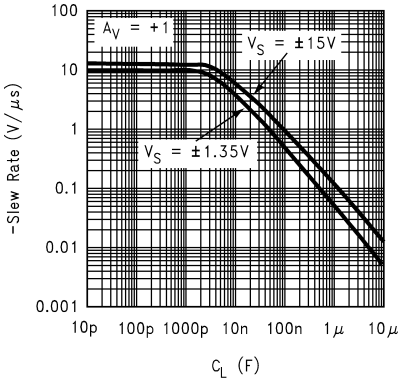


Figure 34. −SR vs. Cap Load

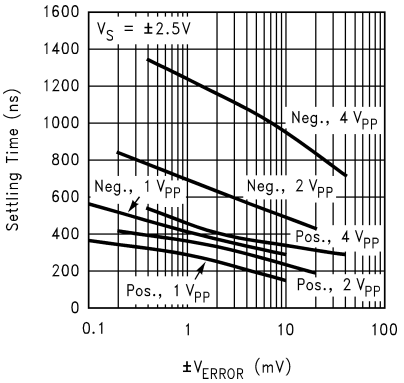


Figure 35. Settling Time vs. Error Voltage

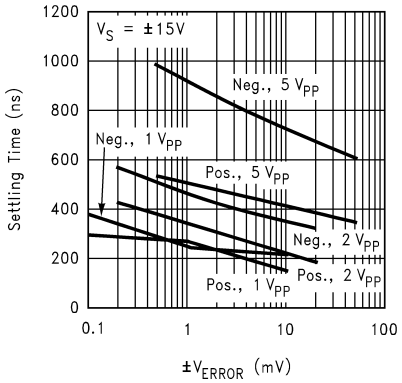


Figure 36. Settling Time vs. Error Voltage

Typical Characteristics (continued)

T_A = 25°C, Unless Otherwise Noted

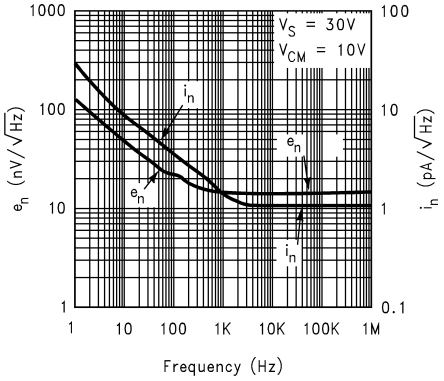


Figure 37. Input Noise Voltage/Current vs. Frequency

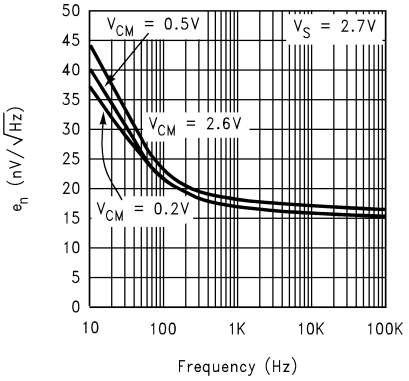


Figure 38. Input Noise Voltage for Various V_{CM}

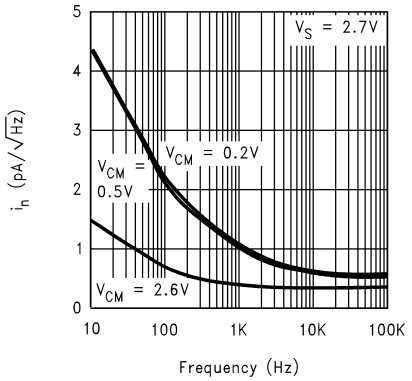


Figure 39. Input Noise Current for Various V_{CM}

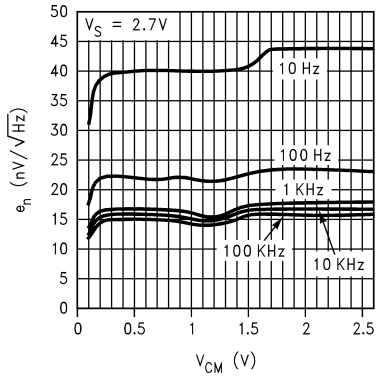


Figure 40. Input Noise Voltage vs. V_{CM}

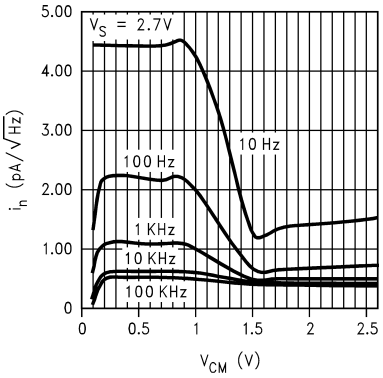


Figure 41. Input Noise Current vs. V_{CM}

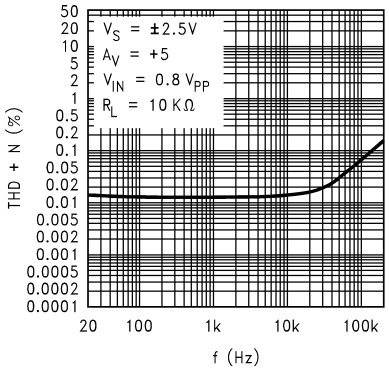


Figure 42. THD+N vs. Frequency

Typical Characteristics (continued)

T_A = 25°C, Unless Otherwise Noted

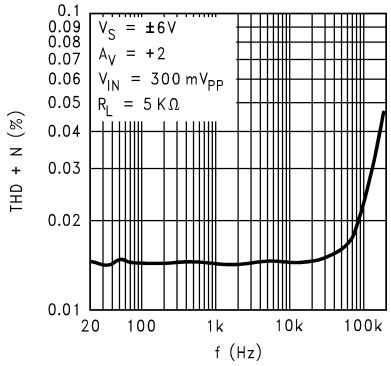


Figure 43. THD+N vs. Frequency

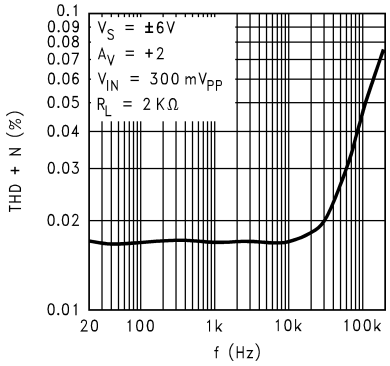


Figure 44. THD+N vs. Frequency

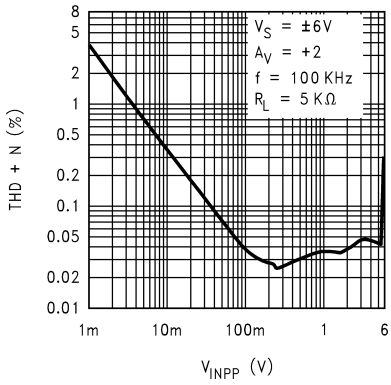


Figure 45. THD+N vs. Amplitude

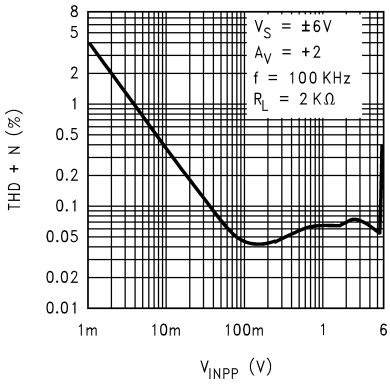


Figure 46. THD+N vs. Amplitude

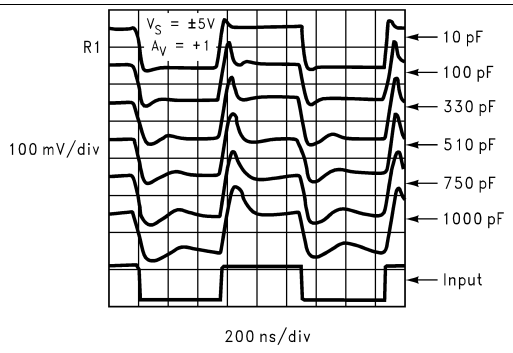


Figure 47. Small Signal Step Response

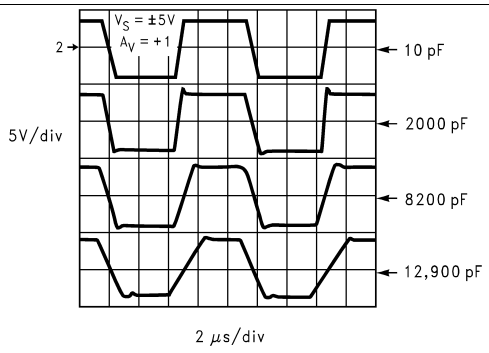


Figure 48. Large Signal Step Response

7 Application and Implementation

7.1 Block Diagram and Operational Description

7.1.1 A) Input Stage

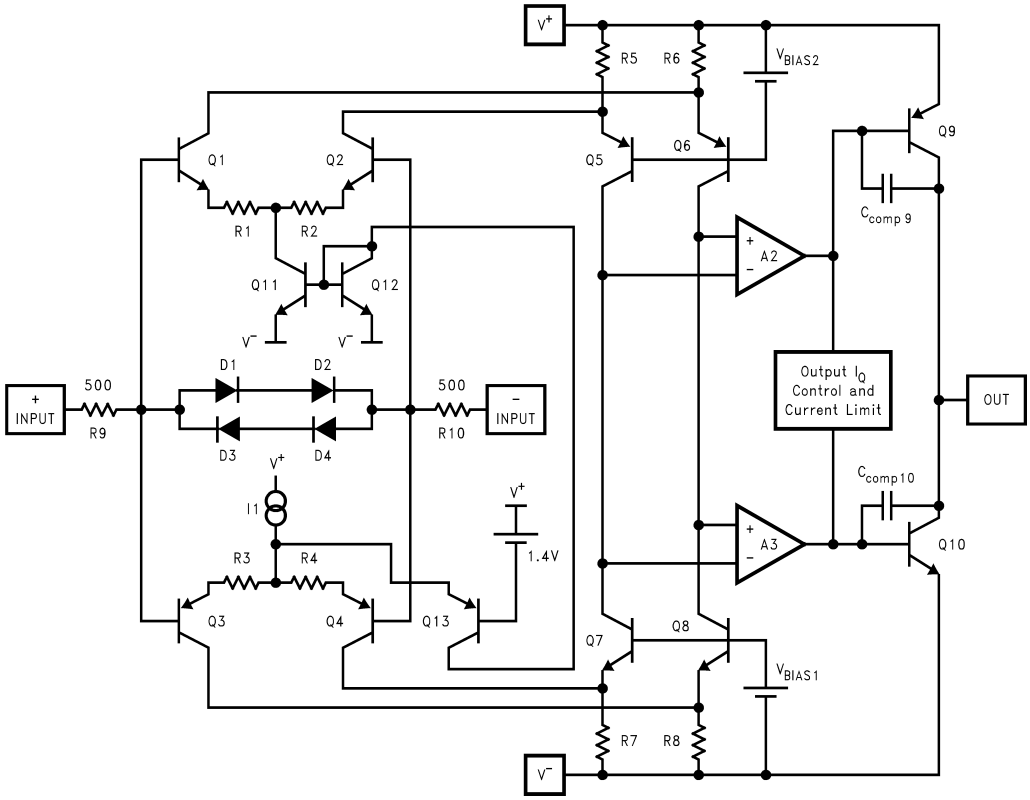


Figure 49. Simplified Schematic Diagram

As seen in Figure 49, the input stage consists of two distinct differential pairs (Q1-Q2 and Q3-Q4) in order to accommodate the full Rail-to-Rail input common mode voltage range. The voltage drop across R5, R6, R7, and R8 is kept to less than 200 mV in order to allow the input to exceed the supply rails. Q13 acts as a switch to steer current away from Q3-Q4 and into Q1-Q2, as the input increases beyond 1.4 V of V^+. This in turn shifts the signal path from the bottom stage differential pair to the top one and causes a subsequent increase in the supply current.

In transitioning from one stage to another, certain input stage parameters (V_{OS}, I_b, I_{OS}, e_n, and i_n) are determined based on which differential pair is "on" at the time. Input Bias current, I_B, will change in value and polarity as the input crosses the transition region. In addition, parameters such as PSRR and CMRR which involve the input offset voltage will also be effected by changes in V_{CM} across the differential pair transition region.

The input stage is protected with the combination of R9-R10 and D1, D2, D3, and D4 against differential input over-voltages. This fault condition could otherwise harm the differential pairs or cause offset voltage shift in case of prolonged over voltage. As shown in Figure 50, if this voltage reaches approximately ±1.4 V at 25°C, the diodes turn on and current flow is limited by the internal series resistors (R9 and R10). The Absolute Maximum Rating of ±10 V differential on V_{IN} still needs to be observed. With temperature variation, the point were the diodes turn on will change at the rate of 5 mV/°C.

Block Diagram and Operational Description (continued)

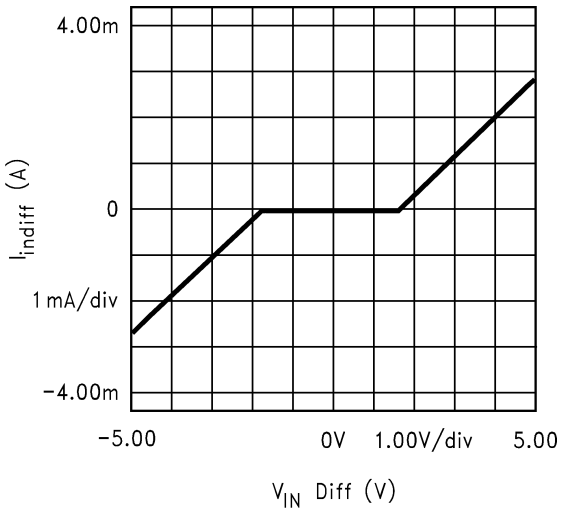


Figure 50. Input Stage Current vs. Differential Input Voltage

7.1.2 B) Output Stage

The output stage Figure 49 is comprised of complementary NPN and PNP common-emitter stages to permit voltage swing to within a $V_{CE(SAT)}$ of either supply rail. Q9 supplies the sourcing and Q10 supplies the sinking current load. Output current limiting is achieved by limiting the V_{CE} of Q9 and Q10; using this approach to current limiting, alleviates the draw back to the conventional scheme which requires one V_{BE} reduction in output swing.

The frequency compensation circuit includes Miller capacitors from collector to base of each output transistor (see Figure 49, C_{comp9} and C_{comp10}). At light capacitive loads, the high frequency gain of the output transistors is high, and the Miller effect increases the effective value of the capacitors thereby stabilizing the Op Amp. Large capacitive loads greatly decrease the high frequency gain of the output transistors thus lowering the effective internal Miller capacitance - the internal pole frequency increases at the same time a low frequency pole is created at the Op Amp output due to the large load capacitor. In this fashion, the internal dominant pole compensation, which works by reducing the loop gain to less than 0dB when the phase shift around the feedback loop is more than 180°C, varies with the amount of capacitive load and becomes less dominant when the load capacitor has increased enough. Hence the Op Amp is very stable even at high values of load capacitance resulting in the uncharacteristic feature of stability under all capacitive loads.

7.2 Driving Capacitive Loads

The LM8261 is specifically designed to drive unlimited capacitive loads without oscillations (See Figure 30). In addition, the output current handling capability of the device allows for good slewing characteristics even with large capacitive loads (see Slew Rate vs. Cap Load plots, Figure 31 through Figure 34). The combination of these features is ideal for applications such as TFT flat panel buffers, A/D converter input amplifiers, and so forth.

However, as in most Op Amps, addition of a series isolation resistor between the Op Amp and the capacitive load improves the settling and overshoot performance.

Output current drive is an important parameter when driving capacitive loads. This parameter will determine how fast the output voltage can change. Referring to the Slew Rate vs. Cap Load Plots (Figure 31 through Figure 34), two distinct regions can be identified. Below about 10,000pF, the output Slew Rate is solely determined by the Op Amp's compensation capacitor value and available current into that capacitor. Beyond 10nF, the Slew Rate is determined by the Op Amp's available output current. Note that because of the lower output sourcing current compared to the sinking one, the Slew Rate limit under heavy capacitive loading is determined by the positive transitions. An estimate of positive and negative slew rates for loads larger than 100nF can be made by dividing the short circuit current value by the capacitor.

Driving Capacitive Loads (continued)

For the LM8261, the available output current increases with the input overdrive. As seen in Figure 51 and Figure 52, both sourcing and sinking short circuit current increase as input overdrive increases. In a closed loop amplifier configuration, during transient conditions while the fed back output has not quite caught up with the input, there will be an overdrive imposed on the input allowing more output current than would normally be available under steady state condition. Because of this feature, the Op Amp's output stage quiescent current can be kept to a minimum, thereby reducing power consumption, while enabling the device to deliver large output current when the need arises (such as during transients).

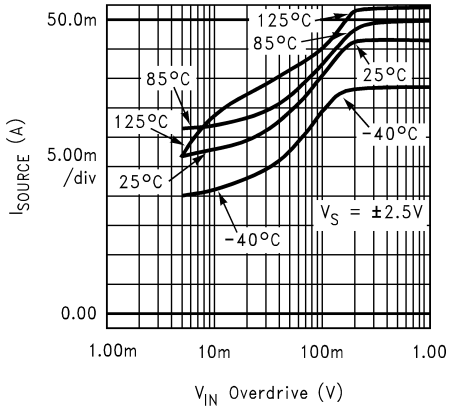


Figure 51. Output Short Circuit Sourcing Current vs. Input Overdrive

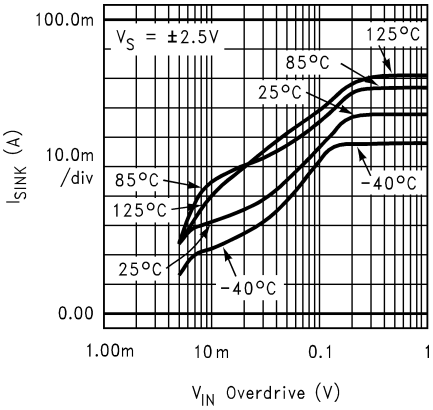


Figure 52. Output Short Circuit Sinking Current vs. Input Overdrive

Driving Capacitive Loads (continued)

Figure 53 shows the output voltage, output current, and the resulting input overdrive with the device set for A_V = +1 and the input tied to a $1V_{PP}$ step function driving a 47nF capacitor. During the output transition, the input overdrive reaches 1 V peak and is more than enough to cause the output current to increase to its maximum value (see Figure 51 and Figure 52). Because the larger output sinking current is compared to the sourcing one, the output negative transition is faster than the positive one.

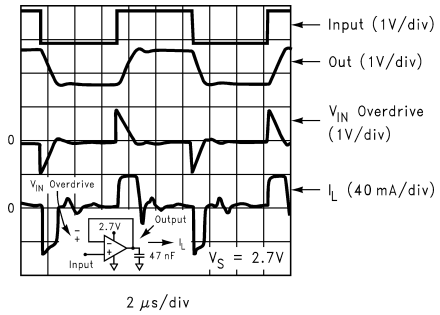


Figure 53. Buffer Amplifier Scope Photo

7.3 Estimating the Output Voltage Swing

It is important to keep in mind that the steady state output current will be less than the current available when there is an input overdrive present. For steady state conditions, Figure 24 through Figure 26 in *Typical Characteristics* can be used to predict the output swing. Figure 54 and Figure 55 show this performance along with several load lines corresponding to loads tied between the output and ground. In each cases, the intersection of the device plot at the appropriate temperature with the load line would be the typical output swing possible for that load. For example, a 1-KΩ load can accommodate an output swing to within 250 mV of V^- and to 330 mV of V^+ (V_S = ±15 V) corresponding to a typical 29.3 V_{PP} unclipped swing.

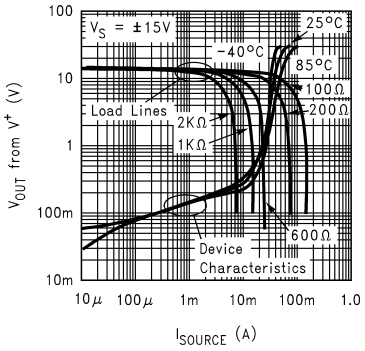


Figure 54. Output Sourcing Characteristics with Load Lines

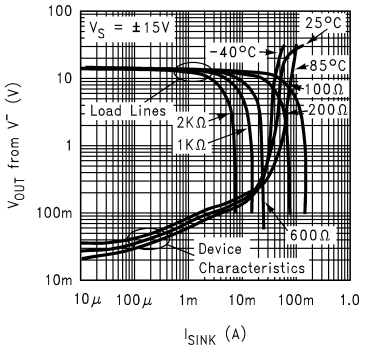


Figure 55. Output Sinking Characteristics with Load Lines

7.4 TFT Applications

Figure 56 below, shows a typical application where the LM8261 is used as a buffer amplifier for the V_{COM} signal employed in a TFT LCD flat panel:

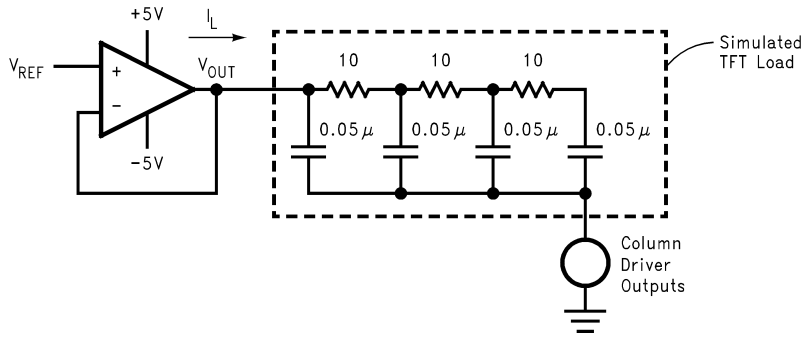


Figure 56. V_{COM} Driver Application Schematic

Figure 57 shows the time domain response of the amplifier when used as a V_{COM} buffer/driver with V_{REF} at ground. In this application, the Op Amp loop will try and maintain its output voltage based on the voltage on its non-inverting input (V_{REF}) despite the current injected into the TFT simulated load. As long as this load current is within the range tolerable by the LM8261 (45 mA sourcing and 65 mA sinking for ±5 V supplies), the output will settle to its final value within less than 2 µs.

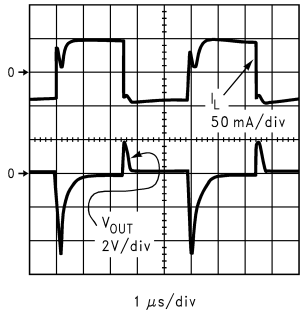


Figure 57. V_{COM} Driver Performance Scope Photo

7.5 Output Short Circuit Current and Dissipation Issues

The LM8261 output stage is designed for maximum output current capability. Even though momentary output shorts to ground and either supply can be tolerated at all operating voltages, longer lasting short conditions can cause the junction temperature to rise beyond the absolute maximum rating of the device, especially at higher supply voltage conditions. Below supply voltage of 6 V, output short circuit condition can be tolerated indefinitely.

With the Op Amp tied to a load, the device power dissipation consists of the quiescent power due to the supply current flow into the device, in addition to power dissipation due to the load current. The load portion of the power itself could include an average value (due to a DC load current) and an AC component. DC load current would flow if there is an output voltage offset, or the output AC average current is non-zero, or if the Op Amp operates in a single supply application where the output is maintained somewhere in the range of linear operation. Therefore:

$$P_{TOTAL} = P_Q + P_{DC} + P_{AC} \quad (1)$$

Op Amp Quiescent Power Dissipation:

$$P_Q = I_S \cdot V_S \quad (2)$$

DC Load Power:

$$P_{DC} = I_O \cdot (V_R - V_O) \quad (3)$$

AC Load Power:

P_{AC} = (outlined in table below)

Output Short Circuit Current and Dissipation Issues (continued)

where

- I_S is Supply Current
- V_S is Total Supply Voltage ($V^+ - V^-$)
- I_O is Average Load Current
- V_O is Average Output Voltage
- V_R is V^+ for sourcing and V^- for sinking current (4)

Table 1 shows the maximum AC component of the load power dissipated by the Op Amp for standard Sinusoidal, Triangular, and Square Waveforms:

Table 1. Normalized AC Power Dissipated in the Output Stage for Standard Waveforms

P_{AC} ($W.\Omega/V^2$)		
Sinusoidal	Triangular	Square
50.7×10^{-3}	46.9×10^{-3}	62.5×10^{-3}

The table entries are normalized to V_S^2/ R_L. To calculate the AC load current component of power dissipation, simply multiply the table entry corresponding to the output waveform by the factor V_S^2/ R_L. For example, with ±15 V supplies, a 600-Ω load, and triangular waveform power dissipation in the output stage is calculated as:

$$P_{AC} = (46.9 \times 10^{-3}) \cdot [30^2/600] = 70.4 \text{ mW} \quad (5)$$

7.6 Other Application Hints

The use of supply decoupling is mandatory in most applications. As with most relatively high speed/high output current Op Amps, best results are achieved when each supply line is decoupled with two capacitors; a small value ceramic capacitor (~0.01 µF) placed very close to the supply lead in addition to a large value Tantalum or Aluminum (> 4.7 µF). The large capacitor can be shared by more than one device if necessary. The small ceramic capacitor maintains low supply impedance at high frequencies while the large capacitor will act as the charge "bucket" for fast load current spikes at the Op Amp output. The combination of these capacitors will provide supply decoupling and will help keep the Op Amp oscillation free under any load.

7.6.1 LM8261 Advantages

Compared to other Rail-to-Rail Input/Output devices, the LM8261 offers several advantages such as:

- Improved cross over distortion.
- Nearly constant supply current throughout the output voltage swing range and close to either rail.
- Consistent stability performance for all input/output voltage and current conditions.
- Nearly constant Unity gain frequency (f_u) and Phase Margin (Phi_m) for all operating supplies and load conditions.
- No output phase reversal under input overload condition.

8 Power Supply Recommendations

The LM8261 can operate off a single supply or with dual supplies. The input CM capability of the parts (CMVR) extends covers the entire supply voltage range for maximum flexibility. Supplies should be decoupled with low inductance, often ceramic, capacitors to ground less than 0.5 inches from the device pins. The use of ground plane is recommended, and as in most high speed devices, it is advisable to remove ground plane close to device sensitive pins such as the inputs.

9 Layout

9.1 Layout Guidelines

Generally, a good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillations. Texas Instruments suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization. See Table 2 for details. The LM8261 evaluation board(s) is a good example of high frequency layout techniques as a reference. General high-speed, signal-path layout suggestions include:

- Continuous ground planes are preferred for signal routing with matched impedance traces for longer runs. However, open up both ground and power planes around the capacitive sensitive input and output device pins as shown in Figure 58. After the signal is sent into a resistor, parasitic capacitance becomes more of a bandlimiting issue and less of a stability issue.
- Use good, high-frequency decoupling capacitors (0.1 µF) on the ground plane at the device power pins as shown in Figure 58. Higher value capacitors (2.2 µF) are required, but may be placed further from the device power pins and shared among devices. For best high-frequency decoupling, consider X2Y supply-decoupling capacitors that offer a much higher self-resonance frequency over standard capacitors.
- When using differential signal routing over any appreciable distance, use microstrip layout techniques with matched impedance traces.
- The input summing junction is very sensitive to parasitic capacitance. Connect any Rf, and Rg elements into the summing junction with minimal trace length to the device pin side of the resistor, as shown in Figure 59. The other side of these elements can have more trace length if needed to the source or to ground.

9.2 Layout Example

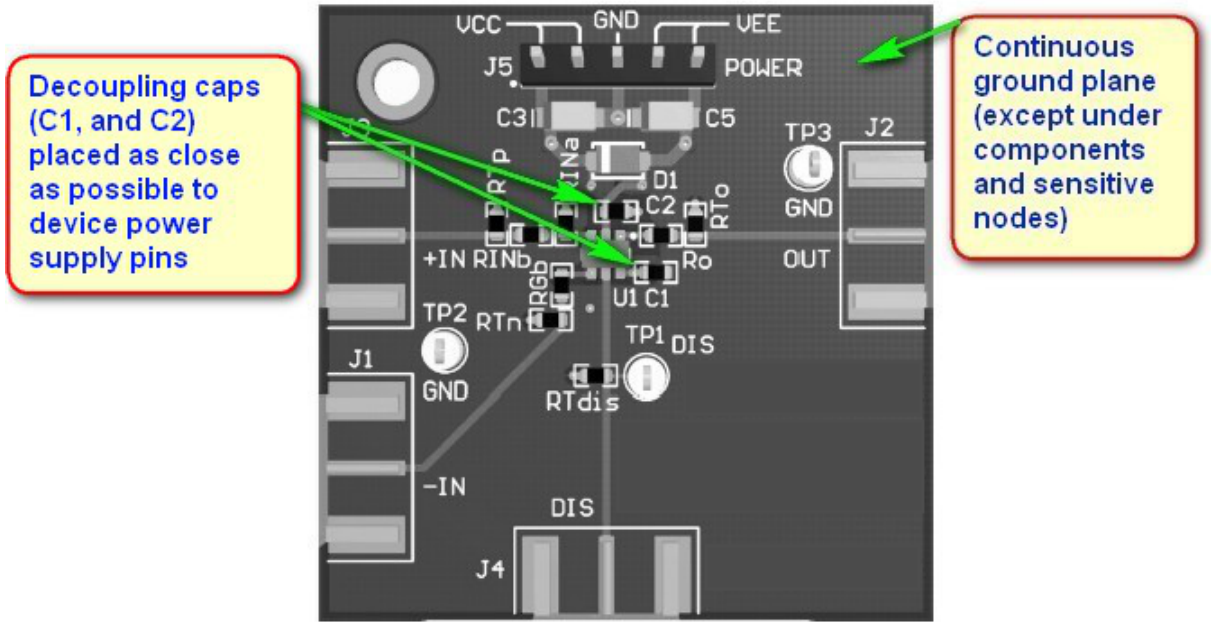


Figure 58. LM8261 Evaluation Board Layer 1

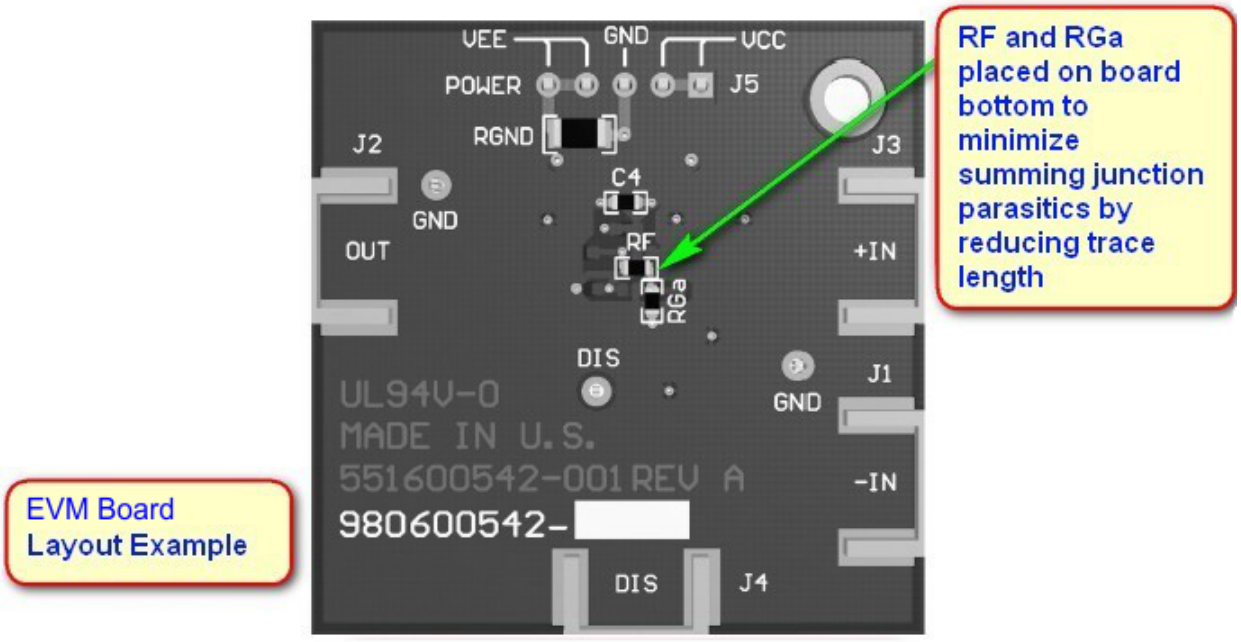


Figure 59. LM8261 Evaluation Board Layer 2

Table 2. Evaluation Board Comparison

DEVICE	PACKAGE	EVALUATION BOARD PART NUMBER
LM8261M5	SOT-23	LMH730216

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see *IC Package Thermal Metrics* Application Report, SPRA953

10.2 Trademarks

All trademarks are the property of their respective owners.

10.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

10.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM8261M5	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	A45A	
LM8261M5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A45A	Samples
LM8261M5X	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 85	A45A	
LM8261M5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A45A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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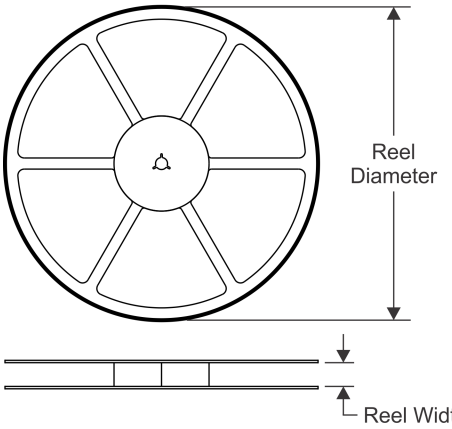
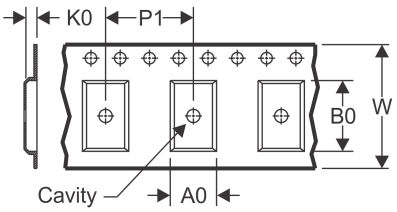
TAPE AND REEL INFORMATION

REEL DIMENSIONS

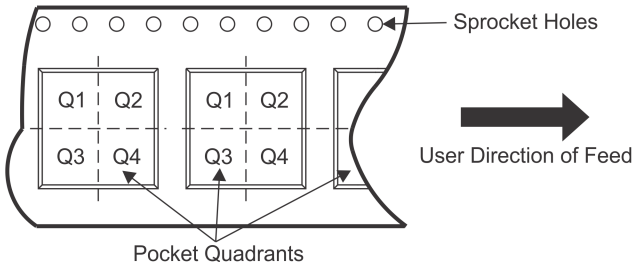


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

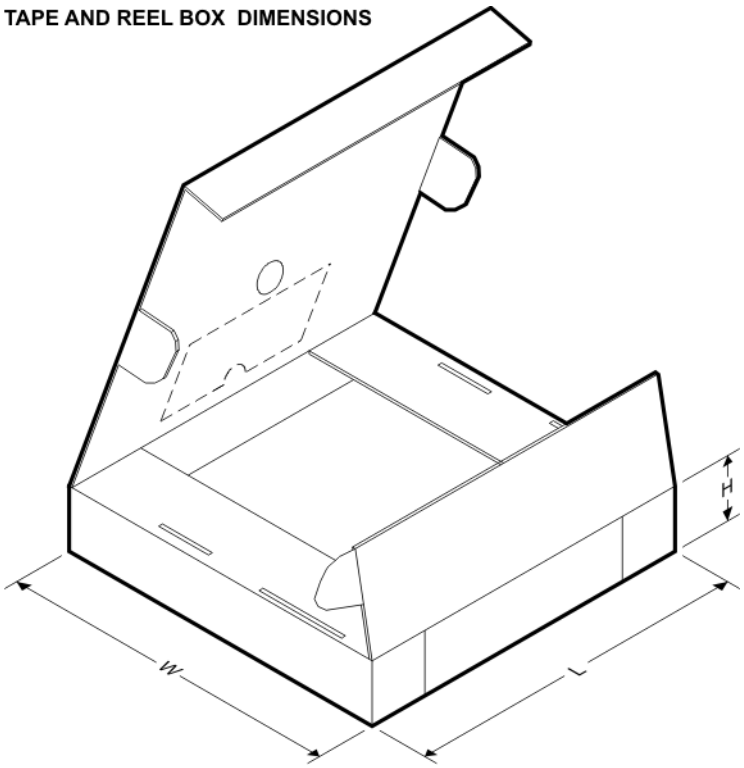
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM8261M5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM8261M5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM8261M5X	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM8261M5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

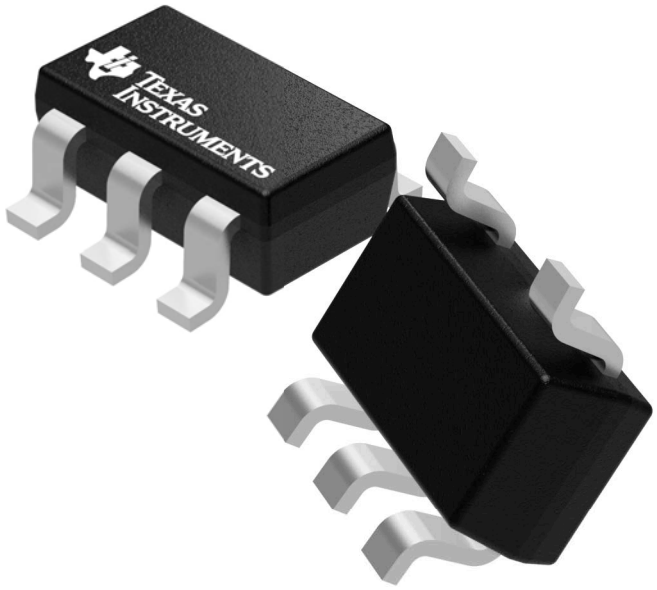


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM8261M5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM8261M5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM8261M5X	SOT-23	DBV	5	3000	210.0	185.0	35.0
LM8261M5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

DBV 5 SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



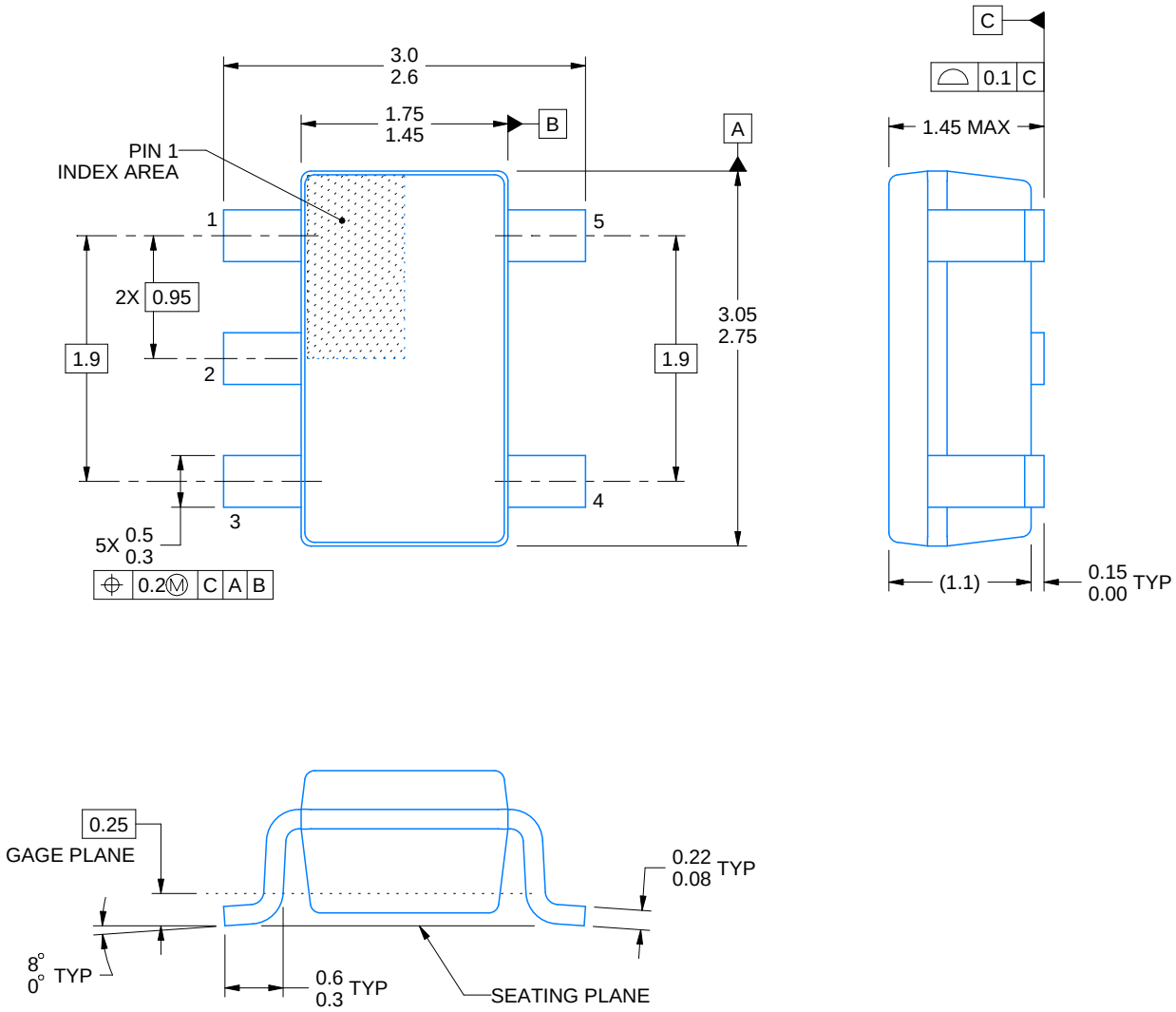
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

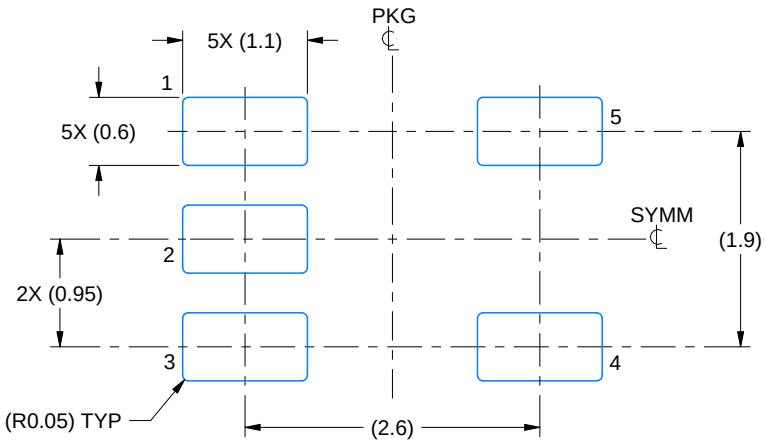
SMALL OUTLINE TRANSISTOR



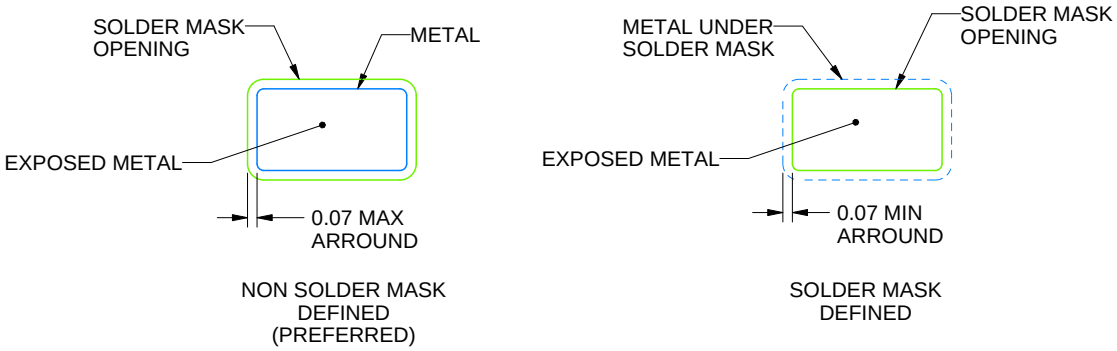
4214839/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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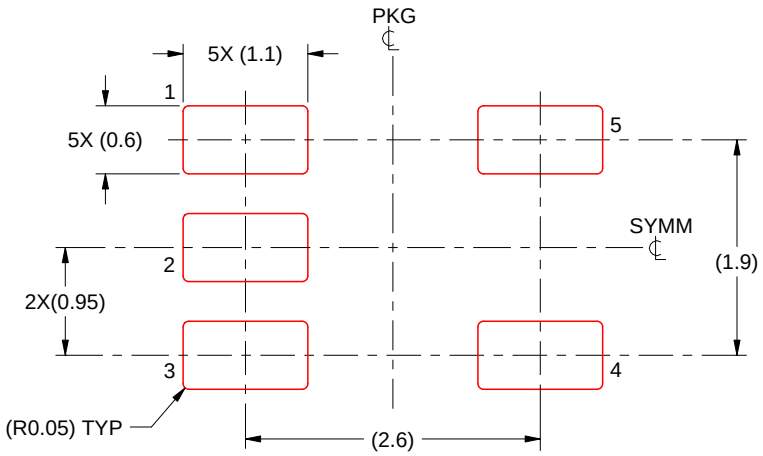
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

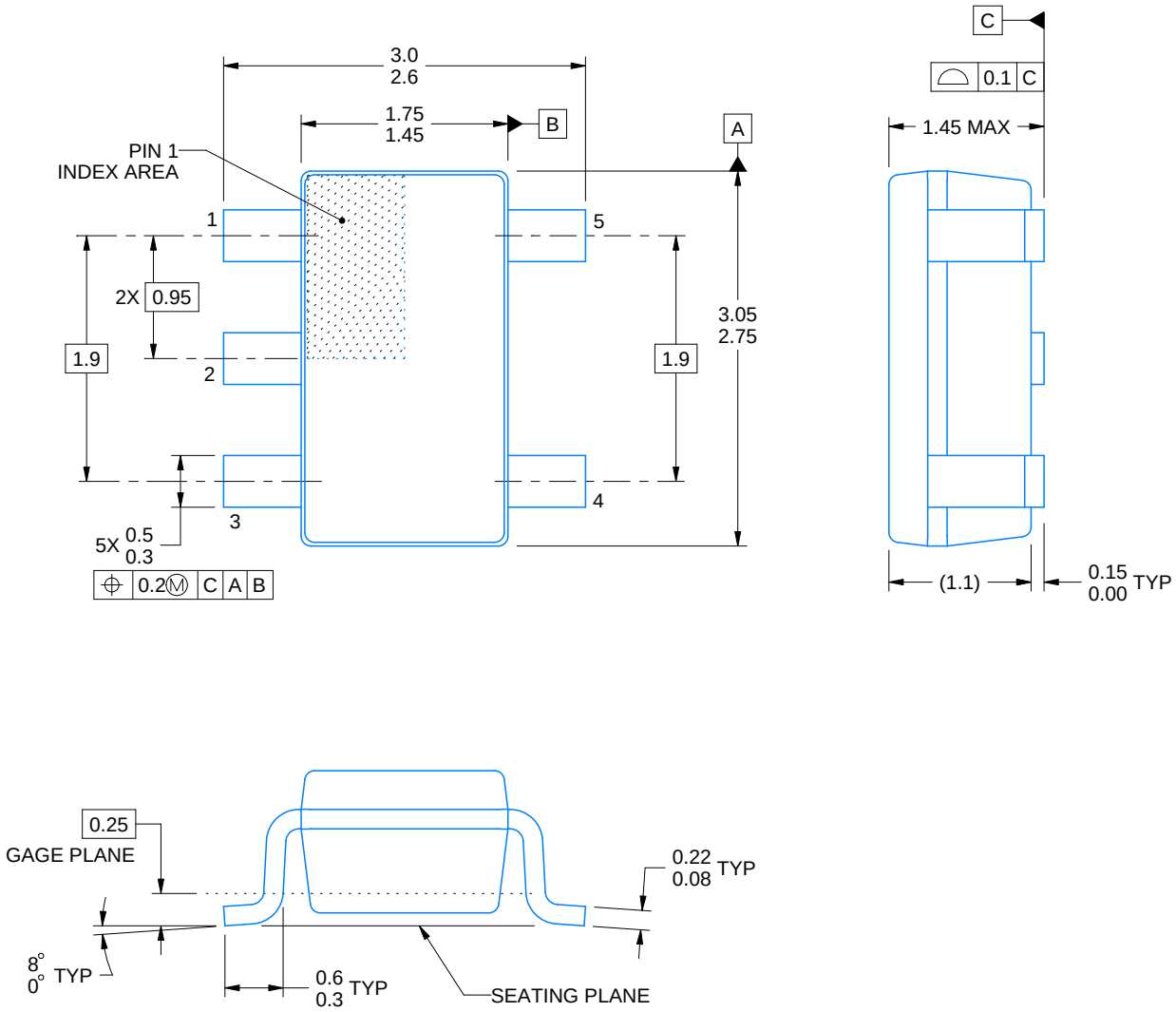
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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NOTES:

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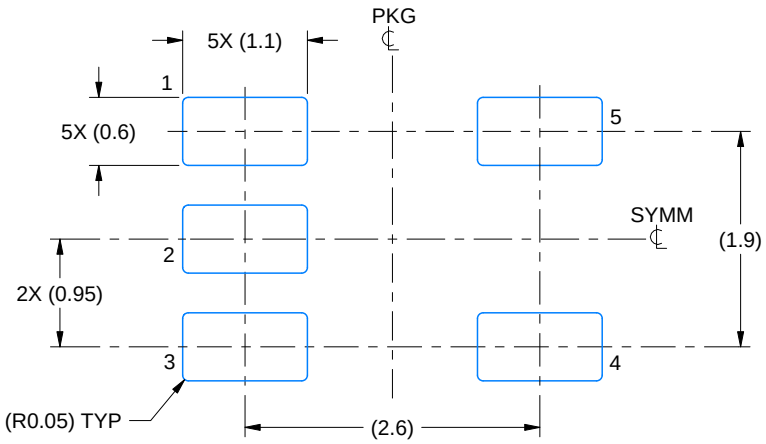
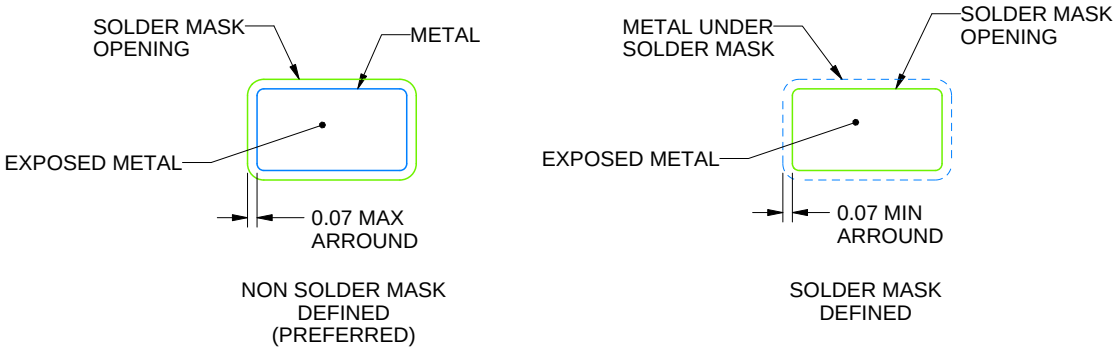


LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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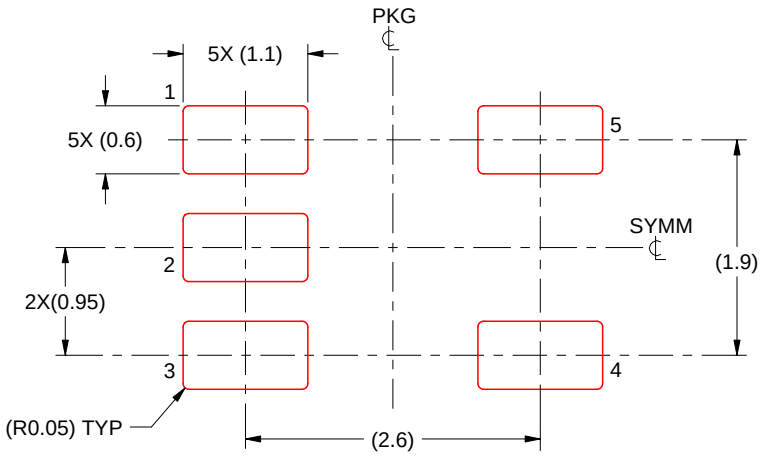
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

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