Video 8-Bit Digital-to-Analog Converter

PRODUCT DESCRIPTION

The MS5602 is a low-power and ultra high-speed video digital-to-analog converter. The MS5602 converts digital signals to analog signals at a sampling rate of DC to 20MHz. Because of its high-speed feature, the MS5602 is suitable for digital video applications, such as digital television, computer video processing and radar-signal processing.

The MS5602 operates from -40°C to 85°C.

SOP20

FEATURES

- 8-Bit Resolution
- ±0.2% Linearity
- Maximum Conversion Rate
  Typical Value: 30MHz
  Minimum Value: 20MHz
- Analog Output Voltage Range: VDD to VDD-1V
- TTL Digital Input Level
- 5V Single Power-Supply
- Low Power Dissipation: 80mW (Typ)

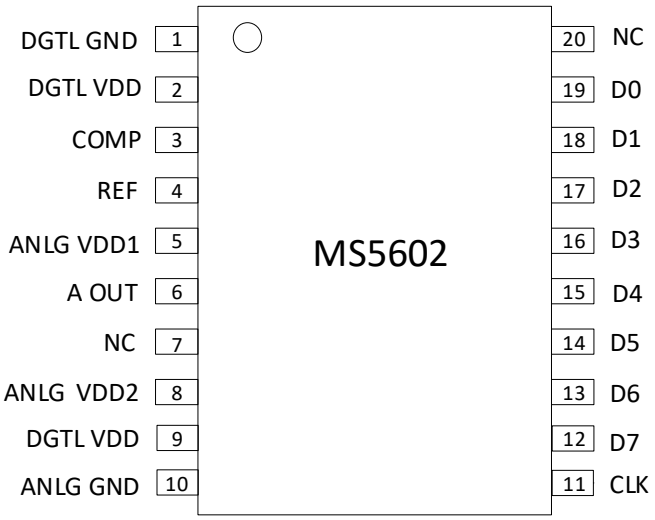
APPLICATIONS

- Digital Video Signal Conversion

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS5602	SOP20	MS5602

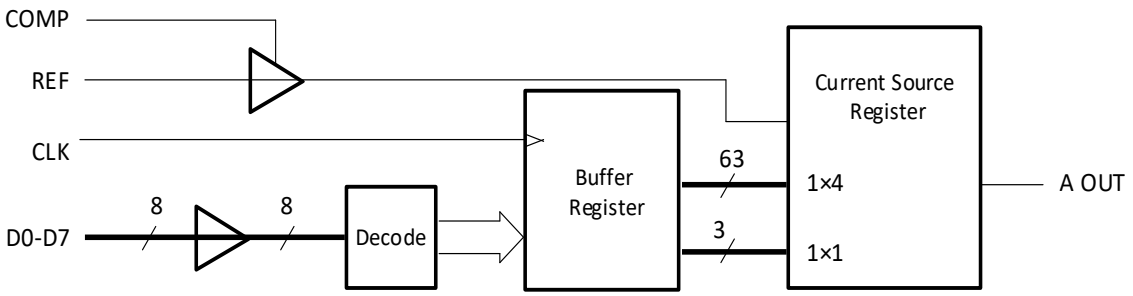
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
1	DGTL GND	-	Digital Ground
2, 9	DGTL VDD	-	Digital Power Supply
3	COMP	I/O	Phase Compensation Capacitance
4	REF	I	Input Reference Voltage
5	ANLG VDD1	-	Analog Power Supply 1
6	A OUT	O	Analog Output
7	NC	-	Not Connection
8	ANLG VDD2	-	Analog Power Supply 2
10	ANLG GND	--	Analog Ground
11	CLK	I	Clock Input
12-19	D7-D0	I	8-Bit Digital Input (D7 is high, D0 is low)
20	NC	-	Not Connection

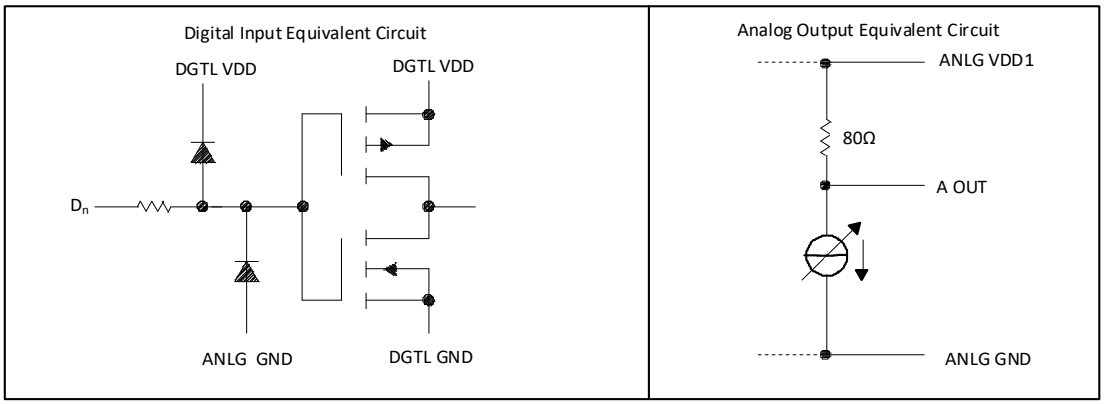
BLOCK DIAGRAM



Function Table

Phase	Digital Input								Output Voltage
	D7	D6	D5	D4	D3	D2	D1	D0	
0	L	L	L	L	L	L	L	L	3.98V
1	L	L	L	L	L	L	L	H	3.984V
~127	L	H	H	H	H	H	H	H	~4.488V
128	H	L	L	L	L	L	L	L	4.492V
129	H	L	L	L	L	L	L	H	4.496V
~254	H	H	H	H	H	H	H	L	~43996V
255	H	H	H	H	H	H	H	H	5.000V

Input and Output Equivalent Circuit:



Because ANLG GND and DGTL GND do not connect internally, so they should be tied together as close to the device terminals as possible.

ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Range	Unit
Power Supply	ANGL VDD, DGTL VDD	-0.5 ~ +7	V
Digital Input Voltage Range	V_I	-0.5 ~ VDD+0.3	V
Input Reference Voltage Range	REF	VDD-1.7V ~ VDD+0.5	V
Operating Temperature Range	T_A	-40 ~ +85	°C
Storage Temperature Range	T_{stg}	-60 ~ +150	°C
Maximum Junction Temperature	T_j	150	°C
Lead temperature (10s)		260	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply	V_{DD}	4.75	5	5.25	V
Digital High-Level Input Voltage	V_{IH}	2			V
Digital Low-Level Input Voltage	V_{IL}			0.8	V
Reference Voltage	REF	3.8	4	4.2	V
Pulse Width	t_W	25			ns
Setup Time	t_{su}	16.5			ns
Hold Time	t_h	12.5			ns
Phase Compensation Capacitance[1]	C_{COMP}	1			μA
Load Resistance	R_L	75k			Ω
Operating Temperature	T_A	-40		85	°C

Note 1: Phase compensation capacitance should be connected between COMP and ANLG GND.

ELECTRICAL CHARACTERISTICS

Electrical characteristics are in the range of power supply and operating temperature.

Parameter		Symbol	Condition	Min	Typ	Max	Unit
High-Level Input Current	Digital Input	I_{IH}	V_I=5V			±1	μA
Low-Level Input Current		I_{IL}	V_I=0V			±1	μA
Input Reference Current		I_{ref}	V_{ref}=4.02V			10	μA
Full-scale Output Voltage		V_{FS}	VDD=5V, V_{ref}=4.02V	VDD-15	VDD	VDD+15	mA
Zero-scale Output Voltage		V_{ZS}	VDD=5V, V_{ref}=4.02V	3.919	3.98	4.042	V
Output Resistance		r_O	T_A=Full Temperature Range	60	80	120	Ω
Input Capacitance		C_i	f_{clock}=1MHz, T_A=25°C		15		pF
Power Supply Current		I_{DD}	f_{clock}=20MHz, V_{ref}=VDD-0.95V	16		25	mA

All typical values are at VCC=5V, T_A=25°C.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Best-fitting Linearity Error	E_L(adj)	T_A=Full Temperature Range		±0.2		%
Endpoint Linearity Error	E_L			±0.15		%
Differential Linearity Error	E_D			±0.2		%
Differential Gain	G_{diff}	NTSC 40-IRE Standard		0.7		%
Differential Phase	Φ_{diff}	f_{clock}=14.3MHz, Z_L≧75kΩ		0.4		°
Propagation Delay, CLK to Analog Output Update Time	t_{pd}	C_L=10pF		25		ns
1/2LSB Setup Time	t_s	C_L=10pF		30		ns

Parameter Measurement Timing Diagram

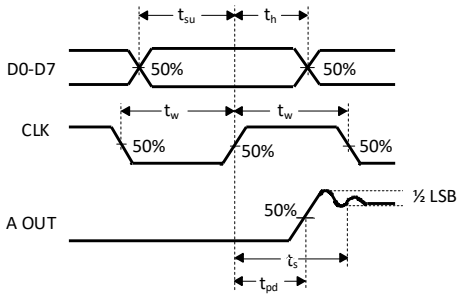


Figure 1. Voltage Waveforms

TYPICAL CHARACTERISTICS CURVE

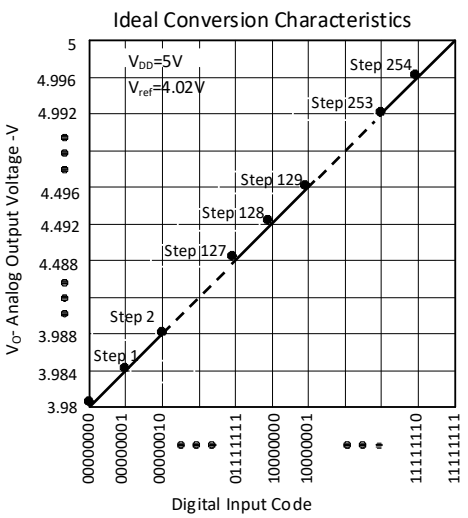


Figure 2

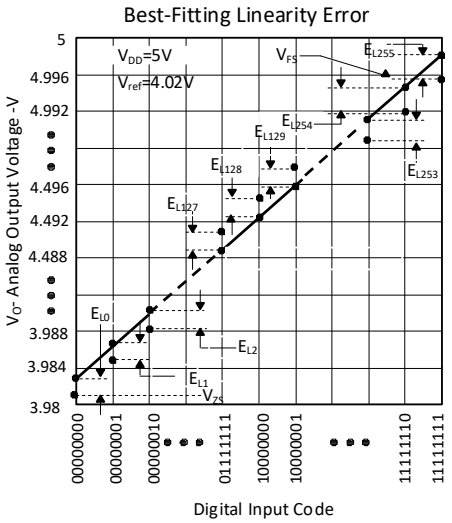
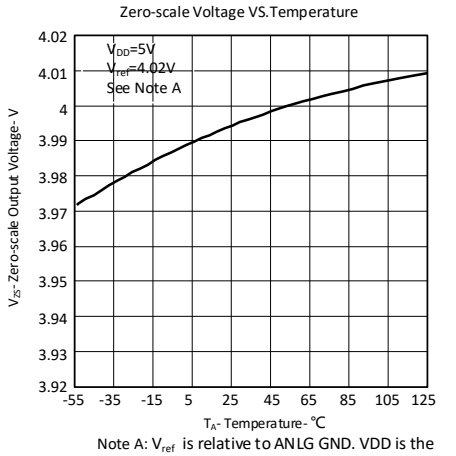


Figure 3



Note A: V_{ref} is relative to ANLG GND. VDD is the voltage between ANLG VDD and DGTL VDD tied together and ANLG GND and DGTL GND tided together.

Figure 4

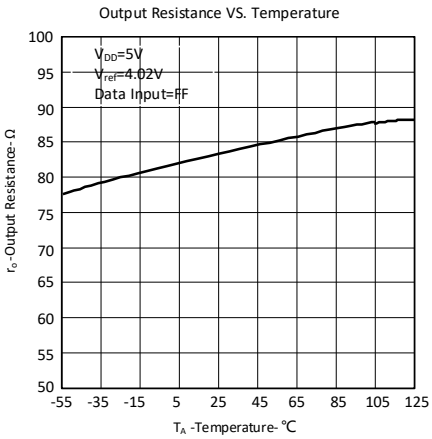


Figure 5

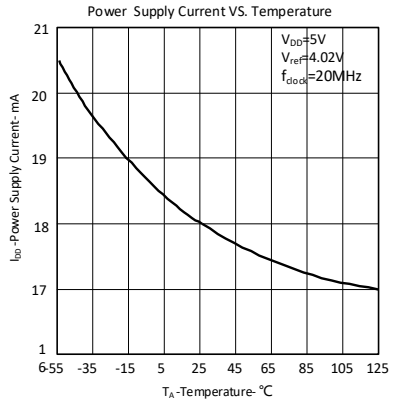
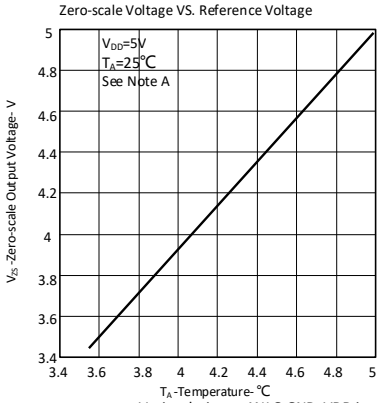


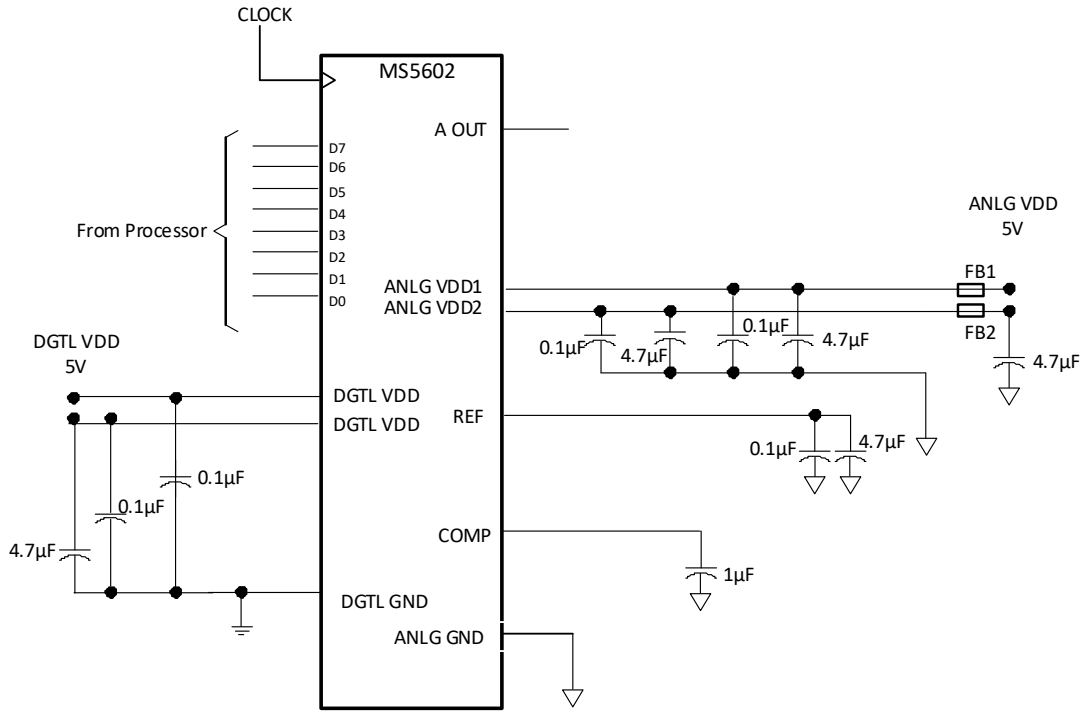
Figure 6



Note A: V_{ref} is relative to ANLG GND. VDD is the voltage between ANLG VDD and DGTL VDD tied together and ANLG GND and DGTL GND tied together.

Figure 7

TYPICAL APPLICATION DIAGRAM

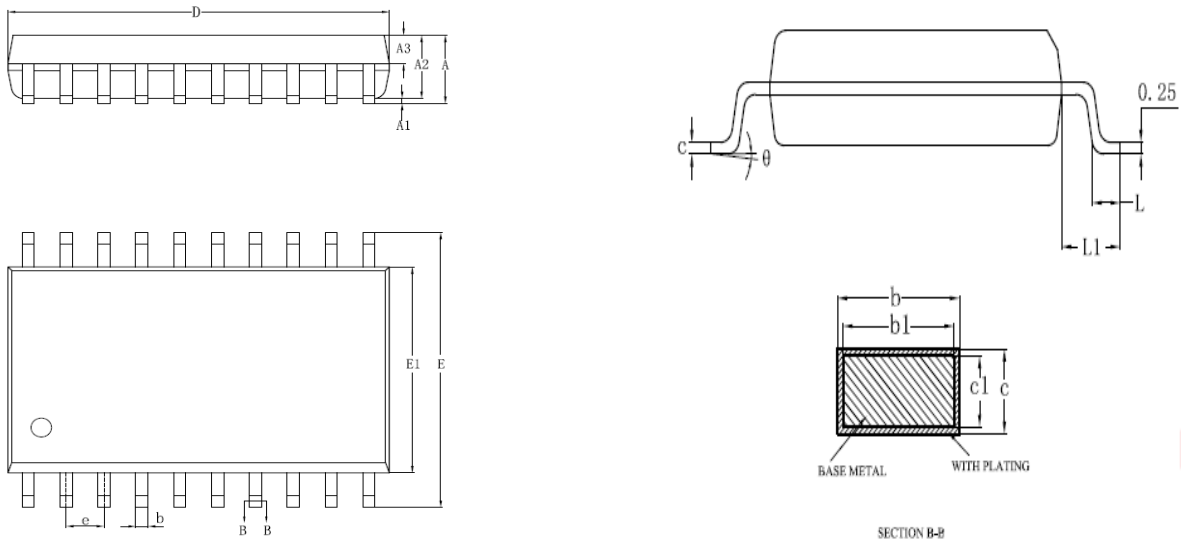


APPLICATION INFORMATION

- External analog and digital circuit should be shielded as much as possible to reduce system noise.
- RF evaluation board or RF printed-circuit-board (PCB) should be used throughout the evaluation and production process.
- Because ANLG GND and DGTL GND do not connect internally, so these terminals must be connected externally. When using the evaluation board, these ground leads should be connected to the ground plane through separated leads with normal power supply bypass. Using twisted-pair cables for power supply lines to minimize pickup noise is a good method. Using wide ground leads or ground plane on the PCB layout to minimize inductance and resistance. Ground plane is the best choice for noise reduction.
- ANLG VDD and DGTL VDD are separated internally, so they must be connected externally. These external PCB leads should be made as wide as possible. Before ANLG VDD is connected with DGTL VDD on the board, placing a ferrite bead or equivalent inductor in series with ANLG VDD. And the decoupling capacitor should be placed as close to the device terminals as possible.
- ANLG VDD to ANLG GND and DGTL VDD to DGTL GND should be decoupled with 1μF and 0.01μF capacitors respectively and placed as close to the device terminals as possible. A ceramic capacitor is recommended for 0.01μF capacitor.
- The leads between COMP and ANLG GND should be as short as possible to connect the phase compensation capacitor.
- NC pins on the small-outline package should be connected to ANLG GND.
- Using ANLG VDD and ANLG GND to separate A OUT from higher-frequency terminal CLK and D7-D0. ANLG GND traces should be placed on both sides of A OUT traces.

PACKAGE OUTLINE DIMENSIONS

SOP20



Symbol	Dimensions in Millimeters		
	Min	Typ	Max
A	-	-	2.65
A1	0.10	-	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.25	-	0.29
c1	0.24	0.25	0.26
D	12.70	12.80	12.90
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27BSC		
L	0.70	-	1.00
L1	1.40REF		
θ	0º	-	8º

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description

Product Name: MS5602

Product Code: XXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS5602	SOP20	1000	1	1000	8	8000

STATEMENT

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- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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