WINSTAR Display

OLED SPECIFICATION

Model No:

WEO002002A

General Specification

Item	Dimension	Unit
Number of Characters	20 Characters x 2 Lines	—
Module dimension	84.5 x 19.28 x 2.17	mm
View area	75.52 x 13.52	mm
Active area	73.52 x 11.52	mm
Dot size	0.62 x 0.67	mm
Dot pitch	0.65 x 0.70	mm
Character size	3.22 x 5.57	mm
Character pitch	3.70 x 5.95	mm
LCD type	OLED , Monochrome	
Duty	1/16	
IC	SSD1311	

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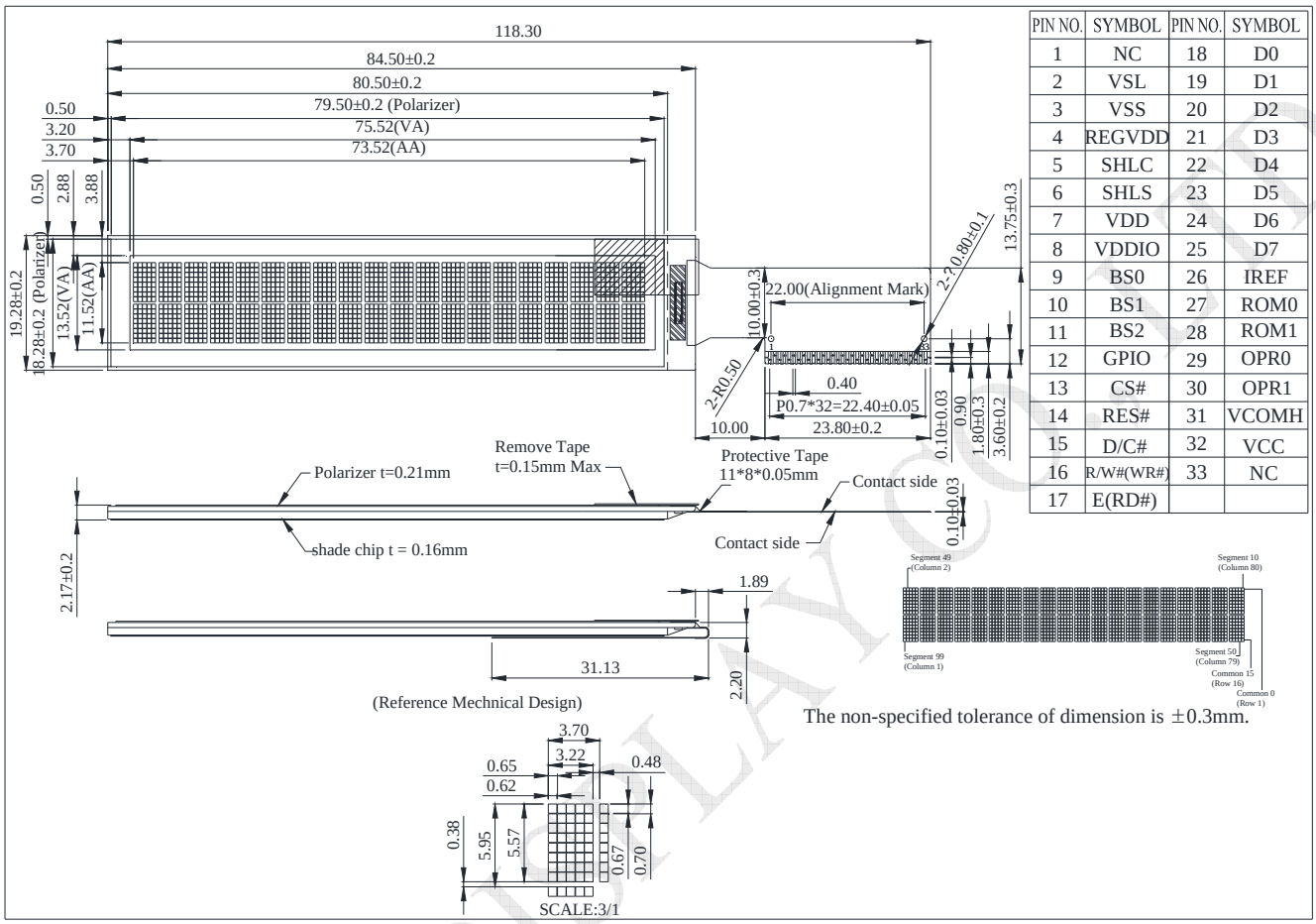
Contour Drawing & Block Diagram



PIN NO.	SYMBOL	PIN NO.	SYMBOL
1	NC	18	D0
2	VSL	19	D1
3	VSS	20	D2
4	REGVDD	21	D3
5	SHLC	22	D4
6	SHLS	23	D5
7	VDD	24	D6
8	VDDIO	25	D7
9	BS0	26	IREF
10	BS1	27	ROM0
11	BS2	28	ROM1
12	GPIO	29	OPR0
13	CS#	30	OPR1
14	RES#	31	VCOMH
15	D/C#	32	VCC
16	R/W#(WR#)	33	NC
17	E(RD#)		

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Interface Pin Function

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Pin Type</th><th>Description</th></tr>
<tr><td>1</td><td>NC</td><td>—</td><td>No connection</td></tr>
<tr><td>2</td><td>VSL</td><td>P</td><td>This is segment voltage (output low level) reference pin.
When external VSL is not used, this pin should be left open.
When external VSL is used, connect with resistor and diode to ground (details depend on application).</td></tr>
<tr><td>3</td><td>VSS</td><td>P</td><td>Ground pin. It must be connected to external ground.</td></tr>
<tr><td>4</td><td>REGVDD</td><td>I</td><td>Internal VDD regulator selection pin in 5V I/O application mode.
When this pin is pulled HIGH, internal VDD regulator is enabled (5V I/O application).
When this pin is pulled LOW, internal VDD regulator is disabled (Low voltage I/O application).</td></tr>
<tr><td>5</td><td>SHLC</td><td>I</td><td>This pin is used to determine the Common output scanning direction.
COM scan direction
<table>
<tr><td>SHLC</td><td>COM scan direction</td></tr>
<tr><td>1</td><td>COM0 to COM31 (Normal)</td></tr>
<tr><td>0</td><td>COM31 to COM0 (Reverse)</td></tr>
</table>
Note
(1) 0 is connected to VSS
(2) 1 is connected to VDDIO</td></tr>
<tr><td>6</td><td>SHLS</td><td>I</td><td>This pin is used to change the mapping between the display data column address and the Segment driver.
SEG scan direction
<table>
<tr><td>SHLS</td><td>SEG direction</td></tr>
<tr><td>1</td><td>SEG0 to SEG99 (Normal)</td></tr>
<tr><td>0</td><td>SEG99 to SEG0 (Reverse)</td></tr>
</table>
Note
(1) 0 is connected to VSS
(2) 1 is connected to VDDIO</td></tr>
<tr><td>7</td><td>VDD</td><td>P</td><td>Power supply for core logic operation.
VDD can be supplied externally or regulated internally.
In LV IO application (internal VDD is disabled), this is a power input pin.
In 5V IO application (internal VDD is enabled), VDD is regulated internally from VDDIO.
A capacitor should be connected between VDD and VSS under all circumstances.</td></tr>
<tr><td>8</td><td>VDDIO</td><td>P</td><td>Low voltage power supply and power supply for interface logic level in both Low Voltage I/O and 5V I/O application. It should match with the MCU interface voltage level and must be connected to external source.</td></tr>
<tr><td>9</td><td>BS0</td><td>I</td><td>MCU bus interface selection pins. Select appropriate logic</td></tr>
</table>

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<table>
<tr><td>10</td><td>BS1</td><td rowspan="2"></td><td rowspan="2">setting as described in the following table. BS2, BS1 and BS0 are pin select.
Bus Interface selection
<table><tr><td>BS[2:0]</td><td>Interface</td></tr><tr><td>000</td><td>Serial Interface</td></tr><tr><td>001</td><td>Invalid</td></tr><tr><td>010</td><td>I²C</td></tr><tr><td>011</td><td>Invalid</td></tr><tr><td>100</td><td>8-bit 6800 parallel</td></tr><tr><td>101</td><td>4-bit 6800 parallel</td></tr><tr><td>110</td><td>8-bit 8080 parallel</td></tr><tr><td>111</td><td>4-bit 8080 parallel</td></tr></table>Note
(1) 0 is connected to VSS
(2) 1 is connected to VDDIO</td></tr>
<tr><td>11</td><td>BS2</td></tr>
<tr><td>12</td><td>GPIO</td><td>I/O</td><td>It is a GPIO pin. Details refer to OLED command DCh.</td></tr>
<tr><td>13</td><td>CS#</td><td>I</td><td>This pin is the chip select input connecting to the MCU.
The chip is enabled for MCU communication only when CS# is pulled LOW (active LOW).
In I2C mode, this pin must be connected to VSS.</td></tr>
<tr><td>14</td><td>RES#</td><td>I</td><td>This pin is reset signal input.
When the pin is pulled LOW, initialization of the chip is executed.
Keep this pin pull HIGH during normal operation.</td></tr>
<tr><td>15</td><td>D/C#</td><td>I</td><td>This pin is Data/Command control pin connecting to the MCU.
When the pin is pulled HIGH, the data at D[7:0] will be interpreted as data.
When the pin is pulled LOW, the data at D[7:0] will be transferred to a command register.
In I2C mode, this pin acts as SA0 for slave address selection.
When serial interface is selected, this pin must be connected to VSS.</td></tr>
<tr><td>16</td><td>R/W#(WR#)</td><td>I</td><td>This pin is read / write control input pin connecting to the MCU interface.
When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW.
When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected.
When serial or I2C interface is selected, this pin must be connected to VSS.</td></tr>
</table>

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<table>
<tr><td>17</td><td>E(RD#)</td><td>I</td><td>This pin is MCU interface input.
When 6800 interface mode is selected, this pin will be used as the Enable (E) signal.
Read/write operation is initiated when this pin is pulled HIGH and the chip is selected.
When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected.
When serial or I2C interface is selected, this pin must be connected to VSS.</td></tr>
<tr><td>18</td><td>D0</td><td rowspan="8">I/O</td><td rowspan="8">These pins are bi-directional data bus connecting to the MCU data bus.
Unused pins are recommended to tie LOW.
When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SID and D2 will be the serial data output: SOD.
When I2C mode is selected, D2, D1 should be tied together and serve as SDAout, SDAin in application and D0 is the serial clock input, SCL.</td></tr>
<tr><td>19</td><td>D1</td></tr>
<tr><td>20</td><td>D2</td></tr>
<tr><td>21</td><td>D3</td></tr>
<tr><td>22</td><td>D4</td></tr>
<tr><td>23</td><td>D5</td></tr>
<tr><td>24</td><td>D6</td></tr>
<tr><td>25</td><td>D7</td></tr>
<tr><td>26</td><td>IREF</td><td>I</td><td>This pin is the segment output current reference pin.
IREF is supplied externally.
A resistor should be connected between this pin and VSS to maintain current of around 15uA.</td></tr>
<tr><td>27</td><td>ROM0</td><td rowspan="2">I</td><td rowspan="2">These pins are used to select Character ROM; select appropriate logic setting as described in the following table. ROM1 and ROM0 are pin select as shown in below table:
Character ROM selection
<table><tr><td>ROM1</td><td>ROM0</td><td>ROM</td></tr><tr><td>0</td><td>0</td><td>A</td></tr><tr><td>0</td><td>1</td><td>B</td></tr><tr><td>1</td><td>0</td><td>C</td></tr><tr><td>1</td><td>1</td><td>S/W selectable (3)</td></tr></table>Note
(1) 0 is connected to VSS
(2) 1 is connected to VDDIO</td></tr>
<tr><td>28</td><td>ROM1</td></tr>
<tr><td>29</td><td>OPR0</td><td rowspan="2">I</td><td rowspan="2">This pin is used to select the character number of character generator.
Character RAM selection
<table><tr><td>OPR1</td><td>OPR0</td><td>CGROM</td><td>CGRAM</td></tr><tr><td>1</td><td>1</td><td>256</td><td>0</td></tr><tr><td>0</td><td>1</td><td>248</td><td>8</td></tr><tr><td>1</td><td>0</td><td>250</td><td>6</td></tr><tr><td>0</td><td>0</td><td>240</td><td>8</td></tr></table>Note
(1) 0 is connected to VSS
(2) 1 is connected to VDDIO</td></tr>
<tr><td>30</td><td>OPR1</td></tr>
</table>

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31	VCOMH	P	COM signal deselected voltage level. A capacitor should be connected between this pin and VSS. No external power supply is allowed to connect to this pin.
32	VCC	P	Power supply for panel driving voltage. This is also the most positive power voltage supply pin. It is supplied by external high voltage source.
33	NC	—	No connection

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Absolute Maximum Ratings

Item	Symbol	Min	Max	Unit
Input Voltage	V_I	-0.3	VDD	V
Supply Voltage For Logic	VDD-V_{SS}	-0.3	3.6	V
Operating Temperature	T_{OP}	-40	+80	℃
Storage Temperature	T_{ST}	-40	+80	℃

Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	VDD-VSS	—	2.8	3.0	3.3	V
Supply Voltage For Display	VCC	—	8	9	10	V
Input High Volt.	VIH	—	0.8 VDD	—	—	V
Input Low Volt.	VIL	—	—	—	0.2VDD	V
Output High Volt.	VOH	IOH=-0.5mA	0.9 VDD	—	—	V
Output Low Volt.	VOL	IOL=0.5mA	—	—	0.1 VDD	V
50% Check Board operating Current	ICC	VCC=9V	14	15	18	mA

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