

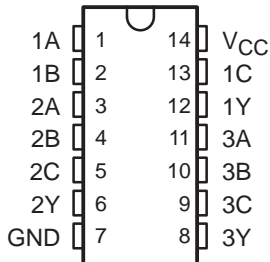
# SN54AC10, SN74AC10 TRIPLE 3-INPUT POSITIVE-NAND GATES

SCAS529D – AUGUST 1995 – REVISED OCTOBER 2003

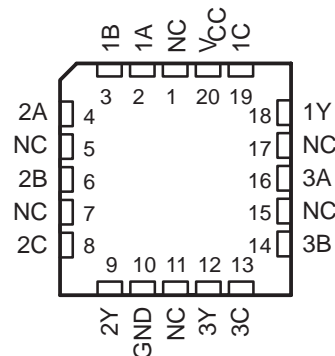
- 2-V to 6-V  $V_{CC}$  Operation
- Max  $t_{pd}$  of 6.5 ns at 5 V

- Inputs Accept Voltages to 6 V

SN54AC10 . . . J OR W PACKAGE  
SN74AC10 . . . D, DB, N, NS, OR PW PACKAGE  
(TOP VIEW)



SN54AC10 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

The 'AC10 devices contain three independent 3-input NAND gates. The devices perform the Boolean function  $Y = \overline{A \cdot B \cdot C}$  or  $Y = \overline{A} + \overline{B} + \overline{C}$  in positive logic.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube	SN74AC10N	SN74AC10N
	SOIC – D	Tube	SN74AC10D	AC10
		Tape and reel	SN74AC10DR	
	SOP – NS	Tape and reel	SN74AC10NSR	AC10
	SSOP – DB	Tape and reel	SN74AC10DBR	AC10
	TSSOP – PW	Tube	SN74AC10PW	AC10
Tape and reel		SN74AC10PWR		
-55°C to 125°C	CDIP – J	Tube	SNJ54AC10J	SNJ54AC10J
	CFP – W	Tube	SNJ54AC10W	SNJ54AC10W
	LCCC – FK	Tube	SNJ54AC10FK	SNJ54AC10FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

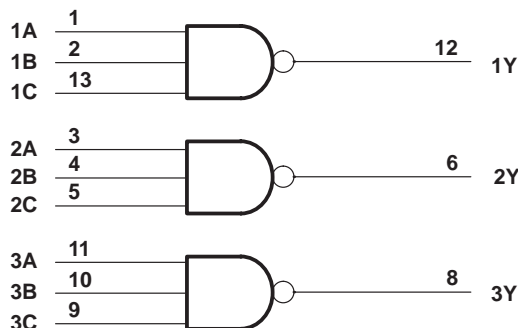
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# SN54AC10, SN74AC10 TRIPLE 3-INPUT POSITIVE-NAND GATES

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## logic diagram, each gate (positive logic)



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 200$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
D package .....	86°C/W
DB package .....	96°C/W
N package .....	80°C/W
NS package .....	76°C/W
PW package .....	113°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.



# SN54AC10, SN74AC10 TRIPLE 3-INPUT POSITIVE-NAND GATES

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## recommended operating conditions (see Note 3)

		SN54AC10		SN74AC10		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2	6	2	6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 3\text{ V}$		2.1		V
		$V_{CC} = 4.5\text{ V}$		3.15		
		$V_{CC} = 5.5\text{ V}$		3.85		
$V_{IL}$	Low-level input voltage	$V_{CC} = 3\text{ V}$		0.9		V
		$V_{CC} = 4.5\text{ V}$		1.35		
		$V_{CC} = 5.5\text{ V}$		1.65		
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 3\text{ V}$		-12		mA
		$V_{CC} = 4.5\text{ V}$		-24		
		$V_{CC} = 5.5\text{ V}$		-24		
$I_{OL}$	Low-level output current	$V_{CC} = 3\text{ V}$		12		mA
		$V_{CC} = 4.5\text{ V}$		24		
		$V_{CC} = 5.5\text{ V}$		24		
$\Delta t/\Delta v$	Input transition rise or fall rate	8		8		ns/V
$T_A$	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54AC10		SN74AC10		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$V_{OH}$	$I_{OH} = -50\ \mu\text{A}$	3 V	2.9	2.99		2.9		2.9	V	
		4.5 V	4.4	4.99		4.4		4.4		
		5.5 V	5.4	5.49		5.4		5.4		
	$I_{OH} = -12\ \text{mA}$	3 V	2.56			2.4		2.46		
		4.5 V	3.86			3.7		3.76		
	$I_{OH} = -24\ \text{mA}$	5.5 V	4.86			4.7		4.76		
		$I_{OH} = -50\ \text{mA}^\dagger$	5.5 V			3.85				
$I_{OH} = -75\ \text{mA}^\dagger$	5.5 V						3.85			
$V_{OL}$	$I_{OL} = 50\ \mu\text{A}$	3 V		0.002	0.1		0.1	0.1	V	
		4.5 V		0.001	0.1		0.1	0.1		
		5.5 V		0.001	0.1		0.1	0.1		
	$I_{OL} = 12\ \text{mA}$	3 V			0.36		0.5	0.44		
		4.5 V			0.36		0.5	0.44		
	$I_{OL} = 24\ \text{mA}$	5.5 V			0.36		0.5	0.44		
		$I_{OL} = 50\ \text{mA}^\dagger$	5.5 V				1.65			
$I_{OL} = 75\ \text{mA}^\dagger$	5.5 V						1.65			
$I_I$	$V_I = V_{CC}$ or GND	5.5 V			$\pm 0.1$		$\pm 1$	$\pm 1$	$\mu\text{A}$	
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			2		80	20	$\mu\text{A}$	
$C_i$	$V_I = V_{CC}$ or GND	5 V		2.6					pF	

$^\dagger$  Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.



# SN54AC10, SN74AC10 TRIPLE 3-INPUT POSITIVE-NAND GATES

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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			SN54AC10		SN74AC10		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A, B, or C	Y	1.5	6	9.5	1	11	1	10.5	ns
$t_{PHL}$			1.5	5.5	8.5	1	10	1	10	

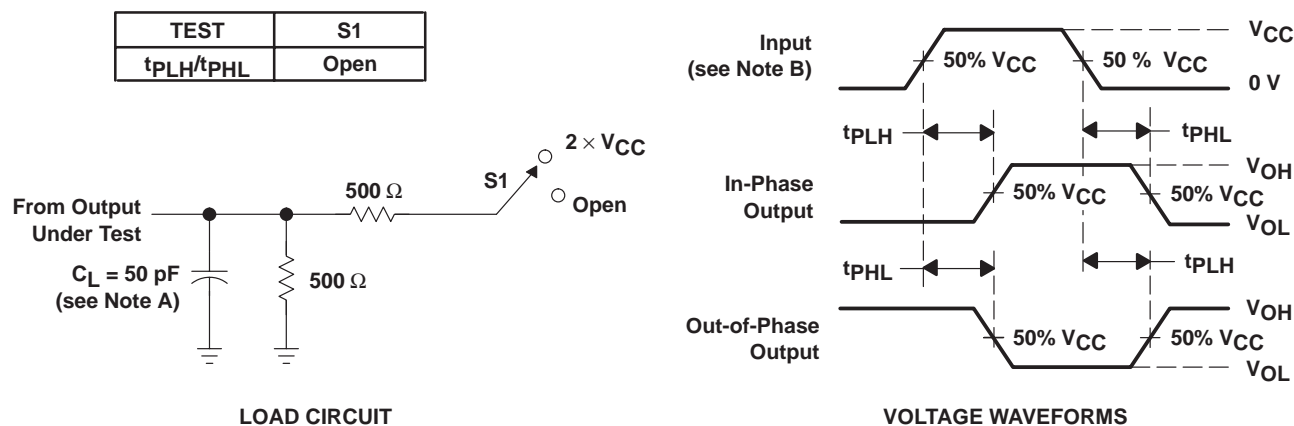
switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			SN54AC10		SN74AC10		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A, B, or C	Y	1.5	4.5	7	1	8.5	1	8	ns
$t_{PHL}$			1.5	4	6	1	7	1	6.5	

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	25	pF

## PARAMETER MEASUREMENT INFORMATION





- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .  
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-87610012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 87610012A SNJ54AC 10FK	<a href="#">Samples</a>
5962-8761001CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8761001CA SNJ54AC10J	<a href="#">Samples</a>
5962-8761001DA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8761001DA SNJ54AC10W	<a href="#">Samples</a>
SN74AC10D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC10	<a href="#">Samples</a>
SN74AC10DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC10	<a href="#">Samples</a>
SN74AC10DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC10	<a href="#">Samples</a>
SN74AC10DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC10	<a href="#">Samples</a>
SN74AC10DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC10	<a href="#">Samples</a>
SN74AC10DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC10	<a href="#">Samples</a>
SN74AC10DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC10	<a href="#">Samples</a>
SN74AC10N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74AC10N	<a href="#">Samples</a>
SN74AC10NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC10	<a href="#">Samples</a>
SN74AC10PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC10	<a href="#">Samples</a>
SN74AC10PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC10	<a href="#">Samples</a>
SNJ54AC10FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 87610012A SNJ54AC 10FK	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54AC10J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8761001CA SNJ54AC10J	
SNJ54AC10W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8761001DA SNJ54AC10W	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54AC10, SN74AC10 :**

- Catalog: [SN74AC10](#)
- Military: [SN54AC10](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC10DBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74AC10DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AC10NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AC10PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC10DBR	SSOP	DB	14	2000	367.0	367.0	38.0
SN74AC10DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74AC10NSR	SO	NS	14	2000	367.0	367.0	38.0
SN74AC10PWR	TSSOP	PW	14	2000	367.0	367.0	35.0

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14

J 14

**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

# J0014A



## PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

### NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

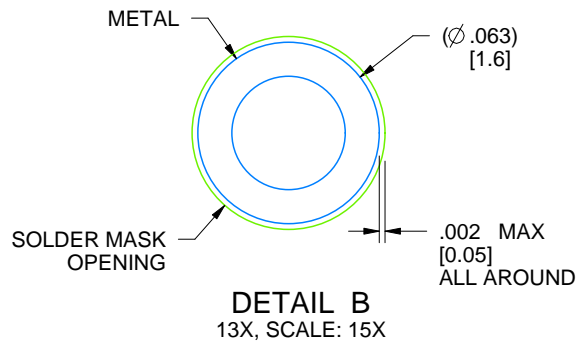
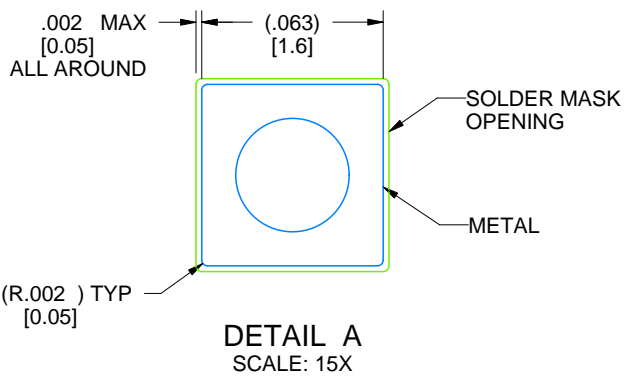
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



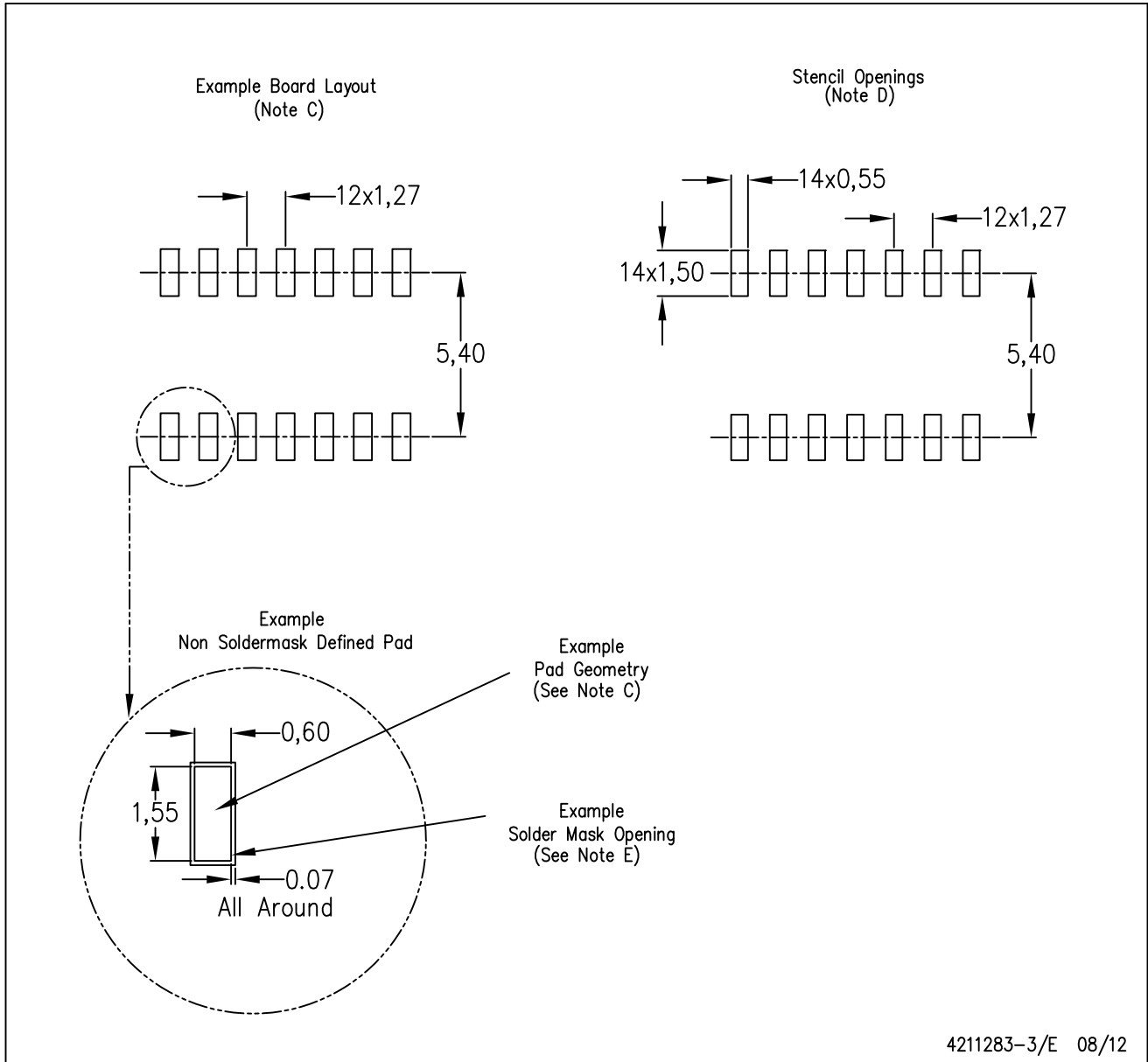
4214771/A 05/2017





D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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