A4955

Full-Bridge PWM Gate Driver

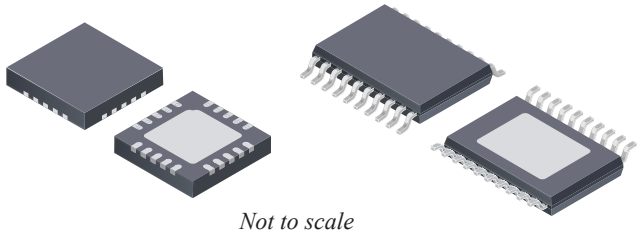
FEATURES AND BENEFITS

- Standard IN1/IN2 control logic
- Overcurrent indication
- Adjustable off-time and blank-time
- Adjustable current limit
- Adjustable gate drive
- Synchronous rectification
- Internal UVLO
- Crossover-current protection
- MOSFET VDS protection
- Voltage output proportional to load current

PACKAGES:

20-Pin QFN (suffix “ES”) with Exposed Thermal Pad

20-Pin eTSSOP (suffix “LP”) with Exposed Thermal Pad



Not to scale

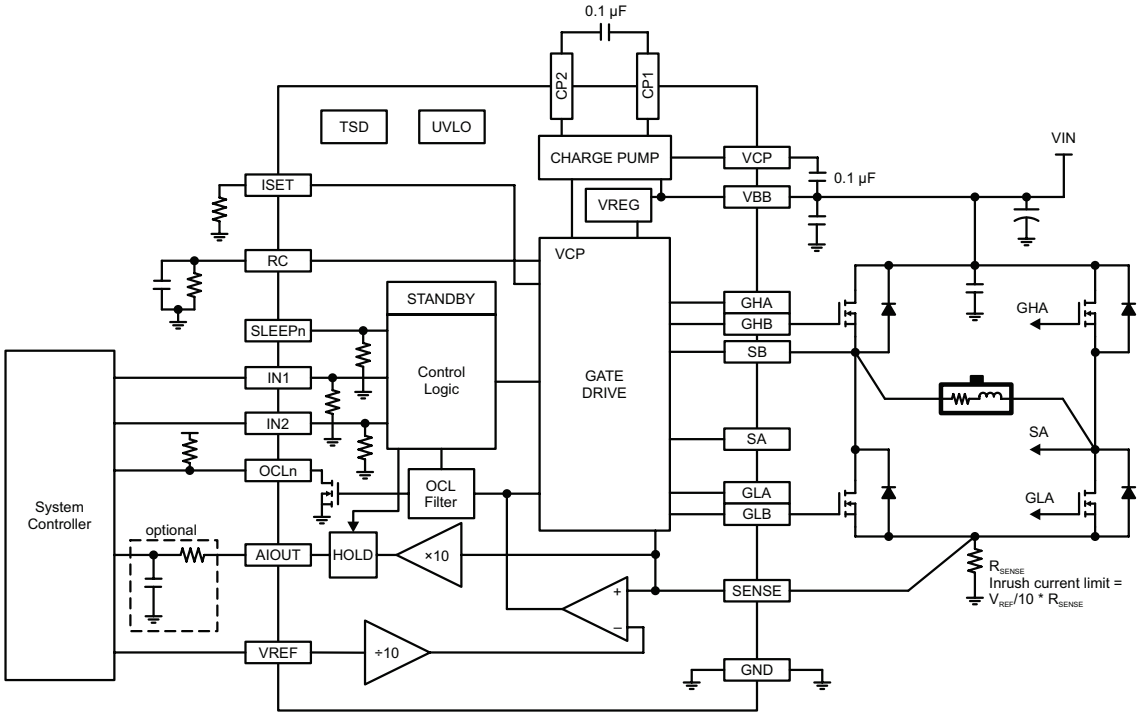
DESCRIPTION

Designed for pulse-width-modulated (PWM) control of DC motors, the A4955 is capable of 50 V operation and provides gate drive for an all N-channel external MOSFET bridge.

Input terminals are provided for use in controlling the speed and direction of a DC motor with externally applied PWM control signals. Internal synchronous rectification control circuitry is provided to lower power dissipation during PWM operation.

Internal circuit protection includes VDS protection, thermal shutdown with hysteresis, undervoltage monitoring of VBB, and crossover-current protection.

The A4955 is supplied in a low-profile 4 × 4 mm, 20-contact QFN package (suffix “ES”) and a 20-lead eTSSOP (suffix “LP”), both with exposed thermal pad.



Functional Block Diagram

SPECIFICATIONS

SELECTION GUIDE

Part Number	Ambient Temperature Range	Packing	Notes
A4955GESTR-T	–40°C to 105°C	1500 pieces per 7-inch reel	
A4955GLPTR-T	–40°C to 105°C	4000 pieces per 13-inch reel	
~~A4955KLPTR-T~~ [1]	–40°C to 125°C	4000 pieces per 13-inch reel	AEC-Q100 Qualified

[1] The A4955KLPTR-T variant is in production but have been determined to be NOT FOR NEW DESIGN. This classification indicates that sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because obsolescence in the near future is probable. Samples are no longer available. Date of status change: July 1, 2019.

ABSOLUTE MAXIMUM RATINGS

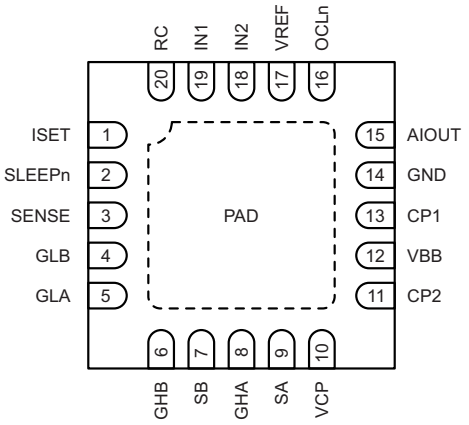
Characteristic	Symbol	Notes	Rating	Unit
Load Supply Voltage	V_{BB}		50	V
Motor Outputs	V_{Sx}	$V_{Sx} – V_{SENSE}$; $V_{BB} – V_{Sx}$	–2 to 52	V
SENSE	V_{SENSE}		–0.5 to 0.5	V
		t_W < 500 ns	–4 to 4	V
OCLn	V_{OCLn}		–0.3 to 5.5	V
VREF	V_{REF}		–0.3 to 5.5	V
ISET	V_{ISET}		–0.3 to 5.5	V
AIOUT	V_{AIOUT}		–0.3 to 5.5	V
Logic Input Voltage Range	V_{IN}	SLEEPn, IN1, IN2	–0.3 to 5.5	V
Junction Temperature	T_J		150	°C
Storage Temperature Range	T_S		–55 to 150	°C
Operating Temperature Range	T_A	Range G	–40 to 105	°C
		Range K	–40 to 125	°C

THERMAL CHARACTERISTICS (may require derating at maximum conditions; see application information)

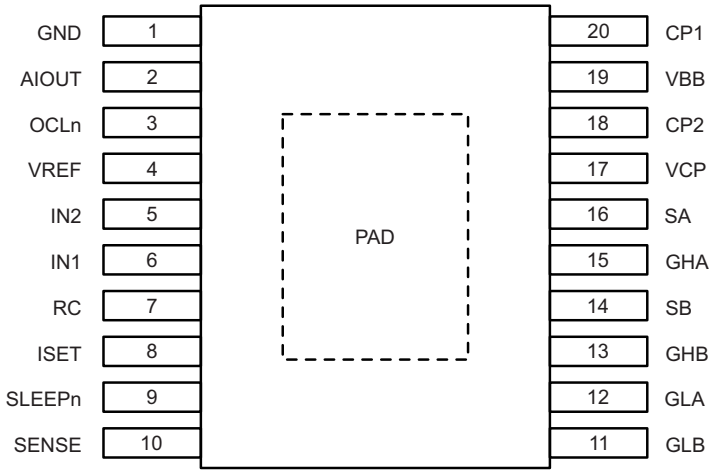
Characteristic	Symbol	Test Conditions*	Value	Unit
ES Package	$R_{\theta JA}$	4-Layer PCB, 1 in.^{2} copper	37	°C/W
LP Package		4-Layer PCB, 1 in.^{2} copper	28	°C/W

*Power dissipation and thermal limits must be observed.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com



Package ES, 20-Pin QFN Pinouts



Package LP, 20-Pin eTSSOP Pinouts

Terminal List Table

Name	Number		Function
	ES Package	LP Package	
ISET	1	8	Terminal to set gate drive current
SLEEPn	2	9	Sleep input, active low
SENSE	3	10	Sense resistor connection, low-side gate return
GLB	4	11	Gate driver
GLA	5	12	Gate driver
GHB	6	13	Gate driver
SB	7	14	High-side bridge reference
GHA	8	15	Gate driver
SA	9	16	High-side bridge reference
VCP	10	17	Charge pump reservoir cap connection
CP2	11	18	Charge pump terminal
VBB	12	19	Supply voltage
CP1	13	20	Charge pump terminal
GND	14	1	Ground
AIOUT	15	2	Analog output proportional to V_{SENSE}
OCLn	16	3	OCP and OVP output flag, open drain
VREF	17	4	Analog OCP reference input
IN2	18	5	Digital IN2 input
IN1	19	6	Digital IN1 input
RC	20	7	Terminal to set blank- and off-time
PAD	–	–	

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS: Valid for Temperature Range G version at T_J = 25°C and for Temperature Range K version at T_J = –40°C to 150°C, V_{BB} = 5.5 to 50 V, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VBB Supply Current	I_{BB}		–	6	10	mA
	I_{BB}	SLEEPn = low, Standby Mode	–	–	5	µA
GATE DRIVE						
High-Side Gate Drive Output	V_{GH}	Relative to V_{BB}, I_{GATE} = 200 µA, V_{BB} = 8 to 50 V	6.5	6.8	7.5	V
		Relative to V_{BB}, I_{GATE} = 200 µA, V_{BB} = 5.5 V	–	5.2	–	V
Low-Side Gate Drive Output	V_{GL}	I_{GATE} = 200 µA, V_{BB} = 8 to 50 V	6.5	6.8	7.5	V
		I_{GATE} = 200 µA, V_{BB} = 5.5 V	–	5.4	–	V
Gate Drive Pull-Up Current	I_{GPU}	R_{ISET} = 30 kΩ; V_{GH} = V_{GL} = 4 V	21	30	39	mA
Gate Drive Pull-Down Current	I_{GPD}	R_{ISET} = 30 kΩ; V_{GH} = V_{GL} = 4 V	47	68	89	mA
Dead-Time	t_{DT}		–	1000	–	ns
Passive Pull-Down Resistance	R_{GPD}		30	50	70	kΩ
LOGIC INPUT AND OUTPUT						
Logic Output Voltage	V_{OCLn}	I = 2 mA, overcurrent detected	–	0.2	0.3	V
Logic Output Leakage	I_{OCLn}	V = 5 V, normal operation	–	–	5	µA
PWM Current Limit Flag Timer	t_{OCLn}		300	500	600	µs
Logic Input Voltage	V_{IH}		2.0	–	–	V
	V_{IL}		–	–	0.8	V
	$V_{IL(SLEEPn)}$	SLEEPn input	–	–	0.4	V
Logic Input Hysteresis	V_{HYS}		–	320	–	mV
Logic Input Pull-Down Resistor	R_{PD}		30	50	70	kΩ
VREF Input Current	I_{VREF}	V_{REF} = 2.5 V	–5	<1	5	µA
VREF Input Range	V_{REF}		0	–	2.5	V
Current Gain	A_V	V_{REF} / V_{SENSE}, V_{REF} = 2.5 V	9.5	–	10.5	V/V
Input Offset, SENSE	$V_{OSSENSE}$		–10	–	10	mV
Fixed Off-Time	t_{OFF}	R_{RC} = 30 kΩ, C_{RC} = 1 nF	–	30	–	µs
Percent Fast Decay	P_{FD}	Internal PWM chop	–	13	–	%
Blank-Time	t_{BLK}	R_{RC} = 30 kΩ, C_{RC} = 1 nF	2.1	3	3.9	µs
Power-Up Delay	t_{pu}	Time until outputs are enabled	–	50	300	µs
AIOUT Gain	A_{IOUT}	AIOUT/V_{SENSE}, V_{SENSE} = 50 to 200 mV	9	10	11	V/V
Input Offset, AIOUT	$V_{OSAIOUT}$		–15	–	15	mV
Sample-and-Hold Accuracy	$V_{SH(ACC)}$		–	15	–	mV
Sample-and-Hold Droop Rate	V_{DROOP}		–	–	1	mV/µs
AIOUT Output Impedance	$R_{OUT(AIOUT)}$		0.75	1.00	1.45	kΩ
PROTECTION CIRCUITS						
UVLO Enable Threshold	$V_{BB(UVLO)}$	V_{BB} rising	5.10	5.25	5.40	V
UVLO Hysteresis	$V_{BB(UVLO,HYS)}$		200	300	350	mV
VDS Threshold	V_{DSTH}		–	2	–	V
Thermal Shutdown Temperature	T_{JTSD}	Temperature increasing	150	165	185	°C
Thermal Shutdown Hysteresis	ΔT_J	Recovery = $T_{JTSD} - \Delta T_J$	–	30	–	°C

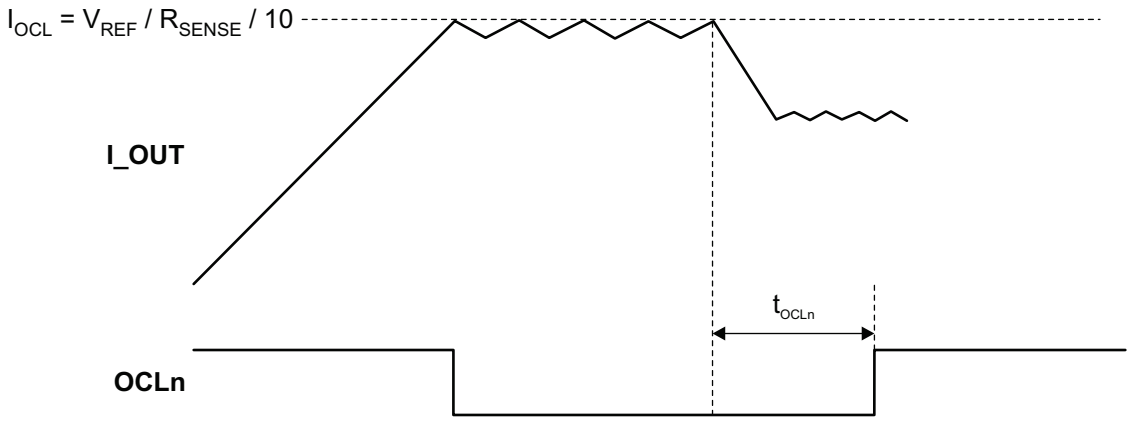
[1] Specified limits are tested at a single temperature and assured over operating temperature range by design and characterization.
[2] Target trip level = V_{DSTH} = V_{DRAIN} – V_{Sx} (High Side On) or V_{DSTH} = V_{Sx} – V_{SENSE} (Low Side On).

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Control Logic

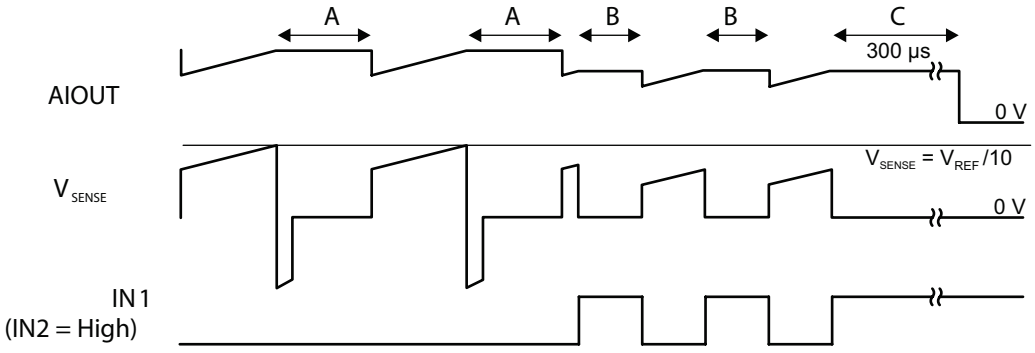
IN1	IN2	SLEEPn	10 × V_{SENSE} > V_{REF}	OUTA	OUTB	Function
x	x	0	x	Z	Z	Sleep (Standby) Mode
0	0	1	x	Z	Z	Coast
0	1	1	false	L	H	Reverse
1	0	1	false	H	L	Forward
1	1	1	x	L	L	Slow Decay SR (Brake)
0	1	1	true	H/L	L	Internal Chop Reverse, Mixed Decay *
1	0	1	true	L	H/L	Internal Chop Forward, Mixed Decay *

* In fast decay, outputs change to high-Z state when load current approaches zero, to prevent reversal of current.



OCLn Output Flag

OCLn output function is described in the Functional Description section.



AIOUT Output

A. Internal OCL chop. AIOUT holds while SENSE voltage varies during the mixed-decay off-time.

B. INx chop. AIOUT holds while SENSE voltage drops to 0 V during slow decay.

C. Slow-decay timeout. AIOUT is forced to 0 V 300 µs after ENABLE goes low.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

FUNCTIONAL DESCRIPTION

Device Operation

The A4955 is designed to operate DC motors. The output drivers are capable of 50 V with gate-driver capability for an all N-channel external MOSFET H-bridge. Control logic includes synchronous rectification to reduce power dissipation. Current limit is regulated by fixed off-time pulse-width-modulated (PWM) control circuitry.

Internal PWM Current Control

Peak current is regulated by monitoring the voltage on an external sense resistor.

$$I_{PEAK} = \frac{V_{REF}}{(10 \times R_{SENSE})}$$

When the peak current is exceeded, the source driver turns off for a fixed period t_{OFF} to chop the current. The outputs operate in mixed-decay mode during t_{OFF}. Refer to the Fixed Off-Time Setting section to set t_{OFF}.

The internal current-sense circuit is ignored for t_{BLANK} after PWM transitions. The comparator output is blanked to prevent false overcurrent detection due to reverse recovery currents of the clamp diodes, or switching transients related to the capacitance of the load, or both. Refer to the Blank-Time Setting section to set t_{BLANK}.

Brake

It is important to note that the internal PWM current-control circuit will not limit the current when braking, since the current does not flow through the sense resistor. The maximum current can be approximated by V_{BEMF} / R_{MOTOR}. Care should be taken to ensure that the maximum ratings of the external MOSFET are not exceeded in worst-case braking situations of high speed and high inertial loads.

ISET

A resistor from ISET terminal to ground sets the magnitude of the gate current. The sink and source current ratios are fixed at approximately 2-to-1 where the pull-down current is approximately two times the pull-up current. R_{ISET} should be between 15 and 150 kΩ.

The formula for determining the gate drive is:

$$I_{GATE\_HS}\,(mA) = 1.9 + \frac{900}{R_{ISET}\,(k\Omega)}$$

$$I_{GATE\_LS}\,(mA) = 3.5 + \frac{1700}{R_{ISET}\,(k\Omega)}$$

RC

The RC terminal is used to set both fixed off-time and blank-time for the internal PWM current control. Refer to the following three sections to select RC component values.

Fixed Off-Time Setting

The internal PWM current-control circuitry uses a one-shot to control the time the drivers remain off. The one-shot off-time (t_{OFF}) is determined by the selection of an external resistor and capacitor connected from the RC timing terminal to ground. The off-time, over a range of values of C_{RC} = 470 to 1500 pF and R_{RC} = 12 to 100 kΩ, is approximated by:

$$t_{OFF} = R_{RC} \times C_{RC} + dead\ time$$

Blank-Time Setting

This circuit blanks the output of the current-sense comparator when the outputs are switched by the internal current-control circuitry or by an external PWM chop command. The comparator blanking time, t_{BLANK}, is determined by the selection of an external resistor and capacitor connected from the RC timing terminal to ground, and is approximated by:

$$t_{BLANK} = 2.6\ \mu s \times C_{RC}\,(nF) \times e^{(3.6/R_{RC}(k\Omega))}$$

Slow Decay

In slow-decay mode, the low-side switch stays on and the high-side switch turns off. Due to the synchronous rectification feature, the complementary low-side switch turns on after a dead-time.

Fast Decay SR

In fast-decay mode, the high-side and low-side switches turn off, and the complementary pair of switches is turned on, effectively reversing the voltage polarity across the motor winding.

ALLEGRO microsystems
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Mixed Decay

When the peak current is reached, as set by the sense resistor and voltage on VREF, the PWM current limiter initiates an off-time. The off-time is determined by the resistor and capacitor on the RC terminal. In mixed-decay mode, the driver will initiate a fast decay, after a dead-time, for 13% of the programmed off-time. After the fast-decay time expires, the bridge will switch to slow decay for the remaining off-time. When the bridge is operating in fast decay, it will internally prevent current reversal by putting the bridge in a high-Z state if the current through the sense resistor falls close to zero.

OCLn Output

An open-drain logic output will be driven low to indicate system operation. The OCLn terminal is driven low under two conditions:

1. When the system is limiting current to value set by V_{REF} and R_{SENSE}. Once overcurrent events are no longer detected, the A4955 will release the indication after a time t_{OCLn}.
2. When a VDS fault is detected, the OCLn terminal is driven low. It is released when the fault is reset.

The OCLn terminal, in combination with the AIOUT terminal, can provide valuable information about how the system is behaving:

- Overcurrent events can indicate a motor stall condition, in which case the system controller can respond to the fault condition by reducing PWM duty. When OCLn is low and the voltage on AIOUT is greater than 0 V, the controller is actively limiting current with the internal, fixed off-time PWM current limiter.
- In the case of a VDS fault, the OCLn terminal is also driven low, but the AIOUT voltage will be 0 V, because the bridge has been disabled. This notifies the user that a VDS fault has occurred and the driver has been disabled.

AIOUT

An analog output can be used to monitor current through the external sense resistor (if used). The SENSE voltage is gained by a factor of 10 and fed to the AIOUT terminal. A sample-and-hold circuit is used to capture the voltage across the sense resistor and holds it during periods when the voltage is not representative of the current in the motor. The AIOUT Output diagram illustrates when the voltage is held. The held voltage will droop at a rate equal to V_{DROOP}. In the case of a VDS fault on the bridge, the AIOUT terminal will be discharged to zero volts.

Charge Pump

The charge pump is used to generate a supply above V_{BB} to drive the high-side MOSFETs. The VCP voltage is internally monitored and, in the case of a fault condition, the outputs of the device are disabled.

MOSFET VDS Protection

The drain-to-source voltage is monitored across the MOSFET any time the MOSFET is on. If the voltage across the MOSFET exceeds V_{DSTH}, the bridge is disabled and latched off.

In order to prevent false VDS faults, the VDS monitor is blanked immediately after any MOSFET is turned on. The VDS monitor waits for a blank-time defined by the components on the RC terminal before monitoring the VDS level. During the off-time when SR is active, VDS blanking is fixed at 1 µs.

VDS Fault

When a VDS fault occurs, and the bridge is disabled, and the fault is latched, the OCLn terminal is immediately driven low. The latch can only be reset by going into standby or by dropping V_{BB} below the UVLO threshold.

Standby Mode

Low power standby mode is activated when SLEEPn is brought low. Standby mode disables most of the internal circuitry, including the charge pump and internal regulator. When coming out of standby mode, the A4955 requires up to 300 µs before the outputs can respond to input commands.

TSD

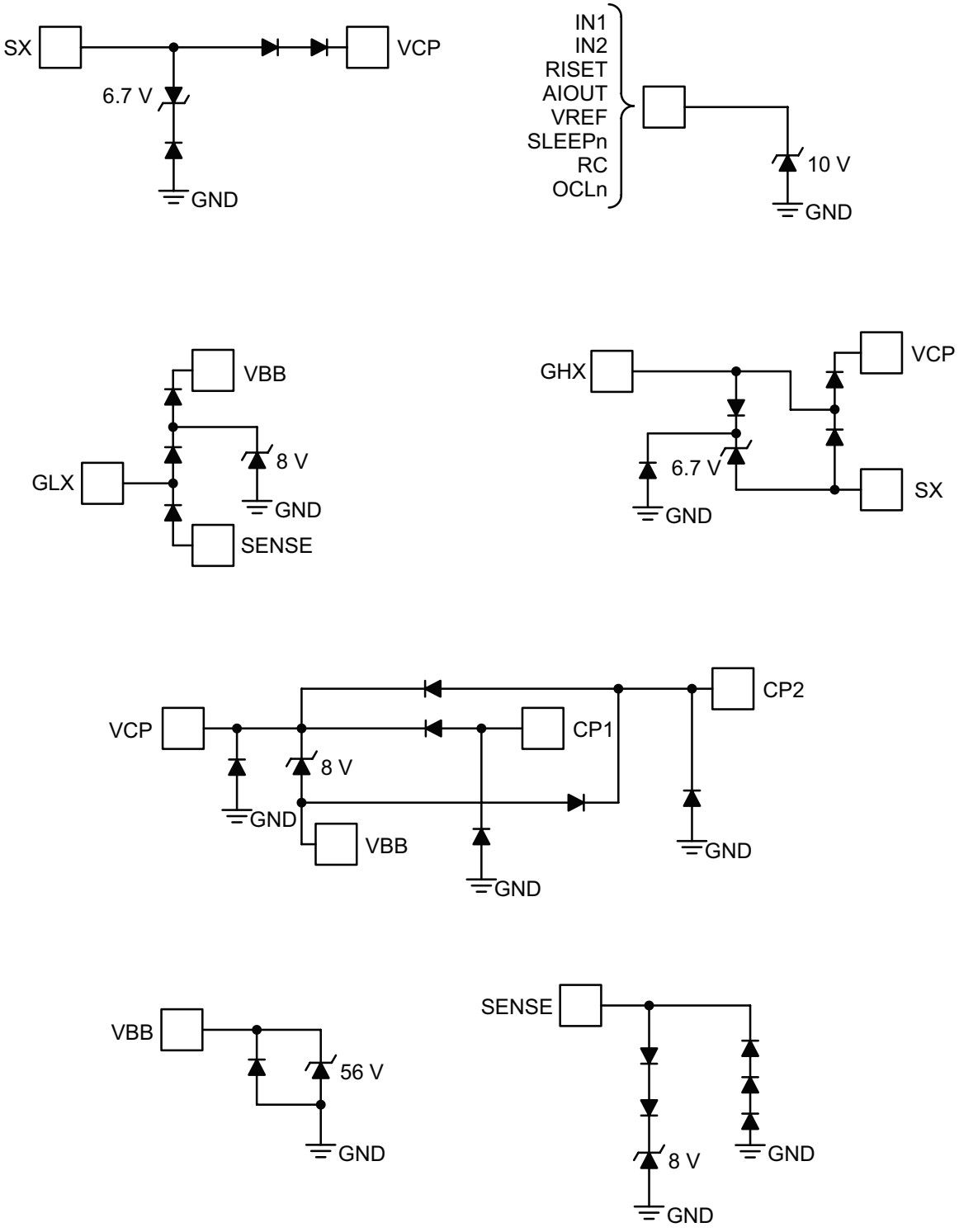
If the die temperature increases to approximately T_{TSD}, the full bridge outputs will be disabled until the internal temperature falls below T_{TSD} minus a hysteresis level of T_{HYS}.

Fault Shutdown

In the event of a fault due to excessive junction temperature, or low voltage on VCP or VBB, the outputs of the device are disabled until the fault condition is removed. At power-up, the UVLO circuit disables the drivers until the UVLO thresholds are exceeded.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

TERMINAL CIRCUIT DIAGRAMS

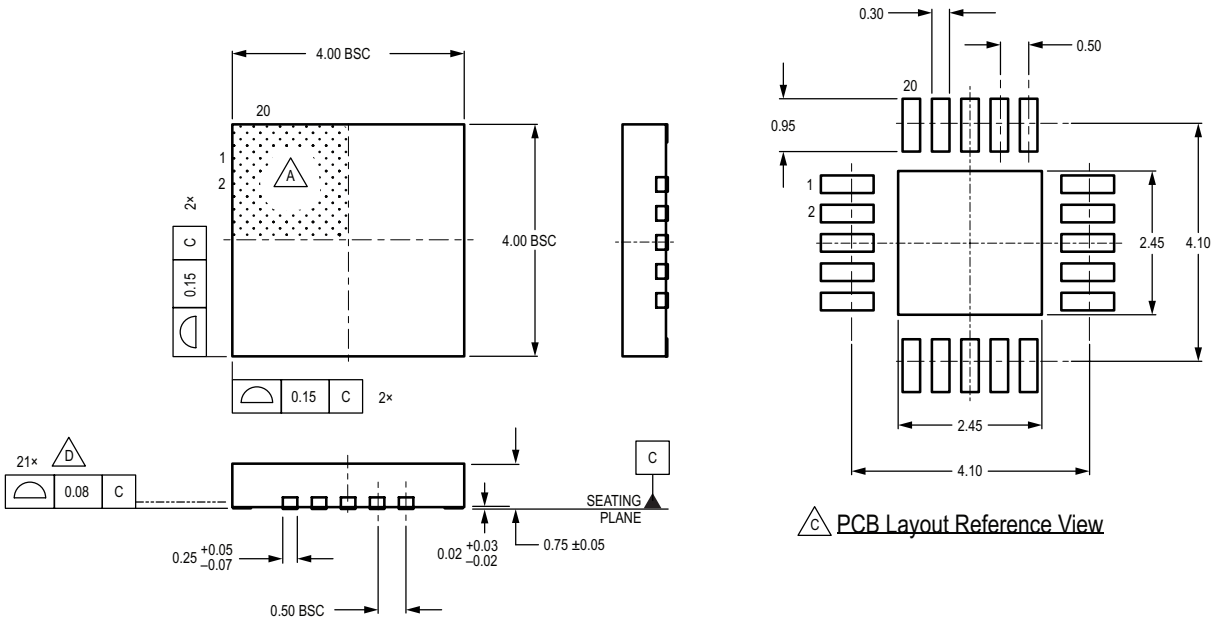


Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PACKAGE OUTLINE DRAWINGS

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000222 Rev. 4 or JEDEC MO-220WGGD)
Dimensions in millimeters – NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P400X400X80-21BM); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

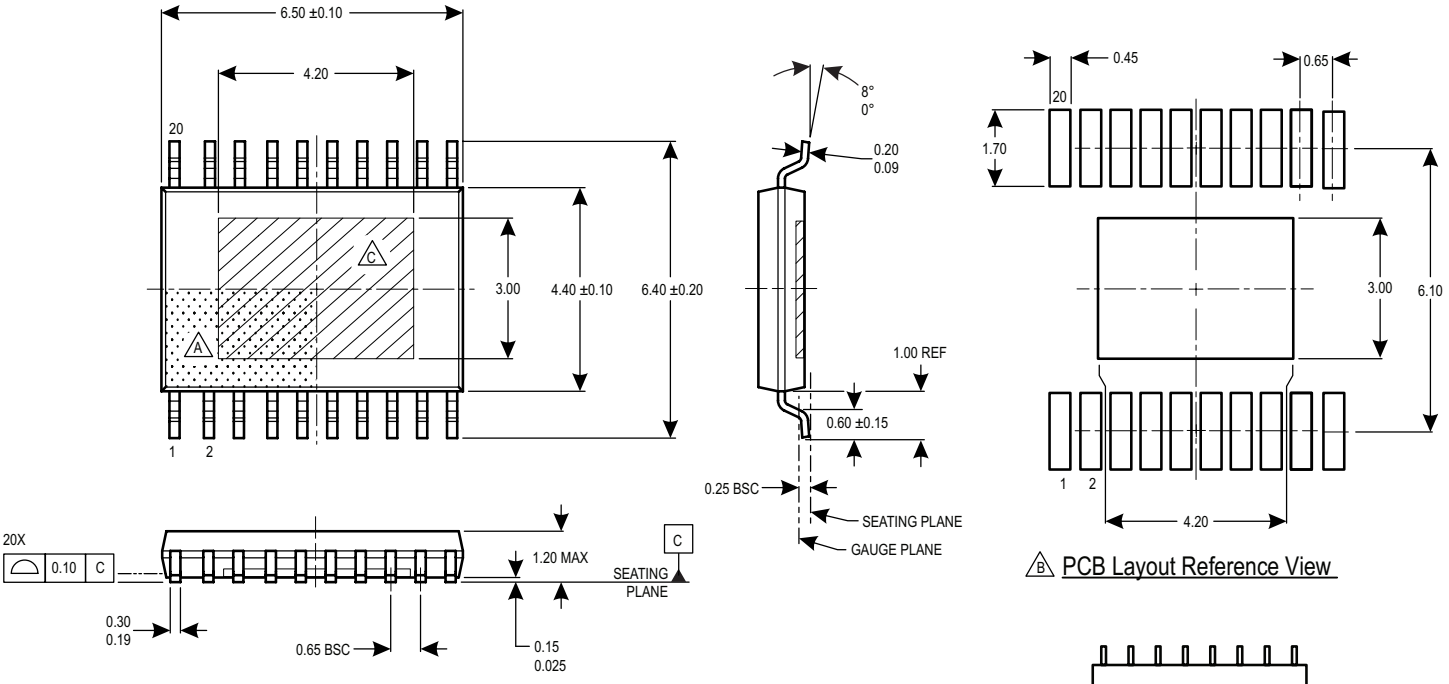
E Branding scale and appearance at supplier discretion.

ES Package, 20-Pin QFN with Exposed Thermal Pad

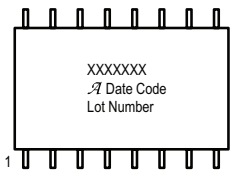
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

For Reference Only – Not for Tooling Use

(Reference JEDEC MO-153ACT; Allegro DWG-0000379, Rev. 3)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



B PCB Layout Reference View



D Standard Branding Reference View

Line 1: Part Number
Line 2: Logo A, 4 digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 SOP65P640X110-21M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

C Exposed thermal pad (bottom surface)

D Branding scale and appearance at supplier discretion

LP Package, 20-Pin eTSSOP with Exposed Thermal Pad

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Revision History

Revision	Revision Date	Description of Revision
–	February 12, 2015	Initial Release
1	July 14, 2015	Updated functional block diagram (page 1); added packing information (page 2); changed references to LSS to SENSE
2	November 30, 2017	Updated ISET section (page 6)
3	January 11, 2019	Minor editorial updates
4	July 1, 2019	Updated A4955KLPTR-T product variant status to Not for New Design
5	July 18, 2022	Updated package drawings (pages 9-10)

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com