

## SN75ALS191 Dual Differential Line Driver

### 1 Features

- Meets or exceeds the requirements of ANSI standard EIA/TIA-422-B and ITU recommendation V.11
- Designed to operate at 20 Mbaud or higher
- TTL- and CMOS-input compatibility
- Single 5V supply operation
- Output short-circuit protection
- Improved replacement for the  $\mu$ A9638

### 2 Applications

- [Factory automation](#)
- ATM and cash counters
- [Smart grid](#)
- AC and [servo motor drives](#)

### 3 Description

The SN75ALS191 is a dual, high-speed, differential line driver designed to meet ANSI Standard EIA/TIA-422-B and ITU Recommendation V.11. The inputs are TTL- and CMOS-compatible and have input clamp diodes. Schottky-diode-clamped transistors minimize propagation delay time. This device operates from a single 5V power supply and is supplied in eight-pin packages.

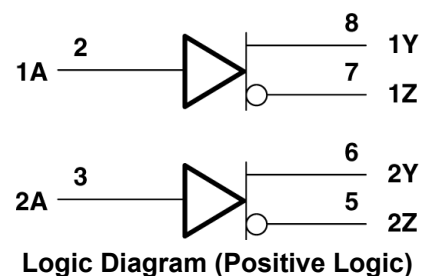
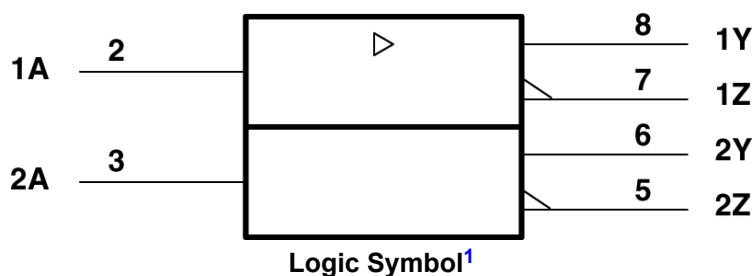
The SN75ALS191 is characterized for operation from 0°C to 70°C.

#### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
SN75ALS191	P (PDIP, 8)	9.81mm × 9.43mm
	D (SOIC, 8)	4.9mm × 6mm
	PS (SOP, 8)	6.2mm × 7.8mm

(1) For more information, see [Section 10](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



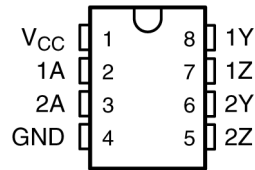
<sup>1</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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## 4 Pin Configuration and Functions



**Figure 4-1. D or P Package  
(Top View)**

**Table 4-1. Pin Functions**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
1Z	7	O	Inverting Output of Differential Driver on Channel 1
1Y	8	O	Non-Inverting Output for Differential Driver on Channel 1
1A	2	I	Single Ended Data Input for Channel 1
GND	4	GND	Device Ground
2A	3	I	Single Ended Data Input for Channel 2
2Y	6	O	Non-Inverting Output for Differential Driver on Channel 2
2Z	5	O	Inverting Output of Differential Driver on Channel 2
V <sub>CC</sub>	1	P	5V Power Supply Positive Terminal Connection

(1) Signal Types: I = Input, O = Output, I/O = Input or Output, P = Power, GND = Ground.

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage, see <sup>(2)</sup>		7	V
V <sub>I</sub>	Input voltage		7	V
	Continuous total dissipation	See <i>Dissipation Rating</i> table		
T <sub>A</sub>	Operating free-air temperature range	0	70	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values except differential output voltage (V<sub>OD</sub>) are with respect to network ground terminal.

### 5.2 Dissipation Rating

PACKAGE	T <sub>A</sub> ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 70°C POWER RATING
D	725mW	5.8mW/°C	464mW
P	1000mW	8mW/°C	640mW

### 5.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V <sub>CC</sub>	4.75	5	5.25	V
High-level input voltage, V <sub>IH</sub>	2			V
Low-level input voltage, V <sub>IL</sub>			0.8	V
High-level output current, I <sub>OH</sub>			-50	mA
Low-level output current, I <sub>OL</sub>			50	mA
Operating free-air temperature, T <sub>A</sub>	0		70	°C

### 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		D	P	PS	UNIT
		8-Pins			
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	116.7	84.3	89.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	56.3	65.4	46.2	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	63.4	62.1	50.7	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	8.8	31.3	23.5	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	62.6	60.4	60.3	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

## 5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP <sup>(1)</sup>	MAX	UNIT								
$V_{IK}$	Input clamp voltage	$V_{CC} = 4.75V$ ,	$I_I = -18mA$			-1	-1.2	V								
$V_{OH}$	High-level output voltage	$V_{CC} = 4.75V$ ,	$V_{IH} = 2V$ ,	$I_{OH} = -10mA$	2.5	3.3		V								
		$V_{IL} = 0.8V$			2											
$V_{OL}$	Low-level output voltage	$V_{CC} = 4.75V$ , $I_{OL} = 40mA$	$V_{IH} = 2V$ ,	$V_{IL} = 0.8V$ ,			0.5	V								
$ V_{OD1} $	Differential output voltage	$V_{CC} = 5.25V$ ,	$I_O = 0$				$2 V_{OD2}$	V								
$ V_{OD2} $	Differential output voltage	$V_{CC} = 4.75V$ to $5.25V$ , See <a href="#">Figure 6-1</a>			2			V								
$\Delta V_{OD} $	Change in magnitude of differential output voltage <sup>(2)</sup>								$\pm 0.4$	V						
$V_{OC}$	Common-mode output voltage <sup>(3)</sup>								3	V						
$\Delta V_{OC} $	Change in magnitude of common-mode output voltage <sup>(2)</sup>							V								
									$I_O$	Output current with power off	$V_{CC} = 0$		$V_O = 6V$	0.1	100	$\mu A$
													$V_O = -0.25V$	-0.1	-100	
					$V_O = -0.25V$ to $6V$		$\pm 100$									
$I_I$	Input current	$V_{CC} = 5.25V$ ,	$V_I = 5.5V$				50	$\mu A$								
$I_{IH}$	High-level input current	$V_{CC} = 5.25V$ ,	$V_I = 2.7V$				25	$\mu A$								
$I_{IL}$	Low-level input current	$V_{CC} = 5.25V$ ,	$V_I = 0.5V$				200	$\mu A$								
$I_{OS}$	Short-circuit output current <sup>(4)</sup>	$V_{CC} = 5.25V$ ,	$V_O = 0$			-50	-150	mA								
$I_{CC}$	Supply current (all drivers)	$V_{CC} = 5.25V$ ,	No load,	All inputs at 0V		32	40	mA								

- (1) All typical values are at  $V_{CC} = 5V$  and  $T_A = 25^\circ C$ .
- (2)  $|V_{OD}|$  and  $|V_{OC}|$  are the changes in magnitude of  $V_{OD}$  and  $V_{OC}$ , respectively, that occur when the input is changed from a high level to a low level.
- (3) In ANSI Standard EIA/TIA-422-B,  $V_{OC}$ , which is the average of the two output voltages with respect to ground, is called output offset voltage,  $V_{OS}$ .
- (4) Only one output at a time should be shorted, and duration of the short circuit should not exceed one second.

## 5.6 Switching Characteristics

over recommended operating free-air temperature range,  $V_{CC} = 5V$

PARAMETER		TEST CONDITIONS			MIN	TYP <sup>(1)</sup>	MAX	UNIT
$t_{d(OD)}$	Differential-output delay time	$C_L = 15pF$ ,	$R_L = 100\Omega$ ,	See <a href="#">Figure 6-2</a>		3.5	7	ns
$t_{t(OD)}$	Differential-output transition time					3.5	7	ns
	Skew					1.5	4	ns

- (1) Typical values are at  $T_A = 25^\circ C$ .

## 6 Parameter Measurement Information

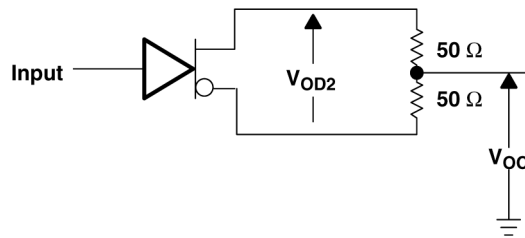
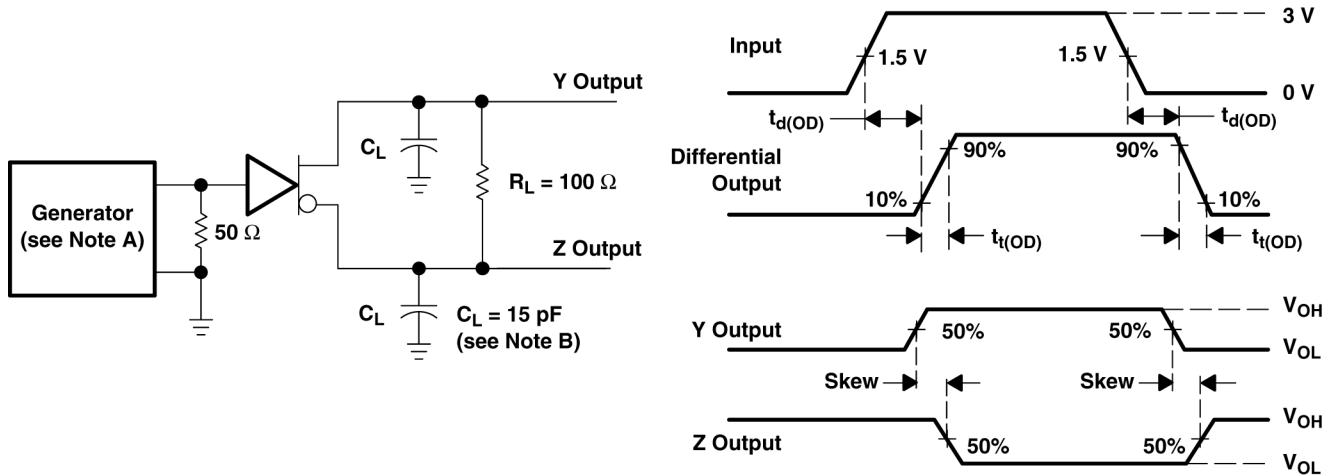


Figure 6-1. Differential and Common-Mode Output Voltages



**TEST CIRCUIT**

**VOLTAGE WAVEFORMS**

- A. The input pulse generator has the following characteristics:  $Z_O = 50\Omega$ ,  $PRR \leq 500\text{kHz}$ ,  $t_w = 100\text{ns}$ ,  $t_r = \leq 5\text{ns}$ .
- B.  $C_L$  includes probe and jig capacitance.

Figure 6-2. Test Circuit and Voltage Waveforms

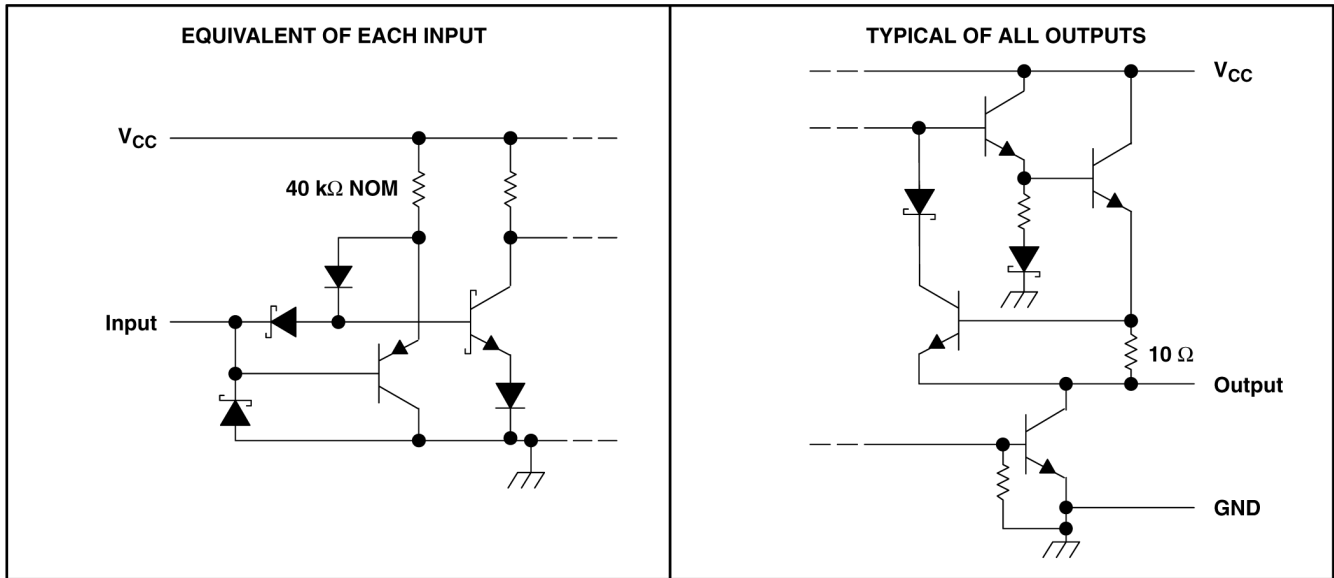
## 7 Detailed Description

### 7.1 Device Functional Modes

**Table 7-1. Function Table (Each Driver)**

INPUTS A <sup>(1)</sup>	OUTPUTS	
	Y	Z
H	H	L
L	L	H

(1) H = high level, L = low level, Z = high impedance



**Figure 7-1. Schematics of Inputs and Outputs**

## 8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 8.3 Trademarks

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### 8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision B (May 1995) to Revision C (March 2024)</b>	<b>Page</b>
• Changed the numbering format for tables, figures, and cross-references throughout the document.....	<b>1</b>

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75ALS191D	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	0 to 70	75A191	
SN75ALS191DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75A191	Samples
SN75ALS191P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	75ALS191	Samples
SN75ALS191PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	75ALS191	Samples
SN75ALS191PSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	V191	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS191DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75ALS191DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75ALS191PSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN75ALS191PSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS191DR	SOIC	D	8	2500	340.5	336.1	25.0
SN75ALS191DR	SOIC	D	8	2500	353.0	353.0	32.0
SN75ALS191PSR	SO	PS	8	2000	356.0	356.0	35.0
SN75ALS191PSR	SO	PS	8	2000	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN75ALS191P	P	PDIP	8	50	506	13.97	11230	4.32
SN75ALS191PE4	P	PDIP	8	50	506	13.97	11230	4.32



# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



# MECHANICAL DATA

PS (R-PDSO-G8)

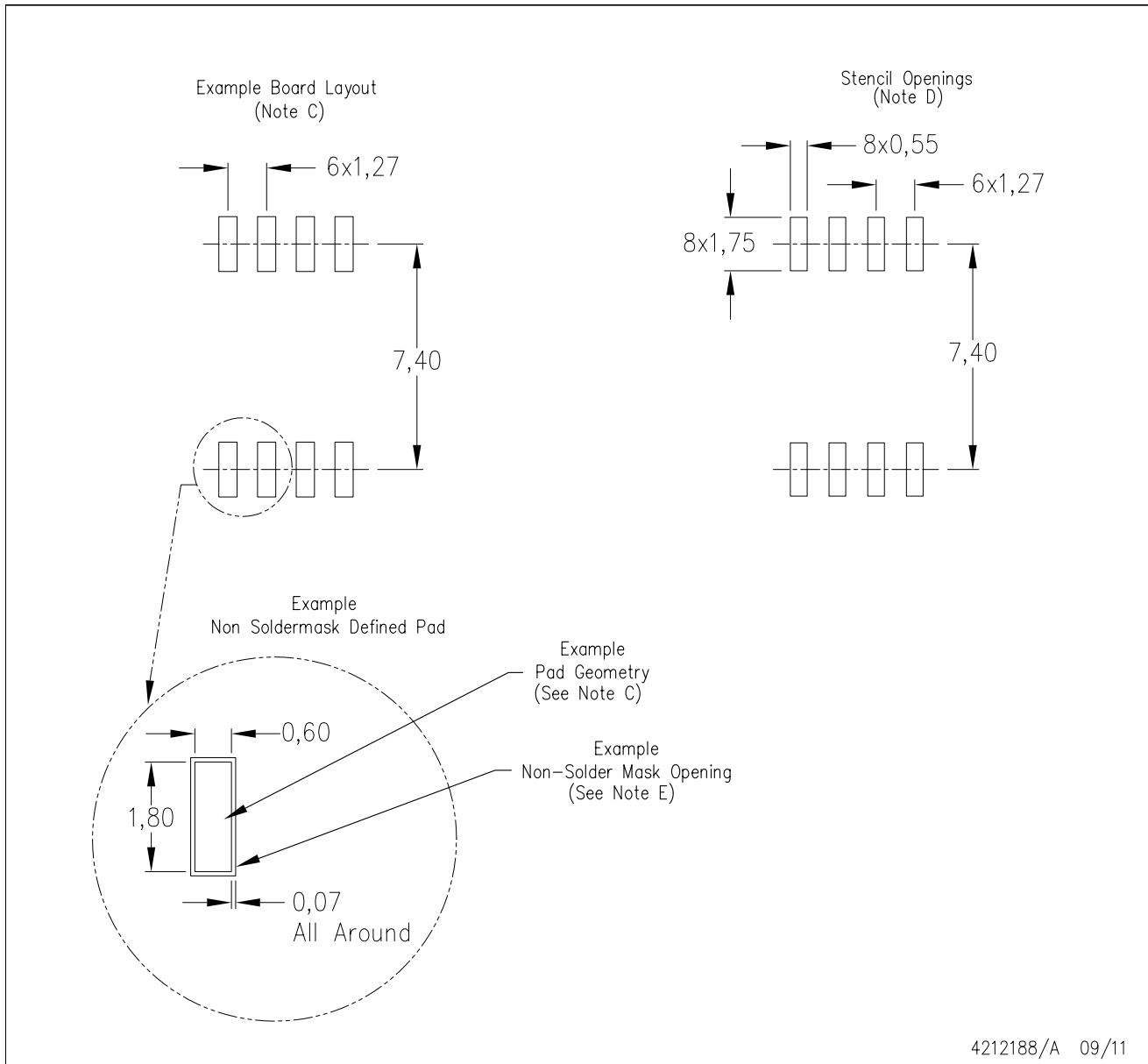
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

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