Data Sheet

BIT3193

High Performance PWM Controller

Preliminary
Version: 0.03

Notice

All information contained in this document is subject to change without notice.

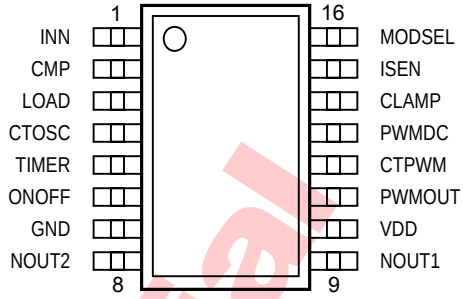
Features:

- 4.5V ~ 8V operation
- Fixed High Frequency, Voltage Mode PWM Control Topology
- Latched Off Protection
- Build-In Low Frequency PWM Generator
- Build-In UVLO
- Low Power CMOS Process
- Totem Pole Output
- 16 Pin Package

Applications:

- DC/DC Converters
- LCD TV
- LCD Monitor
- Notebook Computer
- Tablet PC
- Personal Digital Assistants
- Navigation Devices (GPS Equipment)
- Video Phone/ Door Phone
- Portable consumer product

Pin Layout:



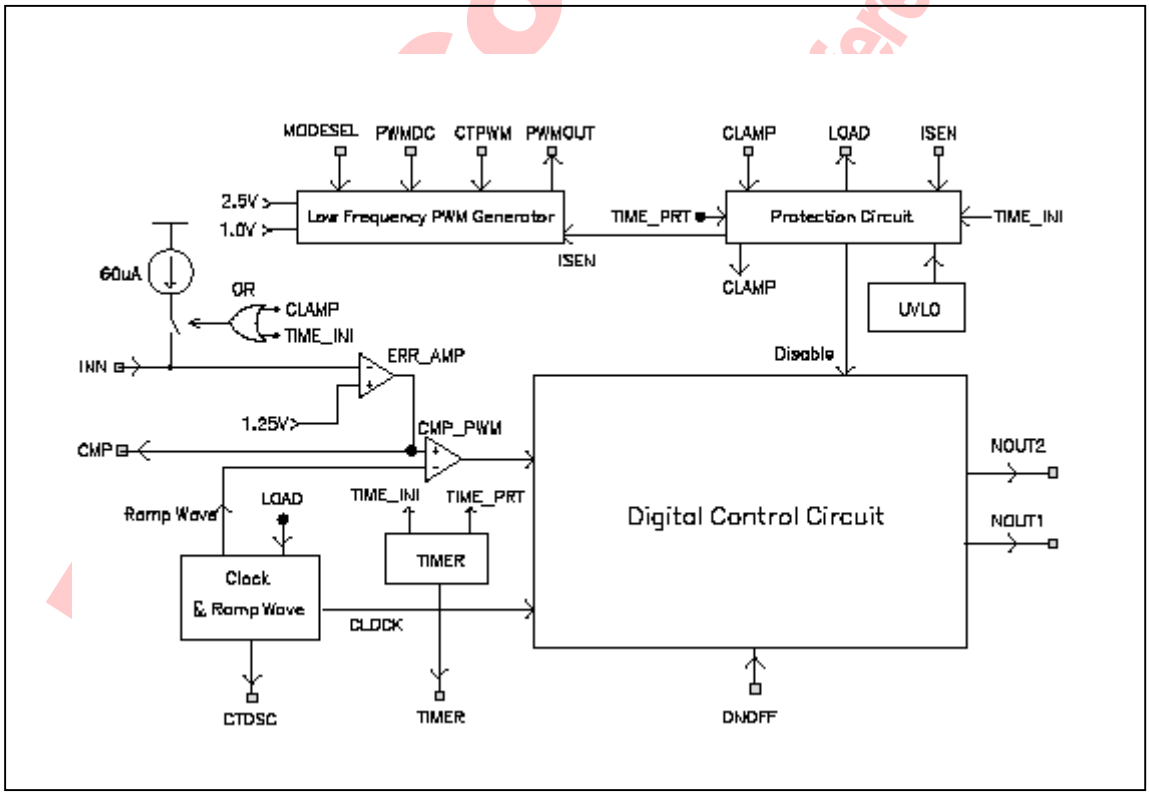
General Description:

BIT3193 integrated circuit provides the essential features for general purpose PWM controller in a small low cost 16-pin package. BIT3193 has built-in a low frequency PWM generator for any specified application. BIT3193 includes latched off protection feature may make the system more reliable while compare to other similar products.

Recommended Operating Condition:

Supply Voltage……4.5 ~ 8V
Operating Ambient Temperature……...0 ~ 70 ℃
Operating Frequency……50K ~ 400K Hz

Functional Block Diagram:



Pin Description:

Pin No.	Symbol	I/O	Descriptions
1	INN	I	The inverting input of the error amplifier.
2	CMP	O	Output of the error amplifier.
3	LOAD	I/O	A switch that connected to the high frequency triangle wave generator. This switch is open while ISEN pin <1.3V. An external resistor connected here may change the operation frequency of CTOSC in open load situation.
4	CTOSC	I/O	An external capacitor connected here can set the frequency of high frequency PWM controller.
5	TIMER	I/O	With internal reference current and an external capacitor connected here can set the required period of starting and the timing of initialization. The controller is forced to reset mode while TIMER <0.3V. During reset mode, a ~ 60uA current will flow into the INN pin to reduce the output level of the error amplifier CMP to turn off the controller. The latched off protection function will be enabled after this node is charged to > 2.5V. System is latched off if any abnormal operation is detected if pin TIMER > 2.5V. The output current of this pin is 20uA when TIMER < 0.3V. The output current becomes to 1uA when TIMER > 0.3V
6	ONOFF	I	The control pin of turning on or off the IC. 1V threshold with an internal 80K± 15% ohm pull-low resistor.
7	GND	I/O	The ground pin of the device.
8	NOUT2	O	The number 2 output driver for driving the NMOSFET switch.
9	NOUT1	O	The number 1 output driver for driving the NMOSFET switch.
10	VDD	I	The power supplies pin of the device.
11	PWMOUT	O	The output pin of low frequency PWM generator. A 2.5V or floating two state output is provided through this pin. The internal circuit limits the max. Duty-cycle to ~ 92%.
12	CTPWM	I/O	With the internal reference current and an external capacitor connected here can set the operation frequency of low frequency PWM generator with 1.0V ~ 2.5V triangle wave output.
13	PWMDC	I	Low frequency PWM controlling input. A PWM output comes out by comparing this DC input and the 1.0 ~ 2.5V triangle wave that is generated by CTPWM.
14	CLAMP	I	Over voltage clamping. If a > 2.0 V voltage is detected. A ~ 60uA current will flow into the INN pin to reduce the output of the error amplifier pin CMP to regulate the output voltage.
15	ISEN	I	Load current detection pin, the open load situation is detected if a less than 1.3V input is sensed.
16	MODSEL	O	To set the output polarity of the low frequency PWM controller.

Functional Description:

Trimmed Band Gap References: An internal trimmed band-gap reference provides a high accuracy, supply and temperature insensitive voltage reference. By amplifying or dividing this voltage can generate the other required references.

To Set the Operation Frequency of High Frequency PWM Controller: An external capacitor C_{CTOSC} pin CTOSC determines the frequency as equation (1)

The frequency of the high frequency PWM controller is:

$$F_{HFPWM} = \frac{K_{HF}}{C_{CTOSC}},\ K_{HF} = 8.2e-5 \quad .....(1)$$

or a 100KHz operation PWM control system if an 820pF capacitor is connected to pin CTOSC. Equation (1) is valid only when VDD=6V, temperature=30ºC and frequency ≈ 80K ~ 120KHz. Fig. 5 shows the relationship between the frequency of the high frequency PWM and CTOSC capacitance.

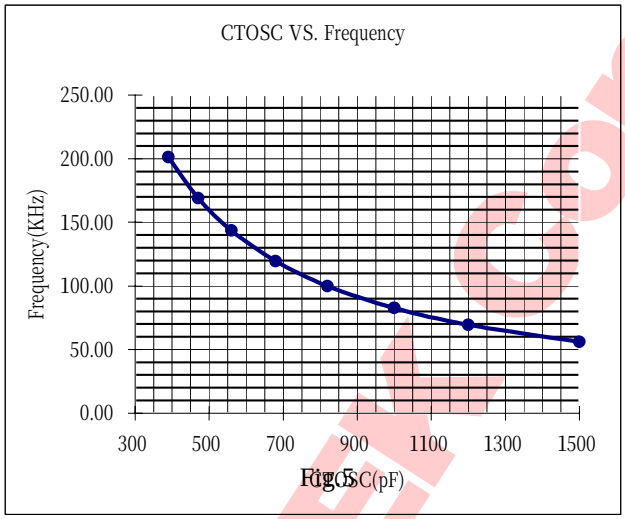


Fig. 5

The Power On Initialization: An internal current source charges the external capacitor connected on TIMER pin determines the initialization timing of BIT3193. This current provides ~ 20uA when TIMER pin less than 0.3V, and ~ 1uA when TIMER pin > 0.3V. BIT3193 is in an "initial state" when TIMER < 0.3V. Table 2 lists the status of each key features during TIMER < 0.3V.

Table 2 BIT3193 initial state

Pin Number	Pin Name	Status
1	INN	Force to VDD (With ~ 60uA current source)
4	CTOSC	Normally run
8	NOUT1	Forced to GND level
9	NOUT2	Forced to GND level
11	PWMOUT	Floating
12	CTPWM	Normally run

The Latched Off Protection_1: The ISEN pin may be used to detect if the operation is under well control during normal operation. In most of the applications to define a " staring period", in which period no signal feed back from the load side, is necessary. BIT3193 disable the latched off function when TIMER < 2.5V. If TIMER >2.5V and ISEN < 1.3V for 32 cycles of low frequency PWM. BIT3193 will shut the output pins NOUT1 and NOUT2 down until the system is powered on again.

The Latched Off Protection_2: The CLAMP pin may be used to detect if the PWM control system operates normally too. A ~ 60uA current source will charge the INN pin to reduce the output of CMP while CLAMP > 2.0V. The latched off over voltage protection performs while TIMER > 2.5V. If TIMER > 2.5V and CLAMP >2.0 V for 14 cycles of high frequency PWM. BIT3193 will shut the output pins NOUT1 and NOUT2 down until the system is powered on again.

To Set The Frequency Deviation of High Frequency PWM During Different Loading Condition: The LOAD pin may be used to change the frequency of CTOSC when ISEN < 1.3V. In many cases, the resonance frequency of the load is varied while the load is changed. For obtaining the better performance, the operation frequency of the PWM controller must fit to the resonance frequency of the load. A connect to GND resistor may increase the operation frequency of CTOSC. The following diagram shows how the load resistance changes the 100KHz operation frequency of CTOSC pin. In above case, CTOSC is connected by an 820pF capacitor. The normal operation frequency of high frequency PWM is 100KHz. If a different frequency says Fn is the set for normal operation.

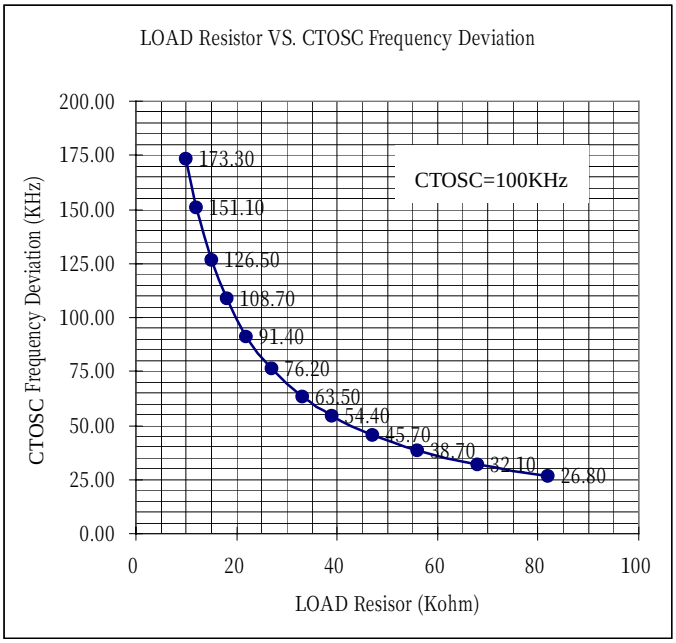


Fig.6

Then the frequency deviation can be calculated as Equation (2)

$$\Delta Fn = \frac{\Delta F100_{KHz} \times F_n}{100KHz} \text{.....(2)}$$

Setting the Frequency of Low Frequency PWM Generator: An internal trimmed low frequency oscillator generates a ± 3% accurate frequency on CTPWM pin with external capacitors. The capacitor values versus operation frequencies are as bellow:

$$F_{LFPWM} = \frac{4512}{[C_{CTPWM} + 0.005]nF} \text{.....(3)}$$

Note: Above equation (3) is valid only when operating frequency is between 150Hz ~ 1.5KHz

The logic high output of pin PWMOUT is made by an 2.5V DC voltage and the floating state makes the logic low portion. MODSEL pin provides the polarity selection of LF_PWM generator. If MODSEL pin is 0V, a 0% duty cycle is obtained when PWMDC < 1.0V. If this pin is pulled to IC VDD level, 0% duty cycle is obtained while PWMDC> 2.5V.

Note: BIT3193 limits the maximum duty cycle to ~ 92 %. PWMOUT sends the pulses when ISEN >1.3V or TIMER >2.5V.

UVLO: The under-voltage-lookout circuit turns the output driver off when supply voltage drops too low. Whole system includes the protection and timing circuits are reset (pin TIMER =0) in low VDD state.

DC/AC Characteristics:

Absolute Ratings:

Table 3

Parameter	Symbol	Ratings	Unit	Remarks
Supply Voltage	VDD	-0.3~+ 9	V	Ta=25°C
Ground	GND	±0.3	V	
Input pin Voltage		-0.3~ VDD+0.3	V	
Operating Ambit Temperature	Ta	0~ +70	°C	
Operating Junction Temperature		+150	°C	
Storage Temperature		-55~+150	°C	

DC/AC Characteristics

Table 4

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Supply Voltages					
Pin VDD input		4.0		8	V
Chip Consumed Current	8V Supply Voltage Ta=25°C		4		mA
Error Amplifier Reference Voltage					
Non-Inverting input of the error amplifier	Measure INN	1.2125	1.25	1.2875	V
Line regulation	VDD=4.0~13.2 V		2	20	mV
Under Voltage Look Out					
Positive Going Threshold	Ta=25°C Note3	3.8	4.0	4.2	V
Hysteresis		0.1	0.2	0.3	V
High Frequency Ramp Wave Generator					
Operating Frequency	Note1	50		400	KHz
Output peak(CTOSC)			2.25		V
Output valley(CTOSC)			0.5		V
Error Amplifier					
Input voltage	Note2	0.1		3	V
Open loop gain		60	80		dB
Unit gain band width		1	1.5		MHz
Power On Initialization and Latched Off Protection Enable					
Pin TIMER Output current Case1. TIMER <0.3V	VDD=12V, Ta=25°C Note 3		20		uA
Pin TIMER Output current Case1. TIMER > 0.3V			1		uA
Power On Reset/Initialization threshold on pin TIMER			0.3		V
Latched Off Protection enable threshold on pin TIMER			2.5		V
Open Load Detection					
Pin ISEN open load detection lower threshold	VDD=12V, Ta=25°C		1.3		V
Hysterisis			20		mV
Over Voltage Detection and Clamping					
Pin CLAMP over voltage detection lower threshold	VDD=12V, Ta=25°C		2.0		V
Hysterisis			20		mV
INN pin pull-up current source			60		uA
Low Frequency PWM Generator					
Ramp Wave Peak(CTPWM)	VDD=12V, Ta=25°C		2.5		V
Ramp Wave Valley(CTPWM)			1.0		V
PWM Frequency		10		100K	Hz
Control voltage of 0 % Duty cycle on pin PWMDC Case 1. MODSEL = 0V			1.0		V
Control voltage of 0 % Duty cycle on pin PWMDC Case 1. MODSEL = ICVDD			2.5		V
Output voltage of Pin PWMOUT for making the logic “high”.			2.5		V
Pin PWMOUT output for making the logic “low”			Floating		
Maximum Duty Cycle			92		%
Output					
CMOS output impedance	(Note2, Note3)		50		ohm
Rising Time	VDD=12V, 2000pF(Note2, Note3)		110		nS
Falling Time			100		nS
Delay Time			200		nS

Note 1. The output driver frequency is the half of the ramp wave frequency.
Note 2. Only verified by simulation. Not 100% tested.
Note 3. The voltages of the output drivers are pulled to GND in each off states.

Timing Diagram

BIT3193 fixed frequency push pull driving methodology to drive the load. The power switches; NMOSFETs are driven by fixed frequency PWM controlled signals. The detail timing relationship is shown as bellow: The maximum duty cycle of NOUT1 and NOUT2 are < 50% with 180° phase shift.

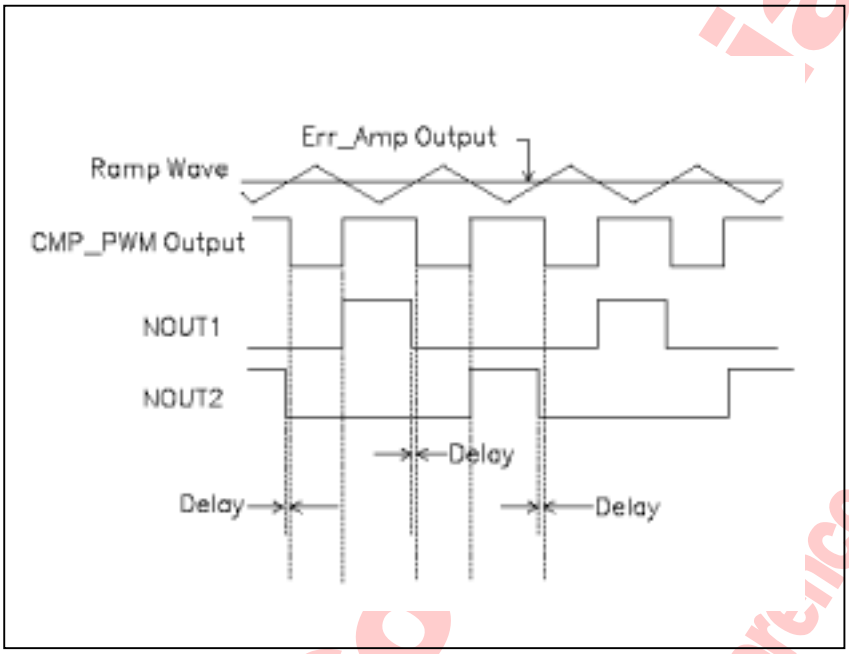


Fig. 3

The timing of another low frequency PWM generator is as bellow: A 51Kohm pulled-low resistor is connected on PWMOUT pin in this example.

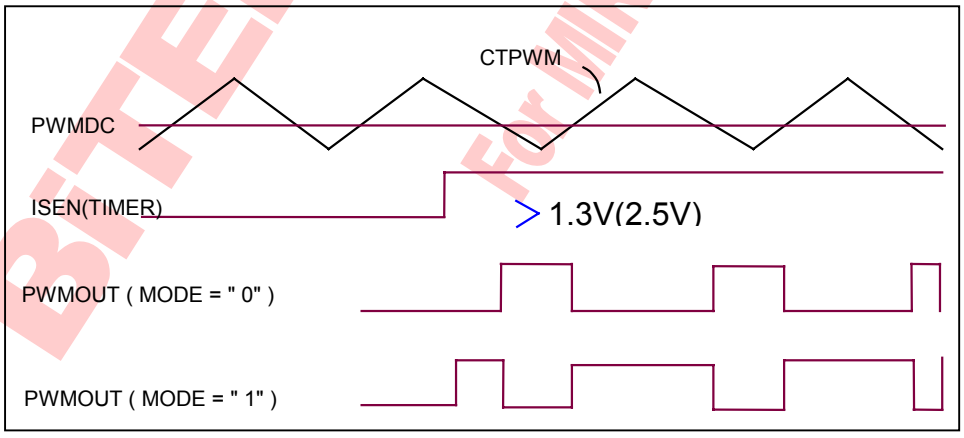


Fig. 4

Order Information:

BIT3193-SO

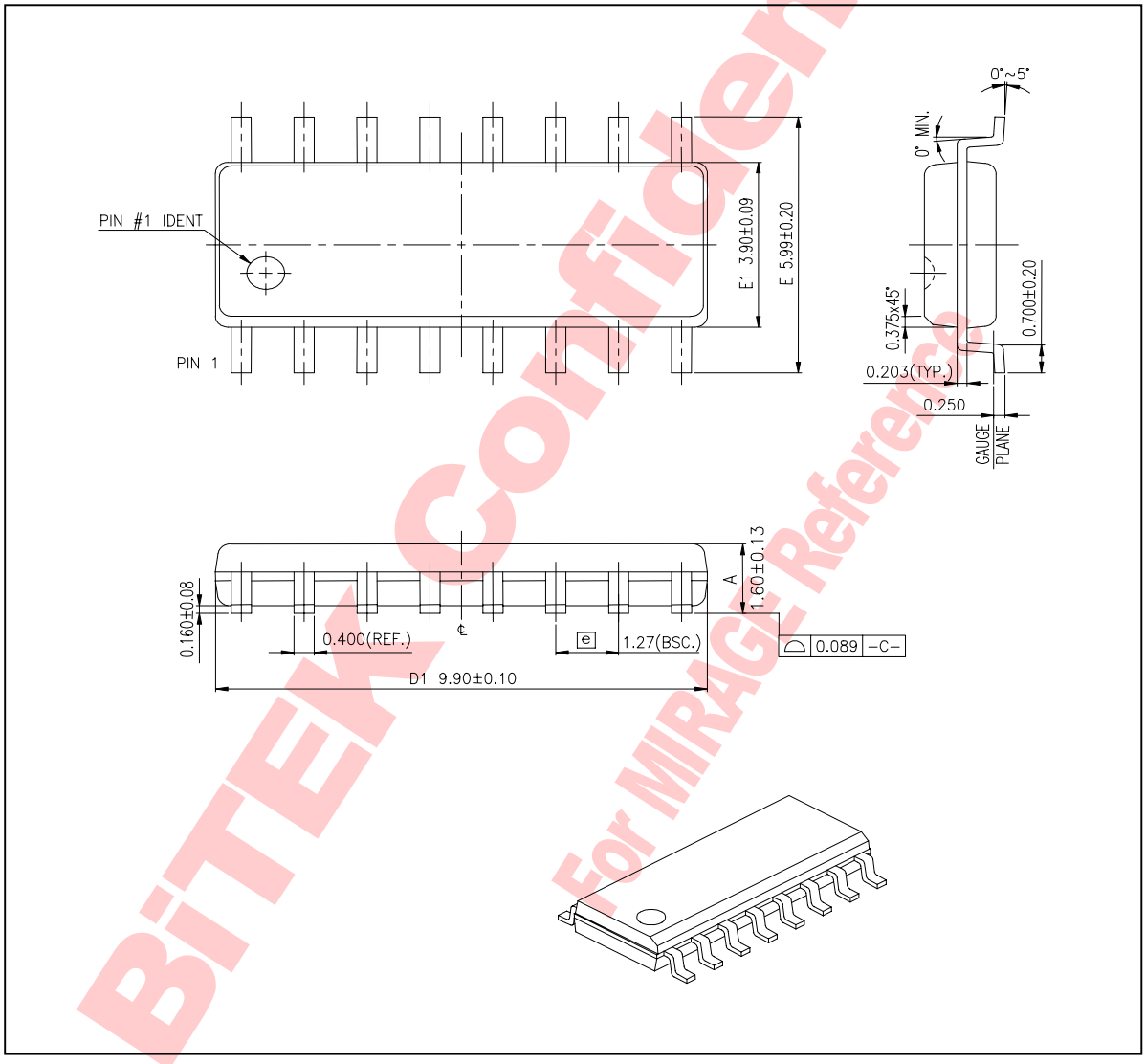
SO: SOP **SS:** SSOP **DP:** DIP

Part number

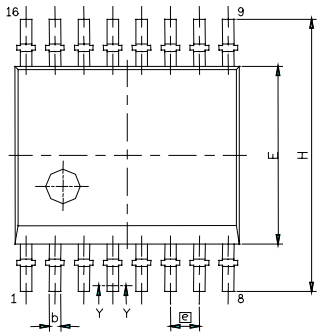
Beyond Innovation Technology Co., Ltd.

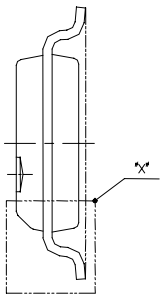
Package Information :

SOP type :

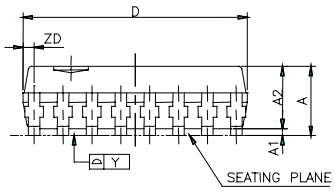


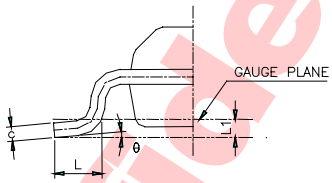
SSOP type :

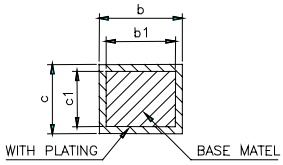




SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1,346	1,600	1,727	53	63	68
A1	0,102	0,152	0,229	4	6	9
A2		1,448	1,499		57	59
b	0,203		0,305	8		12
b1	0,203	0,254	0,279	8	10	11
c	0,178		0,254	7		10
c1	0,178	0,203	0,229	7	8	9
D	4,801	4,928	5,004	189	194	197
E	3,835	3,912	3,988	151	154	157
H	5,867	5,994	6,121	231	236	241
e	0,635 BASIC			25 BASIC		
ZD	0,241 REF			9,5 REF		
L	0,533	0,660	0,787	21	26	31
L1	0,254 BASIC			10 BASIC		
Y			0,106			4
θ	0°	5°	8°	0°	5°	8°



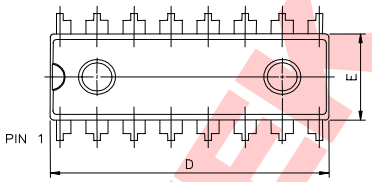


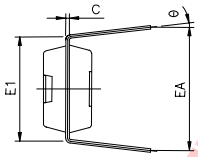


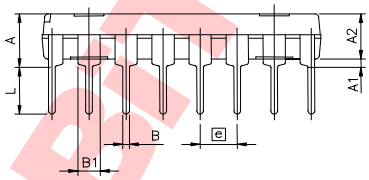
NOTES :

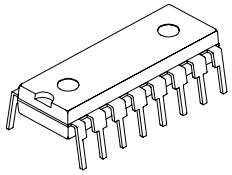
1. CONTROLLING DIMENSION : MILLIMETERS.
2. REFER TO JEDEC MO-137 AB.
3. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTURSIONS AND GATE BURRS SHALL NOT EXCEED 0,15mm (6mil) PER SIDE.
4. DIMENSION "E"DOES NOT INCLUDE INTER-LEAD FLASH OR PROTURSIONS. INTER-LEAD FLASH AND PROTURSIONS SHALL NOT EXCEED 0,25mm (10mil) PER SIDE.

DIP type :









SYMBOL	DIMENSION IN INCH	DIMENSION IN MM
A	0.170 MAX.	4.318 MAX.
A1	0.015 MIN.	0.381 MIN.
A2	0.130±0.005	3.302±0.127
B	0.018 TYP.	0.457 TYP.
B1	0.060 TYP.	1.524 TYP.
C	0.010 NOM.	0.254 NOM.
D	0.752±0.005	19.101±0.127
E	0.252±0.005	6.401±0.127
E1	0.300±0.010	7.62±0.254
EA	0.355±0.020	9.017±0.508
e	0.100 TYP.	2.540 TYP.
L	0.130±0.010	3.302±0.254
θ	0°~15°	0°~15°

NOTE:
1.DIMENSION D & E DOES NOT INCLUDE FLASH.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Life Support Applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in person injury. BiTEK customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify BiTEK for any damages resulting from such improper use or sale.