NSD1624

High Reliability, Half Bridge Gate Driver

Datasheet (EN) 0.4

Product Overview

NSD1624 is a high voltage, high side-low side gate driver having capability to deliver 4A source and sink current to drive power MOSFETs or IGBTs.

The high side section is designed to endure a DC voltage over 1200V with innovative and proven isolation technology. NSD1624 offers best in class propagation delay, low quiescent current, high negative and dv/dt immunity on SW pin.

Both high side and low side driver section work from 10V to 20V supply voltages having independent under voltage lockout (UVLO) protection. NSD1624 has two independent input pins (HIN and LIN) which are compatible for TTL and CMOS logic. NSD1624 is available in LGA10, SOP8, and SOP14 package with operating temperature range from -40°C to 125°C.

Key Features

- High voltage range: Up to 1200V(SOP14)/700V(SOP8)
- Less than 35ns Propagation Delay
- Less than 7ns Delay Matching
- 4 A Source / 6A Sink Currents
- High Negative and Transient Immunity up to 150V/ns on SW pin
- Gate Drive Supply Voltage from 10V to 17V
- TTL and CMOS Compatible Input Logic
- UVLO Protection for High-side and Low-side Drivers
- Separated Grounds for Logic (SGND) and Driver in SOP14 package
- High and Low Voltage Pins Separated for Maximum Creepage and Clearance in SOP14 package

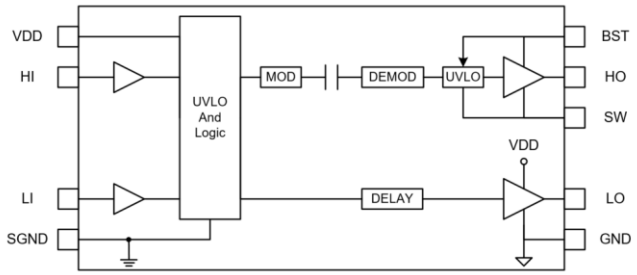
Applications

- Half-bridge, full-bridge and LLC converters.
- High density switching power supplies for Server, Telecom and Industrial
- Solar inverters, Motor controls and EV charges

Device Information

Part Number	Package	Body Size
NSD1624-DLAJR	LGA10	4.0 mm × 4.0 mm
NSD1624-DSPKR	SOP14(150mil)	8.6 mm × 3.9 mm
NSD1624-DSPR	SOP8(150mil)	4.9 mm × 3.9 mm

Functional Block Diagram



NSD1624 Block Diagram

1 INDEX

1. Pin Configuration and Functions

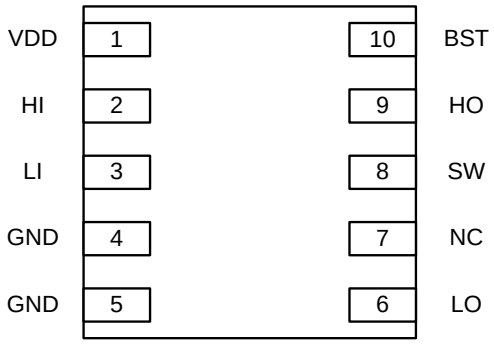


Figure 1.1 NSD1624 LGA10 Package

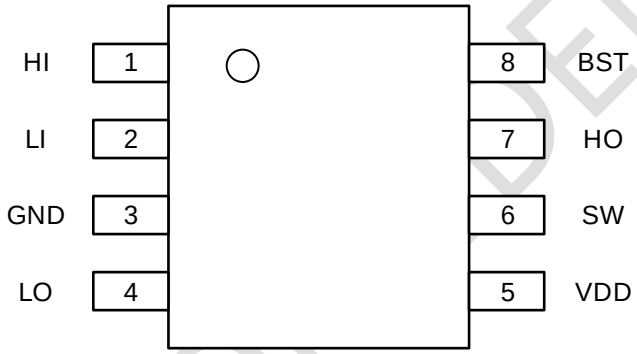


Figure 1.2 NSD1624 SOP8 Package

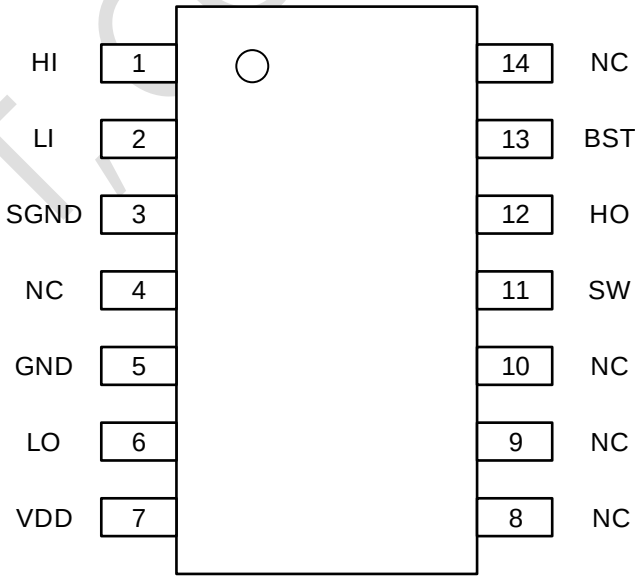


Figure 1.3 NSD1624 SOP14 Package

Table 1.1 NSD1624 Pin Configuration and Description

PIN NO.			SYMBOL	FUNCTION
LGA10	SOP14	SOP8		
4,5	5	3	GND	Power Ground, return for low-side driver.
2	1	1	HI	Logic input for high-side driver.
3	2	2	LI	Logic input for low-side driver.
1	7	5	VDD	Power supply for the input logic part and low-side driver.
6	6	4	LO	Low-side driver output.
9	12	7	HO	High-side driver output.
10	13	8	BST	High-side floating supply.
8	11	6	SW	High-side supply return.
/	3	/	SGND	Signal ground, reference for input
7	4,8,9,10,14		NC	Not connected

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit
Input Supply Voltage	V_{VDD}	-0.3	24	V
High side SW pin voltage	V_{SW}	-700	700	V
High side SW pin voltage	V_{SW}	-700	700	V
High side floating voltage	V_{BST} - V_{SW}	-0.3	24	V
High side output voltage	V_{HO}	V_{SW}-0.3	V_{BST}+0.3	V
	V_{HO}, Transient for 100ns	V_{SW}-2	V_{BST}+0.3	
Low side output voltage	V_{LO}	-0.3	V_{VDD}+0.3	V
	V_{LO}, Transient for 100ns	-2	V_{VDD}+0.3	V
Signal ground to GND[1)]	V_{SGND}	-5	5	V
Input voltage to Signal ground	V_{HI}, V_{LI}, V_{VDD}	V_{SGND}-0.3	V_{SGND}+20	V
Junction Temperature	T_J	-40	150	℃
Storage Temperature	$T_{J.ST}$	-40	150	℃
Electrostatic discharge	HBM	-2000	2000	V
	CDM	-1000	1000	V

1) Only for NSD1624 SOP14 Package

3. Recommended Operating Conditions

Parameters	*Symbol*	*Min*	*Max*	*Unit*	*Comments*
Input Supply Voltage Range	V_{VDD}	10	17	V	
High Side Floating Voltage	V_{BST}- V_{SW}	10	17	V	
High Side SW Pin Voltage	V_{SW}	-700	700	V	
High Side Output Voltage	V_{HO}	V_{SW}	V_{BST}	V	
Low Side Output Voltage	V_{LO}	0	V_{VDD}	V	
Input Signal Voltage Range	V_{HI}, V_{LI}	V_{SGND}	V_{SGND}+17	V	
Signal ground	V_{SGND}	-3	3	V	
Junction Temperature	T_J	-40	125	℃	
Ambient Temperature	T_a	-40	125	℃	

4. Thermal Information

Parameters	*Symbol*	*LGA10*	*SOP8*	*SOP14*	*Unit*
Junction-to-ambient thermal resistance	θ_{JA}				℃/W
Junction-to-case(top) thermal resistance	$\theta_{JC(top)}$				℃/W
Junction-to-board thermal resistance	θ_{JB}				℃/W

1) Standard JESD51-3 Low Effective Thermal Conductivity Test Board (1s) in an environment described in JESD51-2a.
2) Standard JESD51-3 Low Effective Thermal Conductivity Test Board (1s) by transient dual interface test method described in JESD51-14.
3) Obtained by Simulating in an environment described in JESD51-2a.

5. Specifications

5.1. Electrical Characteristics

At V_{VDD} = V_{BST} = 15 V, V_{SGND} = V_{SW} = 0, all voltages are with respect to GND, no load on LO and HO, –40°C < T_J < 125°C

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply Section						
VDD quiescent current	I_{VDD_Q}		0.4	0.5	mA	V_{LI} = V_{HI} = 0
High-side supply quiescent current	I_{BST_Q}		0.6	0.7	mA	V_{LI} = V_{HI} = 0
VDD operating current	I_{VDD_O}		1.1	/	mA	f = 500 kHz, C_{LOAD} = 0

High-side supply operating current	I_{BST_O}		1.3	/	mA	f = 500 kHz, C LOAD = 0
SW to GND leakage current	I_{SW_LK}			0.01	uA	V_{SW} = 700V
INPUT SECTION						
Input rising threshold	V_{HI_H}, V_{LI_H}	1.8	2.1	2.4	V	
Input falling threshold	V_{HI_L}, V_{LI_L}	0.9	1.2	1.5	V	
Input voltage Hysteresis	V_{HI_HYS}, V_{LI_HYS}		0.9		V	
High Level Logic Input Bias Current	I_{IN+}		17		uA	V_{LI} / V_{HI} = 5V
Low Level Logic Input Bias Current	I_{IN-}		0	10	uA	V_{LI} = V_{HI} = 0V
Input pulldown resistance	R_{IN}		260		kohm	V_{LI} = V_{HI} = 3V
UNDER VOLTAGE LOCKOUT						
turn-on threshold voltage of VDD	V_{DD_UV+}	8.6	9.1	9.5	V	
turn-off threshold voltage of VDD	V_{DD_UV-}	8.2	8.7	9.1	V	
V CC hysteresis	V_{DD_UVH}		0.4		V	
UVLO positive Threshold on V_{BST}-V_{SW}	V_{BST_UV+}	7.9	8.4	8.9	V	
UVLO negative Threshold on V_{BST}-V_{SW}	V_{BST_UV-}	7.4	7.9	8.3	V	
VBST hysteresis	V_{BST_UVH}		0.5		V	
Output SECTION						
Low level output voltage	V_{OL}		0.06		V	I_{LO} =100 mA
High level output voltage	V_{OH}		0.12		V	I_{LO} =-100 mA, V_{LOH} = V_{VDD}-V_{LO}
Low level output Resistance	R_{OL}		0.6		Ohm	
High level output Resistance	R_{OH}		1.2		Ohm	
Peak source current	I_{OSRC}		4		A	V O=0 V
Peak sink current	I_{OSNK}		6		A	V O=VDD

5.2. Switching Characteristics

At V_{VDD} = V_{BST} = 15 V, V_{SGND} = V_{SW} = 0, all voltages are with respect to GND, no load on LO and HO if not mentioned, –40°C < T_J < 125°C

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
High Side Startup Time	$T_{startup}$		10	15	us	between VB>UVLO and First HO Pulse
Rise Time LO, HO	T_R		10		ns	C load = 1000 pF
Fall Time LO, HO	T_F		9		ns	C load = 1000 pF
Low-to-high delay matching	T_{LHDM}			7	ns	Pulse width = 1 us

High-to-low delay matching	T_{HLDM}			7	ns	Pulse width = 1 us
Minimum Input Filter	T_{MPW}		11	17	ns	
Turn-on delay, LI to LO	T_{LDLH}		22	35	ns	
Turn-off delay, LI to LO	T_{LDHL}		22	35	ns	
Turn-on delay, HI to HO	T_{HDLH}		22	35	ns	
Turn-off delay, HI to HO	T_{HDHL}		22	35	ns	

5.3. Typical Performance Characteristics

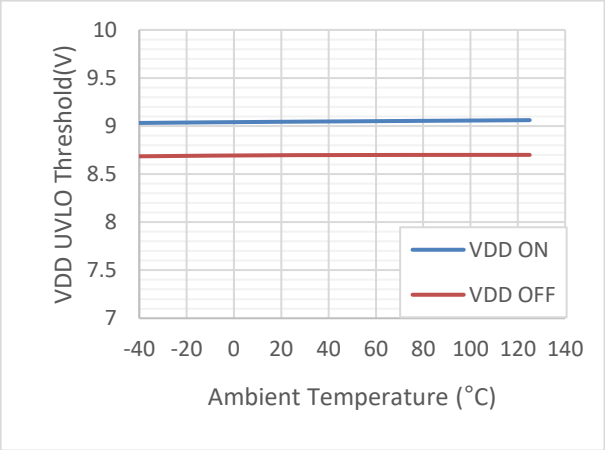


Figure 5.1 VDD UVLO Threshold vs Temperature

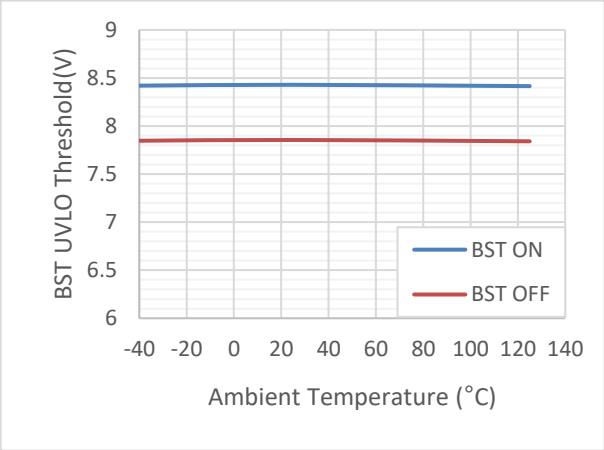


Figure 5.2 BST UVLO Threshold vs Temperature

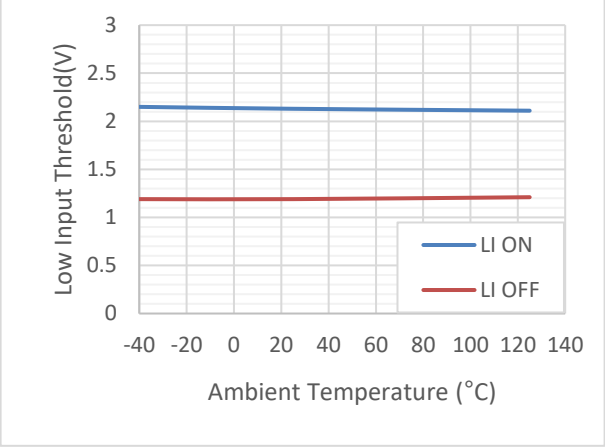


Figure 5.3 Low Input Logic Threshold vs Temperature

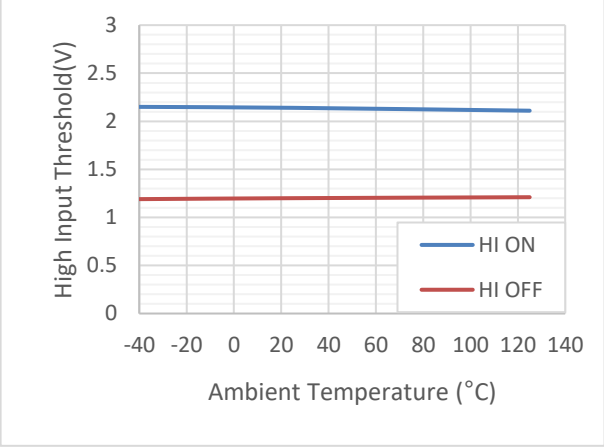


Figure 5.4 High Input Logic Threshold vs Temperature

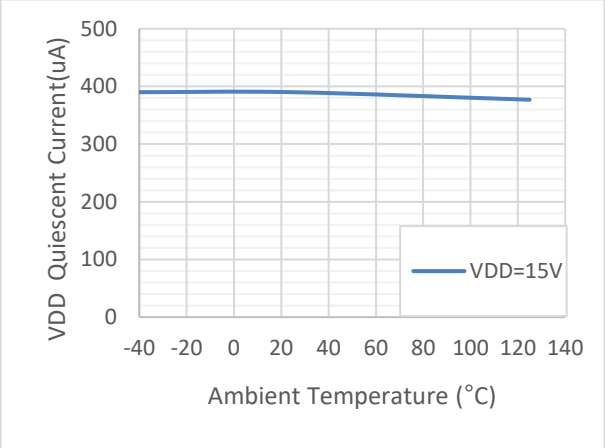


Figure 5.5 VDD Quiescent Current vs Temperature

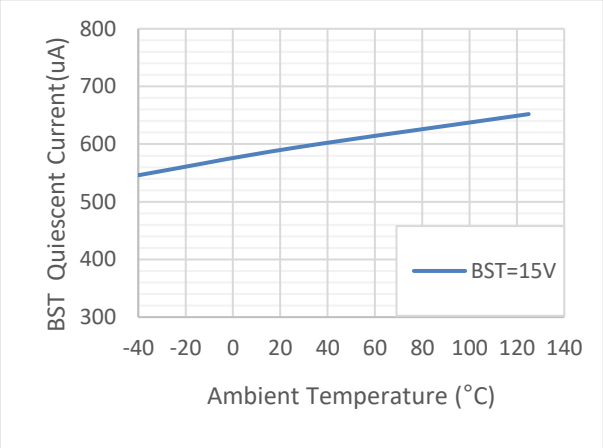


Figure 5.6 BST Quiescent Current vs Temperature

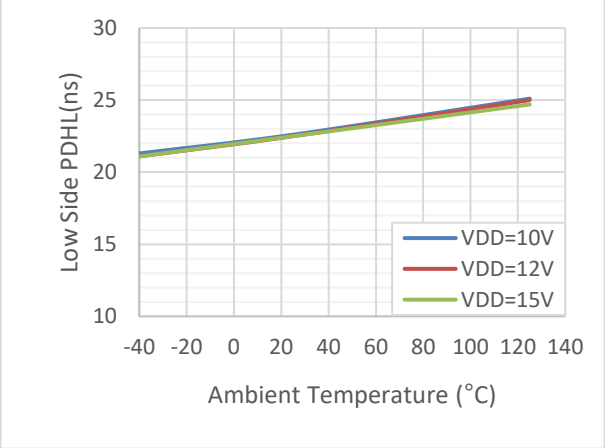


Figure 5.7 Low Side Turn-off Delay vs Temperature

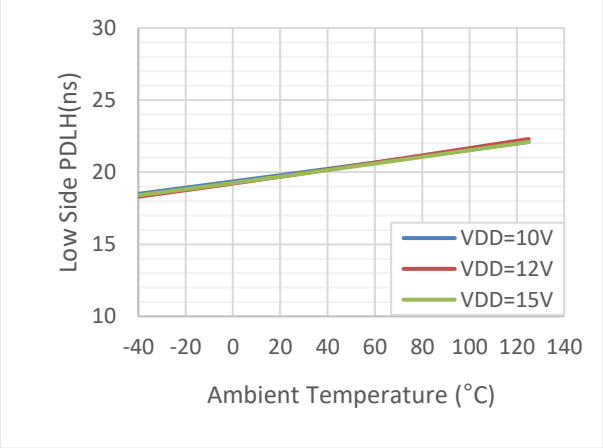


Figure 5.8 Low Side Turn-on Delay vs Temperature

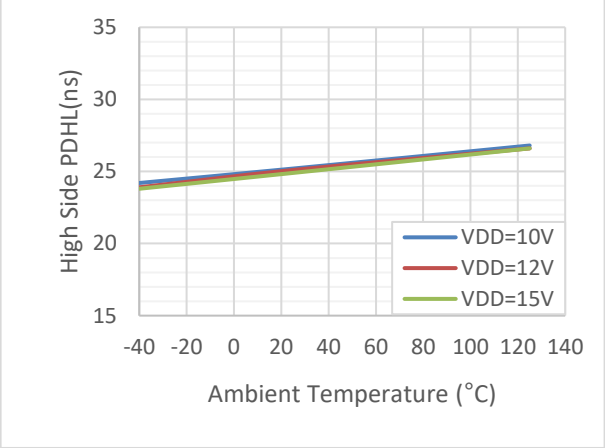


Figure 5.9 High Side Turn-off Delay vs Temperature

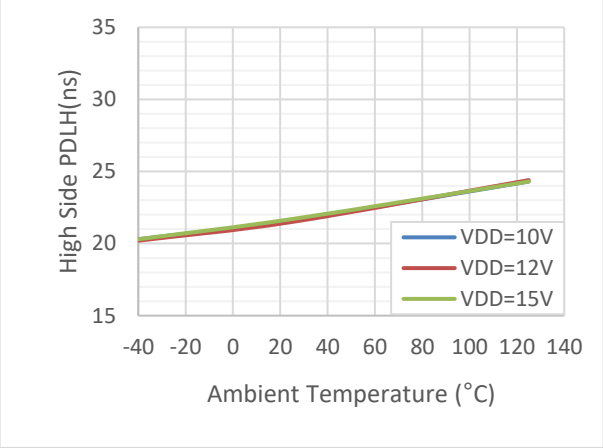


Figure 5.10 High Side Turn-on Delay vs Temperature

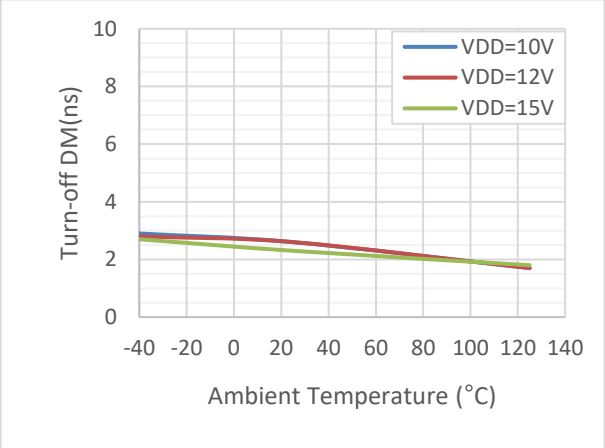


Figure 5.11 Turn-off Delay Match vs Temperature

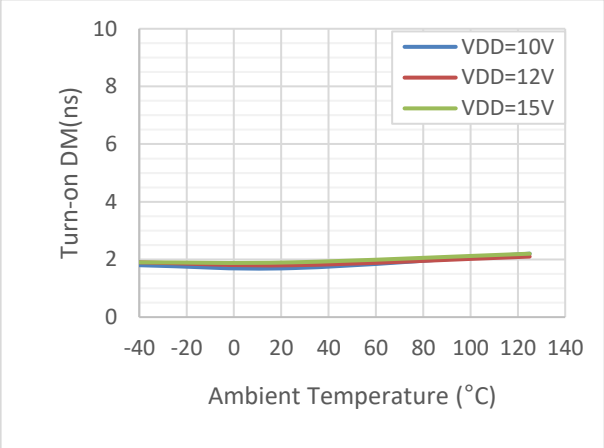


Figure 5.12 Turn-on Delay Match vs Temperature

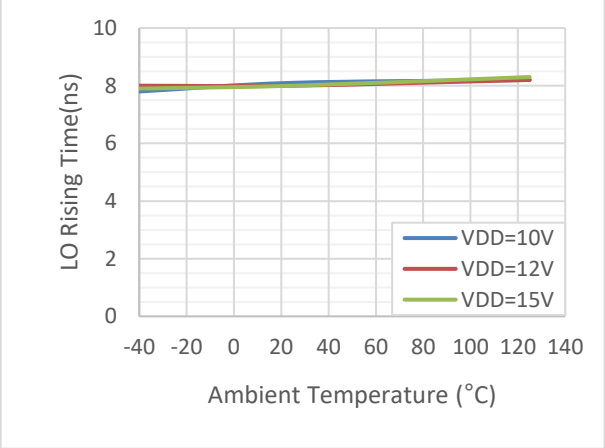


Figure 5.13 LO Rising Time(Co=1000pF) vs Temperature

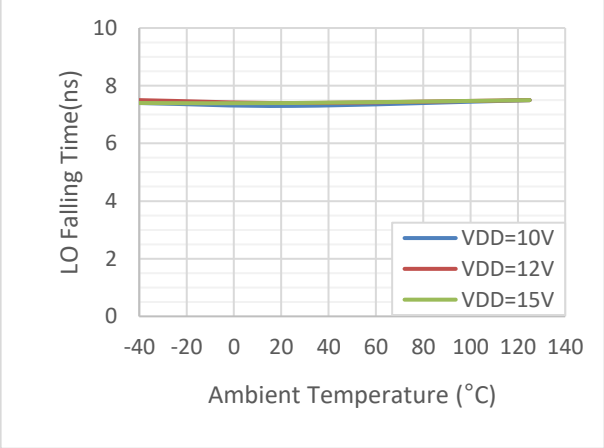


Figure 5.14 LO Falling time(Co=1000pF) vs Temperature

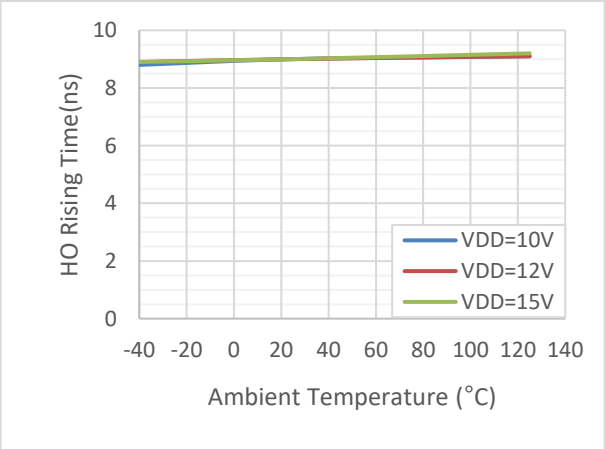


Figure 5.15 HO Rising Time(Co=1000pF) vs Temperature

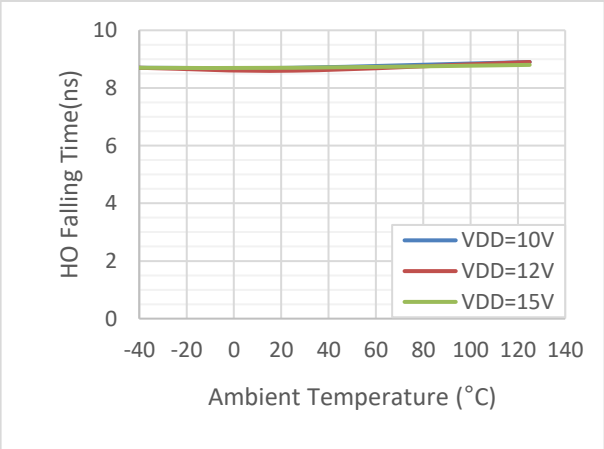


Figure 5.16 HO Falling time(Co=1000pF) vs Temperature

5.4. Parameter Measurement Information

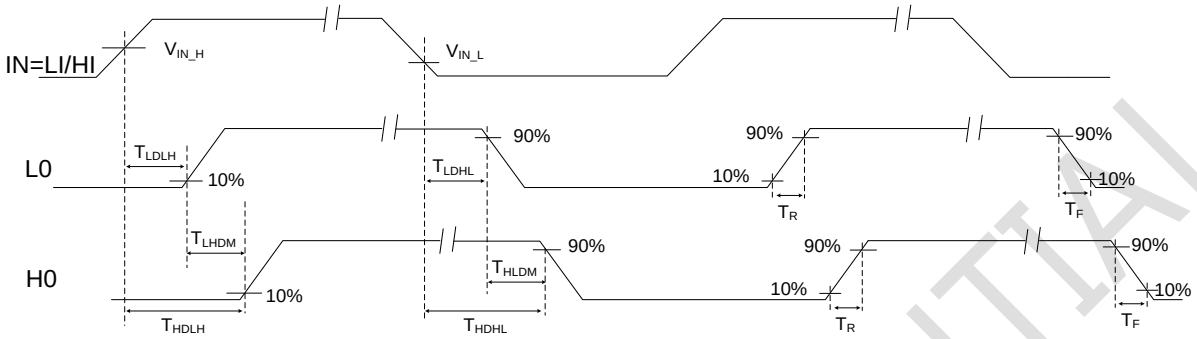


Figure 5.17 Propagation Delay, Channel to Channel Delay Match, rise and fall time

6. General Description

6.1. Overview

NSD1624 is a high reliability low side-high side gate driver with two independent input pins HIN and LIN dedicated to be used in AC-DC and DC-AC power applications. Driver inputs are compatible with CMOS and TTL logic hence it provides easy interface with analog and digital controllers. The high side is a floating section that usually require an effective bootstrap circuit to bias. High side Isolated driver has high negative and dv/dt immunity on SW pin that improve the robustness of the driver. NSD1624 has independent under voltage lock out feature for both high and low side gate drivers which ensure the working of both channels at V_{DD_UV+} and V_{BST_UV+}.

In popular power converter topologies such as; half bridge, full bridge converter, LLC, two switch forward converter and phase-shift full bridge, low and high side gate driver provides a function of buffer and level shifter. This driver can drive the top side MOSFET and IGBT whose source and emitter node is a dynamically changing. Therefore, to make them stable referenced to a fixed potential, floating-driver devices are necessary to use in these topologies.

NSD1624 offers best in class propagation delay, less than 7ns delay matching, low quiescent and operating current at high frequencies. Input pins (HI and LI) allow full and independent flexible ON-OFF state of the output.

6.2. Functional Block Diagram

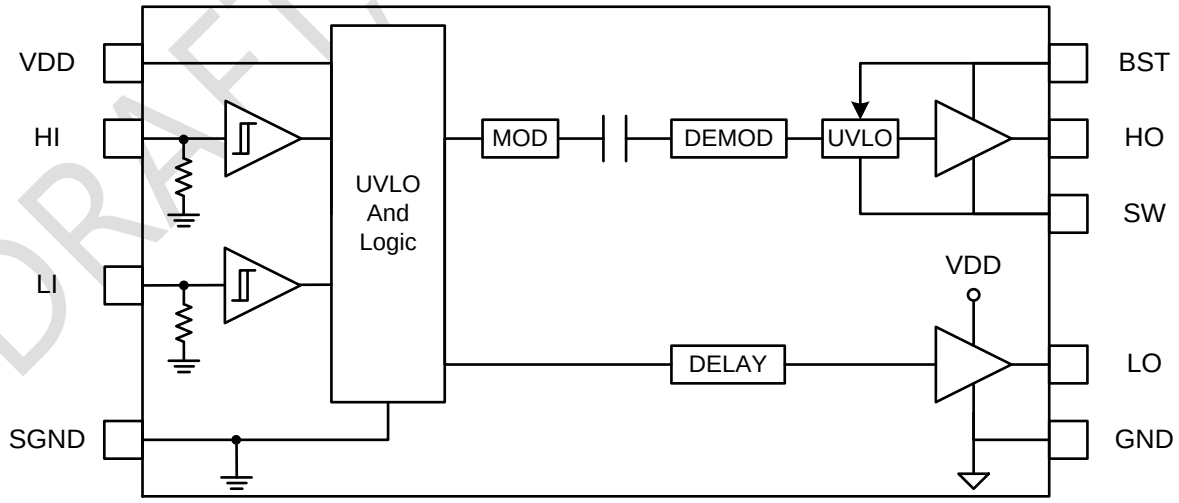


Figure 6.1 Functional Block Diagram

6.3. Feature Description

6.3.1 Under Voltage Lock Out (UVLO)

NSD1624 has independent under voltage lock out feature for both high and low side gate drivers which ensure the working of both channels at VDD_UV+ and VBST_UV+. If the VDD is below the VDD_UV+, the output of both high and low side channel will remain low. Similarly, if the VBST is below the VBST_UV+, the output of high side channel will remain low. So the high side bias voltage has no influence on the low side output channel, regardless of the state of the input signal.

The VDD and VBST ULVO protection circuits have hysteresis (VVDD_HYS) to prevent ground noise in power supply. Hysteresis also allow small drops in supply power which are usually happen in startup.

6.3.2 Input Stage

NSD1624 is a low side-high side gate driver with two independent input pins HIN and LIN. Both the inputs are compatible with CMOS and TTL logic which ensures that the inputs can be driven with analog and digital controllers.

The typical value of high input threshold (VIN_H) is 2.1 V whereas the low threshold (VIN_L) 1.2V. The typical value of hysteresis on input pins is 0.9 V which offers higher noise immunity compared to traditional TTL logic implementations. NSD1624 also feature tight control of the input pin threshold voltage levels which ease system design consideration and ensure stable operation across temperature.

Both the input pins are internally pulled-down through a resistor of 260K which indicates its logic state in case of floating pin. This feature can be regarded as important because the outputs stay low in case of any input is floating. It is recommended to ground the unused input pin especially in the practical applications. The input logic is explained in the following table.

6.3.3 Input Table

INPUTS		OUTPUTS	
LI	*HI*	*LO*	*HO*
L	H	L	H
H	L	H	L
H	H	L	L
L	L	L	L

6.3.4 Output Stage

NSD1624 is equipped with two independent drivers. The device has ability to provide 4A source and sink current which can effectively charge and discharge a load capacitor of 1nF in 10ns. There is no dead-time built in function in NSD1624, so both outputs can be turned-on at the same time. This feature allows NSD1624 to be used for two-switch converter.

7. Application Note

7.1. Typical Application Circuit

The circuit shows a typical half-bridge configuration by using the driver NSD1624 which could be used in several popular power converter topologies such as half-bridge/full bridge/LLC isolated topologies applications.

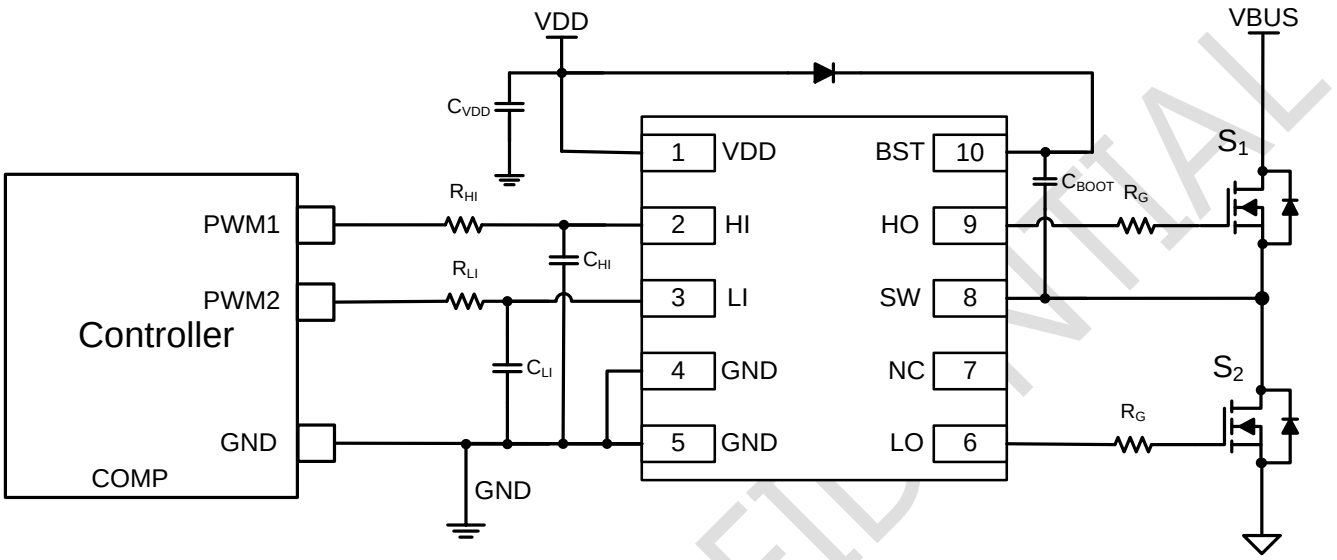


Figure 7.1 Simplified Half-Bridge Schematic

7.2. ESD Structure

Figure.7.2 illustrates the multiple parasitic diodes involved in the ESD protection components of NSD1624 device.

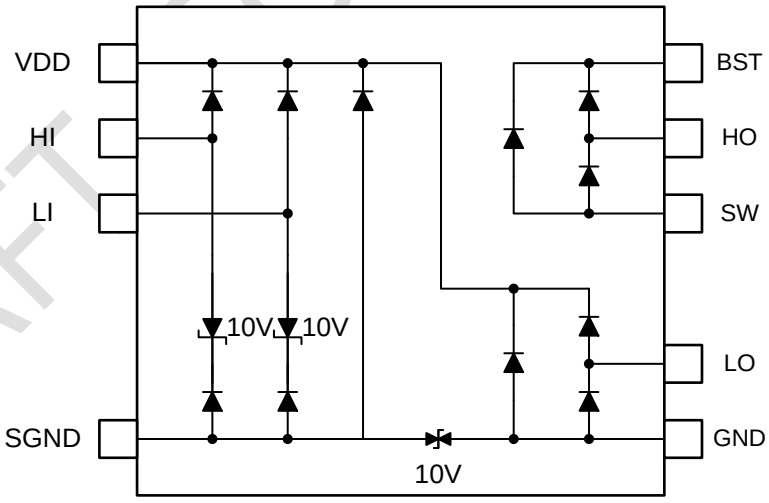


Figure 7.2 ESD Structure for SOP14

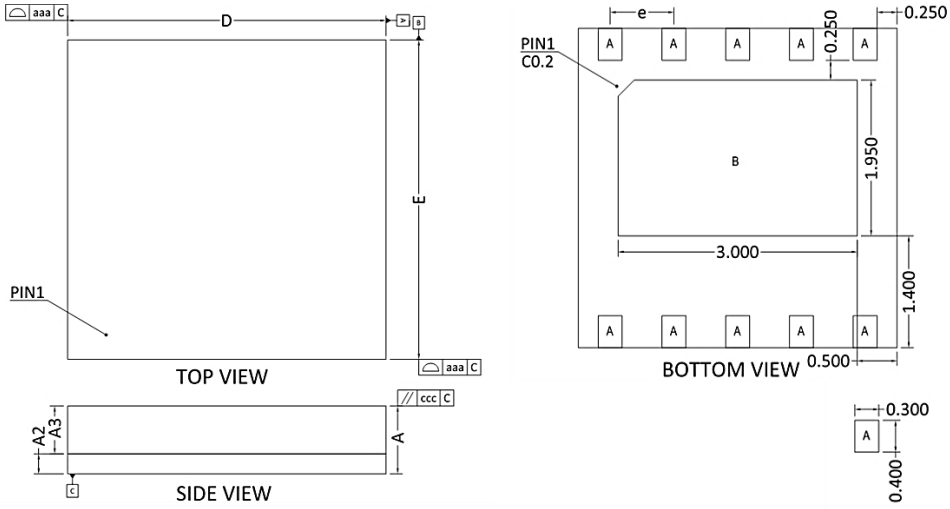
7.3. Layout Recommendations

PCB layout is important to get optimal performance. Some of the layout guidelines to be followed are listed below:

- High frequency switching current that charges and discharges the gate of external power transistor, that causes EMI and ringing issues. In order to minimize the parasitic inductance and ringing on the gate terminal of the low side MOSFET S2, keep the low side loop 'LO-S2-GND' as small as possible. Similarly, keep the path of high side driver 'HO-S1-SW' as minimum as possible.
- Place a bypass capacitor C_{VDD} as close to VDD pin as possible and minimized the path of 'VDD-C_{VDD}-GND'. Similarly, follow the same rule for 'VBST-C_{BOOT}-SW' loop.
- Place a RC input filter with R=2 to 5Ω, & C=100pF close to the driver input pins (HI, LI)
- Use of SMD type devices with low-ESR and low-ESL capacitor are highly recommended.
- Large amount of copper should be placed at VDD, BST, GND, and SW pins for thermal dissipation.

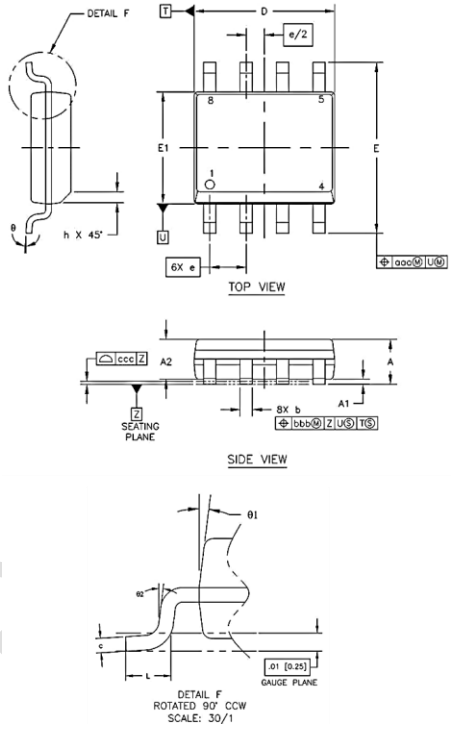
7.4. Example

8. Package information



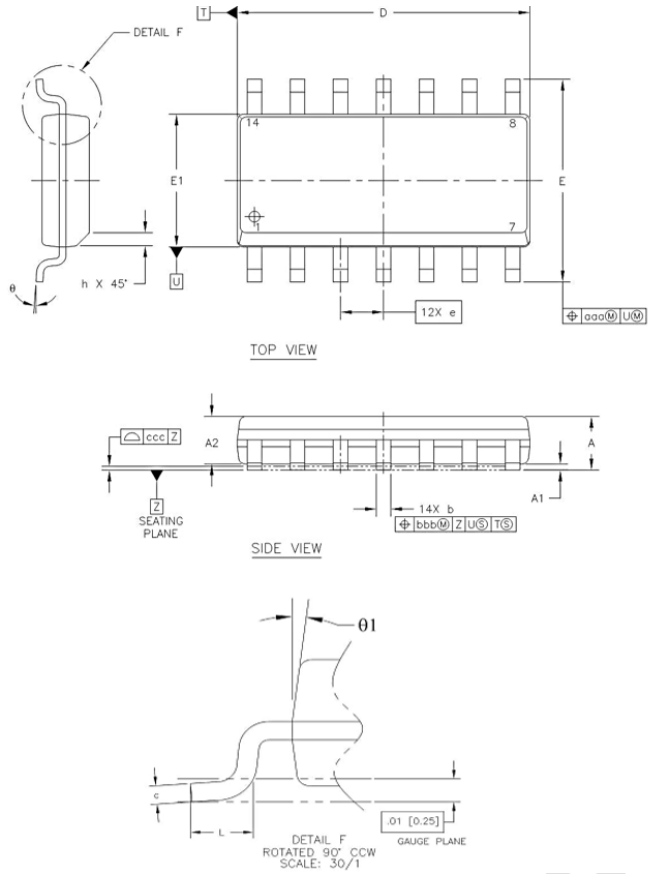
MILLIMETER			
SYMBOL	MIN	NOR	MAX
A	0.77	0.85	0.93
A2	0.22	0.25	0.28
A3	0.55	0.60	0.65
D	3.90	4.00	4.10
E	3.90	4.00	4.10
e	0.8 BSC		
aaa	0.10		
ccc	0.05		

Figure 9.1 LGA10 4X4 Package Shape and Dimension



DESCRIPTION	SYMBOL	MILLIMETER		
		MIN	NOM	MAX
TOTAL THICKNESS	A	1.35		1.75
STAND OFF	A1	0.10		0.25
MOLD THICKNESS	A2	1.25		---
LEAD WIDTH	b	0.35		0.49
L/F THICKNESS	c	0.19		0.25
BODY SIZE	D	4.80		5.00
	E1	3.80		4.00
	E	5.80		6.20
LEAD PITCH	e	1.27 BSC		
	L	0.40		1.25
	h	0.25		0.50
	θ	0°		7°
	θ1	5°		15°
	θ2	2°	7°	12°
LEAD EDGE OFFSET	aaa	0.25		
LEAD OFFSET	bbb	0.25		
COPLANARITY	ccc	0.10		

Figure 9.2 SOP8 Package Shape and Dimension



DESCRIPTION	SYMBOL	MILLIMETER		
		MIN	NOM	MAX
TOTAL THICKNESS	A	1.35	---	1.75
STAND OFF	A1	0.10	---	0.25
MOLD THICKNESS	A2	1.25	---	---
LEAD WIDTH	b	0.33	---	0.51
L/F THICKNESS	c	0.19	---	0.25
BODY SIZE	D	8.55	---	8.75
	E1	3.80	---	4.00
	E	5.80	---	6.20
LEAD PITCH	e	1.27 BSC		
	L	0.40	---	1.27
	h	0.25	---	0.50
	θ	0°	---	8°
	θ1	5°	---	15°
LEAD EDGE TOLERANCE	aaa	0.25		
LEAD OFFSET	bbb	0.25		
COPLANARITY	ccc	0.10		

Figure 9.3 SOP14 Package Shape and Dimension

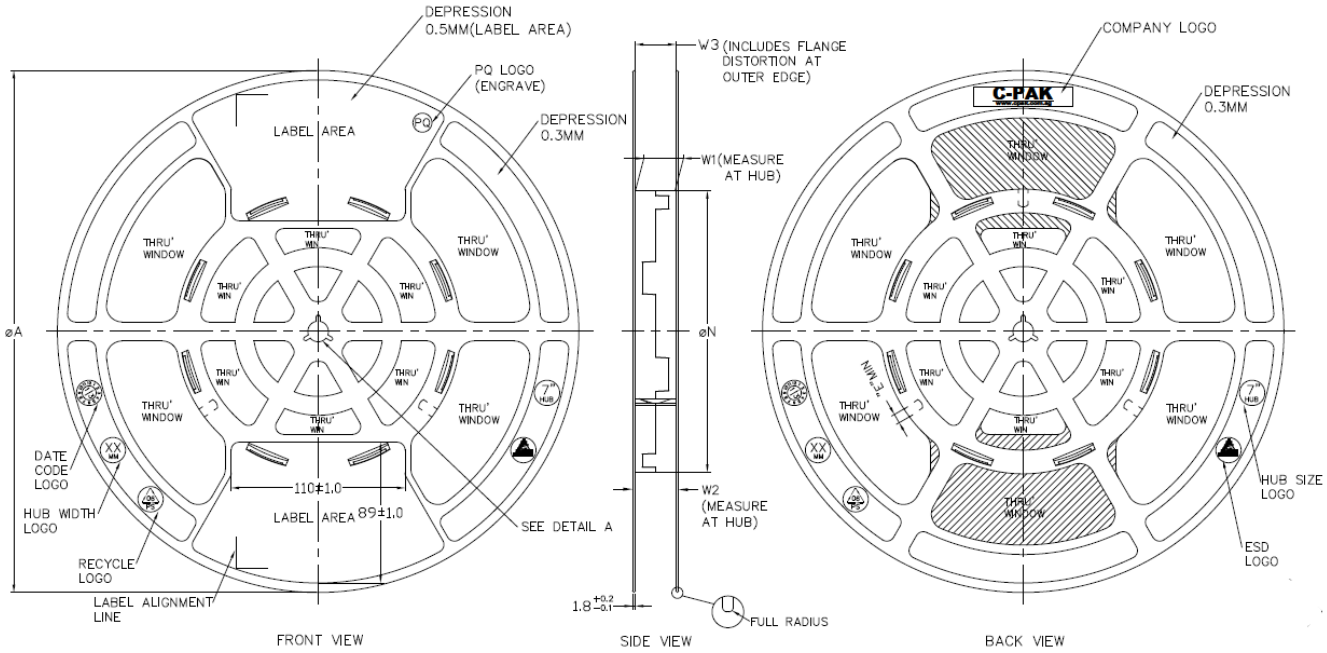
9. Ordering Information

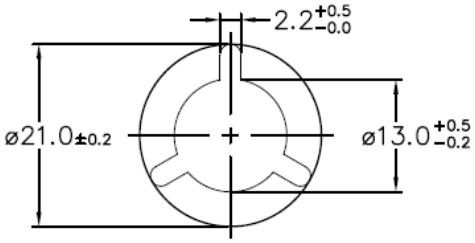
Part No.	*Temperature*	*Automotive*	*Package Type*	*Package Drawing*	*MSL*	*SPQ*
NSD1624-DLAR	-40 to 125℃	NO	LGA10	LGA10	TBD	TBD
NSD1624-DSPR	-40 to 125℃	NO	SOP8(150mil)	SOP8	TBD	TBD
NSD1624-DSPKR	-40 to 125℃	NO	SOP14(150mil)	SOP14	TBD	TBD

10. Documentation Support

Part Number	*Product Folder*	*Datasheet*	*Technical Documents*	*Isolator selection guide*
	Click here	Click here	Click here	Click here

11. Tape and Reel Information

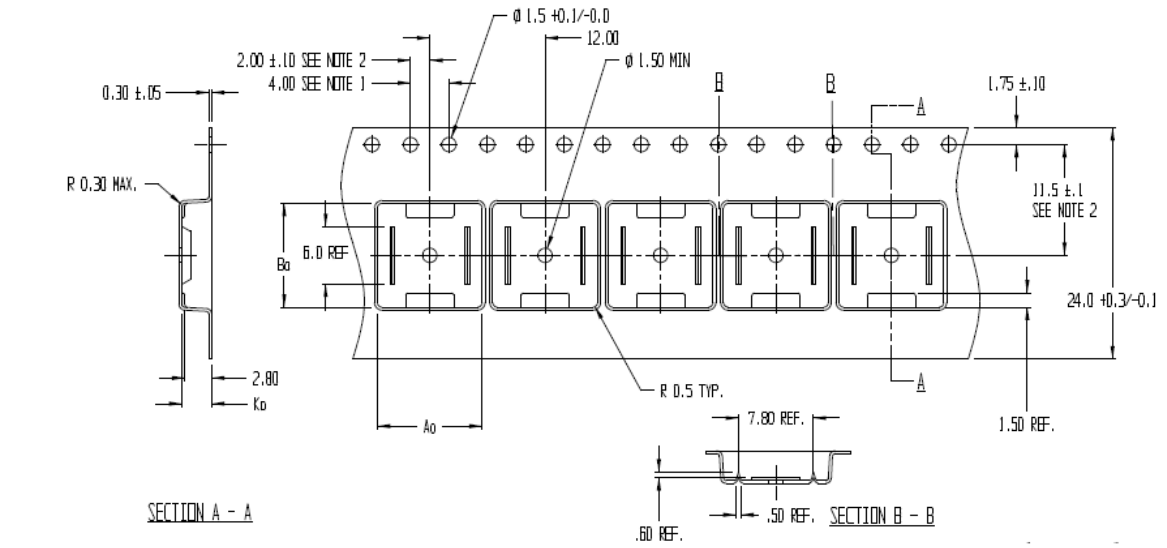




ARBOR HOLE
DETAIL A
SCALE : 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4 +1.5 −0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4 +2.0 −0.0	18.4		5.5
16MM	330	178	16.4 +2.0 −0.0	22.4		5.5
24MM	330	178	24.4 +2.0 −0.0	30.4		5.5
32MM	330	178	32.4 +2.0 −0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES



NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE
3. Ao AND Bo ARE CALCULATED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.

Ao = 10.90
Bo = 10.80
Ko = 3.1

Figure 12.1 Tape and Reel Information

12. Revision History

Revision	Description	Date
0.4	Initial version	2021/7/09