1. Product characteristics

- 100Mbps signal transmission rate
- Powerful isolation performance
  - ± 100kV / μ s CMTI (TYP)
  - 5kV$_{RMS}$isolation and withstand voltage
  - >50 years barrier life
  - Surge resistance up to 10kV
- wide power supply voltage range: 2.5V to 5.5V
- 2.5V to 5.5V level conversion
- A wide temperature range: - 40 ℃ to 125 ℃
- The default output high level (H) and low level (L) options
- Low propagation delay: 11ns (TYP value, 5V power supply)
- Low pulse width distortion: 3ns

2. application

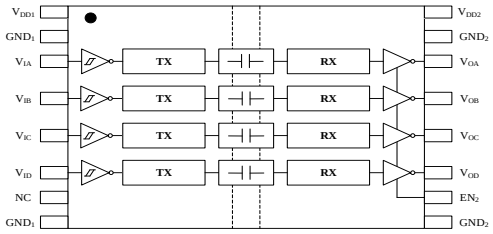
- Industrial automation
- motor control
- Photovoltaic inverter
- Separate the power supply
- medical equipment

3. summary

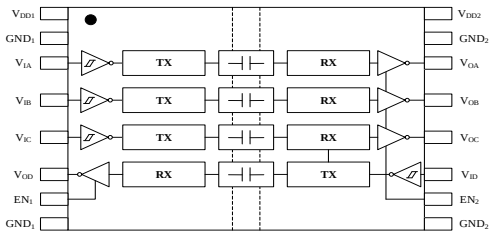
BL714x is a high performance four channel digital isolator, which can realize complete electrical isolation between input and output.$_2$gic input and output buffers of each isolation channel are isolated by a silicon dioxide insulated gate with double capacitors. The four data channels are completely independent. The input data can be encoded and recovered without distortion at the receiving end.BL7140 has four output channels on the same side;BL7141 has three forward channels and one reverse channel, and both sides have output enable;BL7142 has two forward channels and two reverse channels, and both sides have output enable.If the input side power or signal is lost, the device with suffix l will output low level by default, and the device with suffix h will output high level by default.

BL714x device has high insulation ability, which can provide high electromagnetic immunity and low radiation with low power consumption. It helps to prevent noise and surge on data bus or other circuits from entering local grounding terminal, thus interfering or damaging sensitive circuit. High CMTI capability can ensure the correct transmission of digital signal.BL714x device is packaged in 16 pin wide body SOIC (W) package, with 5kV$_{RMS}$isolation and withstand voltage capability.

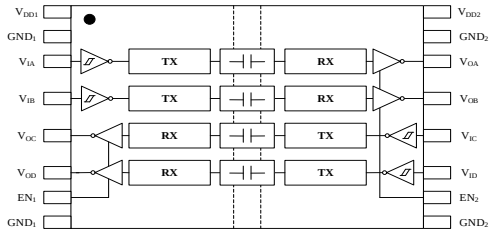
4. Principle block diagram



BL7140



BL7141



BL7142

Catalog

5. Product specifications

5.1 Absolute MAX rating[a]

PARAMETER	Min	MAX	UNIT
V_{DD1}, V_{DD2}supply voltage[b]	-0.5	6	V
V input / output voltage	-0.5	V_{DD}+0.5[c]	V
$I_O$output current	-20	20	mA
$T_J$junction temperature		150	℃
T_{STG}storage temperature range	-65	150	℃

Note:

[a]The stress beyond the absolute MAX rating may cause permanent damage to the device, and long-term operation at the absolute MAX rating may affect the reliability of the device.

[b]Except differential I / O bus voltage, all voltage values are voltage peaks relative to local grounding terminal (GND_1or GND_2).

[c]The MAX voltage shall not exceed 6V.

5.2 ESD rating

		VALUE	UNIT
V_{ESD}electrostatic discharge	Human body model (HBM) according to ANSI / ESDA / JEDEC js-001-	±6000	V
	Module charging mode (CDM) according to ANSI / ESDA / JEDEC js-	±1500	
	Machine mode (mm) according to jesd22-a115c	±400	

5.3 Recommended working conditions

PARAMETER		TYP		MAX	UNIT
V_{DD1}，V_{DD2} Power supply voltage		2.35		5.5	V
Under voltage threshold when $V_{DD(UVLO+)}$$V_{DD}$supply voltage rises			1.75	2.0	V
Under voltage threshold of $V_{DD(UVLO-)}$$V_{DD}$supply voltage drop		1.55	1.65		V
$V_{HYS(UVLO)}$$V_{DD}$hysteresis under voltage threshold		10	70	230	mV
I_{OH}high level output current	V_{DDO}[a]=5V	-4			mA
	V_{DDO}=3.3V	-2			
	V_{DDO}=2.5V	-1			
I_{OL}low level output current	V_{DDO}=5V			4	mA
	V_{DDO}=3.3V			2	
	V_{DDO}=2.5V			1	
V_{IH}input threshold logic high level		0.7 x V_{DDI}[a]		V_{DDI}	V
V_{IL}input threshold logic low level		0		0.25 x V_{DDI}	V
DR[b]signal transmission rate		0		100	Mbps
$_A$) ambient temperature		-40	25	125	℃

Note:

[a]V_{DDO}=output side;V_{DDI} = input side V_{DD}.

[b]Recommends a MAX speed of 100Mbps, which does not mean that the device can only work under 100Mbps.

5.4 Rated power

PARAMETER	TEST CONDITIONS	MAX	UNIT
BL7140			
Power consumption of P_D	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input 50 MHz 50% duty cycle square wave	260	mW
Power consumption of P_{D1}		52	mW
Power consumption of P_{D2}		208	mW
BL7141			
Power consumption of P_D	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input 50 MHz 50% duty cycle square wave	260	mW
Power consumption of P_{D1}		98	mW
Power consumption of P_{D2}		162	mW
BL7142			
Power consumption of P_D	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input 50 MHz 50% duty cycle square wave	260	mW
Power consumption of P_{D1}		130	mW
Power consumption of P_{D2}		130	mW

5.5 Isolation characteristics

PARAMETER	TEST CONDITIONS	VALUE	UNIT
CLR outer clearance a	MAX distance between input and output	8	mm
CpG external creepage	The shortest distance from the input end to the	8	mm
DTI isolation distance	MAX internal clearance	18	μm
CTI relative leakage index	According to DIN IEC UL etc,	>600	V
V_{IORM} max repetitive peak	AC voltage (bipolar)	2121	V_{PK}
V_{IOWM} MAX working isolation voltage	AC voltage	1500	V_{RMS}
	DC voltage	2121	V_{DC}
V_{IOTM} MAX transient isolation voltage	V_{TEST}= V_{IOTM}，t=60s	8000	V_{PK}
V_{IOSM} MAX surge isolation	1.2/50μ$_{IOSM}$orm, V (m298) = 1.6 x V (m296)	7000	V_{PK}
V_{ISO} MAX isolation voltage	V (m298) = V_{ISO}, t = 60s (certification), V_{TEST}= 1.2×V_{ISO}, t = 1s (100% product test)	5	kV_{RMS}

Note:

[a]Creepage distance and clearance PARAMETERs are selected according to the specific equipment isolation standard.Pay attention to the creepage distance and gap distance of the circuit board design to ensure that the isolator pad on the printed circuit board does not reduce the distance.In some cases, the creepage distance and clearance on the printed circuit board are equal.The use of grooves and other technologies on printed circuit boards can help to improve these indicators.

5.6 Electrical characteristics – 5V

V_{DD1}= V_{DD2}= 5V ± 10% (all PARAMETERs were measured in the recommended working environment, unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH} High-level output voltage	I_{OH}=-4mA;Figure 7-1	V_{DDO}[a]-0.4	4.8		V
V_{OL} Low-level output voltage	I_{OL}=4mA;Figure 7-1		0.2	0.3	V
$V_{IT+(IN)}$Rising input voltag threshold			0.65 x V_{DDI}	0.7 x V_{DDI}	V
$V_{IT-(IN)}$Falling input voltage threshold		0.3 x V_{DDI}	0.4 x V_{DDI}		V
$V_{I(HYS)}$Input threshold voltage hysteresis			1.24		V
I_{IH} High-level input current	V_{DD1} at INX or ENX			5	μA
I_{IL} Low-level input current	0V at INX or ENX	-10			μA
$Z_O$output impedance	Z_O=V_{OL}/I_{OL}		43		Ω
CMTI Common-mode transient	Figure 7-2	80	100		kV/μs

Note:

[a]V_{DDO}=output side;V_{DDI} = input side V_{DD}.

[b]INX = input, ENX = output enable.

5.7 Electrical characteristics – 3.3V

V_{DD1}= V_{DD2}= 3.3V ± 10% (all PARAMETERs are measured in the recommended working environment, unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH} High-level output voltage	I_{OH}=-2mA;Figure 7-1	V_{DDO}[a] -0.3	3.2		V
V_{OL} Low-level output voltage	I_{OL}=2mA;Figure 7-1		0.06	0.1	V
$V_{IT+(IN)}$Rising input voltag threshold			0.65 x V_{DDI}	0.7 x V_{DDI}	V
$V_{IT-(IN)}$Falling input voltage threshold		0.3 x V_{DDI}	0.4 x V_{DDI}		V
$V_{I(HYS)}$Input threshold voltage			0.9		V
I_{IH} High-level input current	V_{DD1} at INX or ENX			5	μA
I_{IL} Low-level input current	0V at INX or ENX	-10			μA
$Z_O$output impedance	Z_O=V_{OL}/I_{OL}		30		Ω
CMTI Common-mode transient	Figure 7-2	80	100		kV/μs

Note:

[a]V_{DDO}=output side;V_{DDI} = input side V_{DD}.

[b]INX = input, ENX = output enable.

5.8 Electrical characteristics – 2.5V

V_{DD1}= V_{DD2}= 2.5V ± 10% (all PARAMETERs measured in recommended working environment, unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH} High-level output voltage	I_{OH}=-1mA;Figure 7-1	V_{DDO}[a]-0.2	2.45		V
V_{OL} Low-level output voltage	I_{OL}=1mA;Figure 7-1		0.03	0.05	V
$V_{IT+(IN)}$Rising input voltag threshold			0.65 x V_{DDI}	0.7 x V_{DDI}	V
$V_{IT-(IN)}$Falling input voltage threshold		0.25 x V_{DDI}	0.35 x V_{DDI}		V
$V_{I(HYS)}$Input threshold voltage			0.85		V
I_{IH} High-level input current	V_{DD1} at INX or ENX			5	μA
I_{IL} Low-level input current	0V at INX or ENX	-10			μA
$Z_O$output impedance	Z_O=V_{OL}/I_{OL}		34		Ω
CMTI Common-mode transient	Figure 7-2	80	100		kV/μs

Note:

[a]V_{DDO}=output side;V_{DDI} = input side V_{DD}.

[b]INX = input, ENX = output enable.

5.9 Power supply current characteristic – 5V

V_{DD1}= V_{DD2}= 5V ± 10% (all PARAMETERs were measured in the recommended working environment, unless otherwise specified)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	TYP	MAX	UNIT
BL7140						
Turn off the power supply	EN_2=0V; V_I=0V(BL7140WL) V_I=V_{DD1}（BL7140WH）		I_{DD1}	1.8	2.0	mA
			I_{DD2}	0.4	0.6	
	EN_2=0V; V_I= V_{DD1}(BL7140WL) V_I=0V（BL7140WH）		I_{DD1}	8.2	9.7	
			I_{DD2}	0.4	0.6	
DC power supply	EN_2= V_{DD2} ;V_I=0V(BL7140WL) V_I=V_{DD1}（BL7140WH）		I_{DD1}	1.8	2.0	
			I_{DD2}	3.0	4.2	
	EN_2= V_{DD2} ;V_I=V_{DD1}(BL7140WL) V_I=0V(BL7140WH)		I_{DD1}	8.2	9.7	
			I_{DD2}	3.2	4.4	
Power supply current - AC signal	All channels input 50% duty cycle square wave, each channel C_L= 15 PF	2Mbps (1MHz)	I_{DD1}	5.7	6.9	
			I_{DD2}	4.5	5.7	
		10Mbps (5MHz)	I_{DD1}	5.6	6.9	
			I_{DD2}	6.8	7.8	
		100Mbps (50MHz)	I_{DD1}	5.8	6.9	
			I_{DD2}	24.8	29.3	
BL7141						
Turn off the power supply	EN_1=EN_2=0V; V_I=0V(BL7141WL) V_I=V_{DDI}[a]（BL7141WH）		I_{DD1}	1.6	2.1	mA
			I_{DD2}	1.2	1.6	
	EN_1=EN_2=0V; V_I= V_{DDI}(BL7141WL) V_I=0V（BL7141WH）		I_{DD1}	7.6	9.2	
			I_{DD2}	3.2	4.1	
DC power supply	EN_1=EN_2= V_{DDI} ;V_I=0V(BL7141WL) V_I=VDDI（BL7141WH）		I_{DD1}	2.6	3.5	
			I_{DD2}	3.4	4.2	
	EN1=EN2=VDDI ;VI=VDDI(BL7141WL) V_I=0V（BL7141WH）		I_{DD1}	8.1	9.6	
			I_{DD2}	5.9	7.5	
Power supply current - AC signal	All channels input 50% duty cycle square wave, each channel C_L= 15 PF	2Mbps (1MHz)	I_{DD1}	5.7	6.9	
			I_{DD2}	4.9	6.1	
		10Mbps (5MHz)	I_{DD1}	5.8	7.0	
			I_{DD2}	6.5	7.5	
		100Mbps (50MHz)	I_{DD1}	9.8	12.3	
			I_{DD2}	19.8	22.3	
BL7142						
Turn off the power supply	EN_1=EN_2=0V; V_I=0V(BL7142WL) V_I=V_{DDI}（BL7142WH）		I_{DD1}	1.4	1.6	mA
			I_{DD2}	1.4	1.6	
	EN_1=EN_2=0V; V_I= V_{DDI} (BL7142WL) V_I=0V（BL7142WH）		I_{DD1}	5.4	6.0	
			I_{DD2}	5.4	6.0	
DC power supply	EN_1=EN_2= V_{DDI} ;V_I=0V(BL7142WL) V_I=V_{DDI}（BL7142WH）		I_{DD1}	3.1	4.2	
			I_{DD2}	3.1	4.2	
	EN_1=EN_2= V_{DDI} ;V_I=V_{DDI}(BL7142WL) V_I=0V（BL7142WH）		I_{DD1}	7.2	8.4	
			I_{DD2}	7.2	8.4	
Power supply current - AC signal	All channels input 50% duty cycle square wave, each channel CL = 15 PF	2Mbps (1MHz)	I_{DD1}	5.3	6.5	
			I_{DD2}	5.3	6.5	
		10Mbps (5MHz)	I_{DD1}	6.2	7.2	
			I_{DD2}	6.2	7.2	
		100Mbps (50MHz)	I_{DD1}	14.8	17.3	
			I_{DD2}	14.8	17.3	

Note:

[a] V_{DDI} = input side V_{DD}.

5.10 Power supply current characteristic – 3.3V

V_{DD1}= V_{DD2}= 3.3V ± 10% (all PARAMETERs are measured in the recommended working environment, unless otherwise specified)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	TYP	MAX	UNIT
BL7140						
Turn off the power supply	EN_2=0V; V_I=0V(BL7140WL) V_I=V_{DD1}（BL7140WH）		I_{DD1}	1.8	2.0	mA
			I_{DD2}	0.4	0.6	
	EN_2=0V; V_I= V_{DD1}(BL7140WL) V_I=0V（BL7140WH）		I_{DD1}	8.2	9.7	
			I_{DD2}	0.4	0.6	
DC power supply	EN_2= V_{DD2} ;V_I=0V(BL7140WL) V_I=V_{DD1}（BL7140WH）		I_{DD1}	1.8	2.0	
			I_{DD2}	3.0	4.2	
	EN_2= V_{DD2} ;V_I=V_{DD1}(BL7140WL) V_I=0V(BL7140WH)		I_{DD1}	8.2	9.7	
			I_{DD2}	3.2	4.4	
Power supply current - AC signal	All channels input 50% duty cycle square wave, each channel C_L= 15 PF	2Mbps (1MHz)	I_{DD1}	5.7	6.9	
			I_{DD2}	4.5	5.7	
		10Mbps (5MHz)	I_{DD1}	5.3	6.6	
			I_{DD2}	6.5	7.5	
		100Mbps (50MHz)	I_{DD1}	4.8	6.2	
			I_{DD2}	20.8	24.3	
BL7141						
Turn off the power supply	EN_1=EN_2=0V; V_I=0V(BL7141WL) V_I=V_{DDI}[a]（BL7141WH）		I_{DD1}	1.6	2.1	mA
			I_{DD2}	1.2	1.6	
	EN_1=EN_2=0V; V_I= V_{DDI}(BL7141WL) V_I=0V（BL7141WH）		I_{DD1}	7.6	9.2	
			I_{DD2}	3.2	4.1	
DC power supply	EN_1=EN_2= V_{DDI} ;V_I=0V(BL7141WL) V_I=V_{DDI}（BL7141WH）		I_{DD1}	2.6	3.5	
			I_{DD2}	3.4	4.2	
	EN1=EN2=V_{DDI} ;VI=V_{DDI}(BL7141WL) V_I=0V（BL7141WH）		I_{DD1}	8.1	9.6	
			I_{DD2}	5.9	7.5	
Power supply current - AC signal	All channels input 50% duty cycle square wave, each channel C_L= 15 PF	2Mbps (1MHz)	I_{DD1}	5.7	6.9	
			I_{DD2}	4.9	6.1	
		10Mbps (5MHz)	I_{DD1}	5.5	6.7	
			I_{DD2}	6.1	7.1	
		100Mbps (50MHz)	I_{DD1}	8.4	10.8	
			I_{DD2}	17.2	20.3	
BL7142						
Turn off the power supply	EN_1=EN_2=0V; V_I=0V(BL7142WL) V_I=V_{DDI}（BL7142WH）		I_{DD1}	1.4	1.6	mA
			I_{DD2}	1.4	1.6	
	EN_1=EN_2=0V; V_I= V_{DDI} (BL7142WL) V_I=0V（BL7142WH）		I_{DD1}	5.4	6.0	
			I_{DD2}	5.4	6.0	
DC power supply	EN_1=EN_2= V_{DDI} ;V_I=0V(BL7142WL) V_I=V_{DDI}（BL7142WH）		I_{DD1}	3.1	4.2	
			I_{DD2}	3.1	4.2	
	EN_1=EN_2= V_{DDI} ;V_I=V_{DDI}(BL7142WL) V_I=0V（BL7142WH）		I_{DD1}	7.2	8.4	
			I_{DD2}	7.2	8.4	
Power supply current - AC signal	All channels input 50% duty cycle square wave, each channel CL = 15 PF	2Mbps (1MHz)	I_{DD1}	5.3	6.2	
			I_{DD2}	5.3	6.2	
		10Mbps (5MHz)	I_{DD1}	5.8	7.1	
			I_{DD2}	5.8	7.1	
		100Mbps (50MHz)	I_{DD1}	12.9	15.2	
			I_{DD2}	12.9	15.2	

Note:

[a] V_{DDI} = input side V_{DD}.

5.11 Current characteristics of 2.5V power supply

V_{DD1}= V_{DD2}= 2.5V ± 10% (all PARAMETERs measured in recommended working environment, unless otherwise specified)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	TYP	MAX	UNIT
BL7140						
Turn off the power supply	EN_2=0V; V_I=0V(BL7140WL) V_I=V_{DD1}（BL7140WH）		I_{DD1}	1.8	2.0	mA
			I_{DD2}	0.4	0.6	
	EN_2=0V; V_I= V_{DD1}(BL7140WL) V_I=0V（BL7140WH）		I_{DD1}	8.2	9.7	
			I_{DD2}	0.4	0.6	
DC power supply	EN_2= V_{DD2} ;V_I=0V(BL7140WL) V_I=V_{DD1}（BL7140WH）		I_{DD1}	1.8	2.0	
			I_{DD2}	3.0	4.2	
	EN_2= V_{DD2} ;V_I=V_{DD1}(BL7140WL) V_I=0V(BL7140WH)		I_{DD1}	8.2	9.7	
			I_{DD2}	3.2	4.4	
Power supply current - AC signal	All channels input 50% duty cycle square wave, each channel C_L= 15 PF	2Mbps (1MHz)	I_{DD1}	5.8	7.0	
			I_{DD2}	4.6	5.8	
		10Mbps (5MHz)	I_{DD1}	5.2	6.5	
			I_{DD2}	6.2	7.2	
		100Mbps (50MHz)	I_{DD1}	4.4	5.9	
			I_{DD2}	18.2	22.3	
BL7141						
Turn off the power supply	EN_1=EN_2=0V; V_I=0V(BL7141WL) V_I=V_{DDI}[a]（BL7141WH）		I_{DD1}	1.6	2.1	mA
			I_{DD2}	1.2	1.6	
	EN_1=EN_2=0V; V_I= V_{DDI}(BL7141WL) V_I=0V（BL7141WH）		I_{DD1}	7.6	9.2	
			I_{DD2}	3.2	4.1	
DC power supply	EN_1=EN_2= V_{DDI} ;V_I=0V(BL7141WL) V_I=V_{DDI}（BL7141WH）		I_{DD1}	2.6	3.5	
			I_{DD2}	3.4	4.2	
	EN1=EN2=V_{DDI} ;VI=V_{DDI}(BL7141WL) V_I=0V（BL7141WH）		I_{DD1}	8.1	9.6	
			I_{DD2}	5.9	7.5	
Power supply current - AC signal	All channels input 50% duty cycle square wave, each channel C_L= 15 PF	2Mbps (1MHz)	I_{DD1}	5.6	6.9	
			I_{DD2}	4.8	6.1	
		10Mbps (5MHz)	I_{DD1}	5.4	6.5	
			I_{DD2}	6.0	7.1	
		100Mbps (50MHz)	I_{DD1}	7.8	10.3	
			I_{DD2}	14.8	18.3	
BL7142						
Turn off the power supply	EN_1=EN_2=0V; V_I=0V(BL7142WL) V_I=V_{DDI}（BL7142WH）		I_{DD1}	1.4	1.6	mA
			I_{DD2}	1.4	1.6	
	EN_1=EN_2=0V; V_I= V_{DDI} (BL7142WL) V_I=0V（BL7142WH）		I_{DD1}	5.4	6.0	
			I_{DD2}	5.4	6.0	
DC power supply	EN_1=EN_2= V_{DDI} ;V_I=0V(BL7142WL) V_I=V_{DDI}（BL7142WH）		I_{DD1}	3.1	4.2	
			I_{DD2}	3.1	4.2	
	EN_1=EN_2= V_{DDI} ;V_I=V_{DDI}(BL7142WL) V_I=0V（BL7142WH）		I_{DD1}	7.2	8.4	
			I_{DD2}	7.2	8.4	
Power supply current - AC signal	All channels input 50% duty cycle square wave, each channel CL = 15 PF	2Mbps (1MHz)	I_{DD1}	5.2	6.4	
			I_{DD2}	5.2	6.4	
		10Mbps (5MHz)	I_{DD1}	5.7	6.8	
			I_{DD2}	5.7	6.8	
		100Mbps (50MHz)	I_{DD1}	11.3	13.2	
			I_{DD2}	11.3	13.2	

Note:

[a] V_{DDI} = input side V_{DD}.

5.12 Timing characteristics – 5V

V_{DD1}= V_{DD2}= 5V ± 10% (all PARAMETERs were measured in the recommended working environment, unless otherwise specified)

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
T_{PLH}, t_{PHL}propagation delay time		Figure 7-1	7	11	ns
PWD pulse width distortion | t_{PLH} – t_{PHL}|			0.2	3	ns
$T_{sk(pp)}$inter chip output offset time[a]				4.5	ns
$T_r$output signal rise time		Figure 7-1	1.9	2.4	ns
$T_f$output signal decline time			1.9	2.4	ns
T_{PHZ}turn off enable propagation delay, output high level to			20	28	ns
T_{PLZ}turn off enable propagation delay, output low level to			18	24	ns
T_{PZH}enables the propagation delay, and outputs the time from high impedance to high output level	BL714xWL		1.3	2	μs
	BL714xWH		7	13	ns
T_{PZL}enables the propagation delay and outputs the time from high impedance to low output level	BL714xWL		7	13	ns
	BL714xWH		1.3	2	μs

Note:

[a]$t_{sk(pp)}$is the difference of propagation delay time between different chips input in the same direction under the same supply voltage, temperature, input signal and load.

5.13 Timing characteristics – 3.3V

V_{DD1}= V_{DD2}= 3.3V ± 10% (all PARAMETERs are measured in the recommended working environment, unless otherwise specified)

PARAMETER		TEST CONDITIONS		TYP	MAX	UNIT
T_{PLH}, t_{PHL}propagation delay time		Figure 7-1	7	11	15	ns
PWD pulse width distortion | t_{PLH} – t_{PHL}|				0.2	3	ns
$T_{sk(pp)}$inter chip output offset time[a]					4.5	ns
$T_r$output signal rise time		Figure 7-1		1.9	2.4	ns
$T_f$output signal decline time				1.9	2.4	ns
T_{PHZ}turn off enable propagation delay, output high level to				25	32	ns
T_{PLZ}turn off enable propagation delay, output low level to				8	14	ns
T_{PZH}enables the propagation delay, and outputs the time from high impedance to high output level	BL714xWL			1.2	2	μs
	BL714xWH			10	15	ns
T_{PZL}enables the propagation delay and outputs the time from high impedance to low output level	BL714xWL			10	15	ns
	BL714xWH			1.2	2	μs

Note:

[a]$t_{sk(pp)}$is the difference of propagation delay time between different chips input in the same direction under the same supply voltage, temperature, input signal and load.

5.14 Timing characteristics – 2.5V

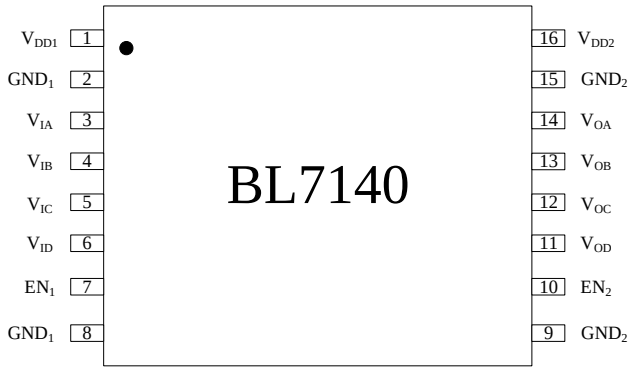
V_{DD1}= V_{DD2}= 2.5V ± 10% (all PARAMETERs measured in recommended working environment, unless otherwise specified)

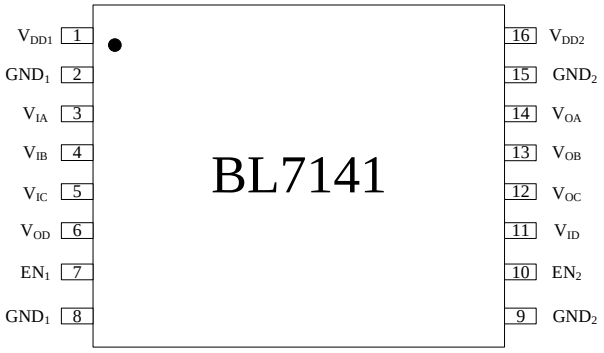
PARAMETER		TEST CONDITIONS		TYP	MAX	UNIT
T_{PLH}, t_{PHL}propagation delay time		Figure 7-1	9	13	17	ns
PWD pulse width distortion | t_{PLH} – t_{PHL}|				0.2	3	ns
$T_{sk(pp)}$inter chip output offset time[a]					4.5	ns
$T_r$output signal rise time		Figure 7-1		1.9	2.4	ns
$T_f$output signal decline time				1.9	2.4	ns
T_{PHZ}turn off enable propagation delay, output high level to				31	37	ns
T_{PLZ}turn off enable propagation delay, output low level to				10	15	ns
T_{PZH}enables the propagation delay, and outputs the time from high impedance to high output level	BL714xWL			1.2	2	μs
	BL714xWH			16	22	ns
T_{PZL}enables the propagation delay and outputs the time from high impedance to low output level	BL714xWL			16	22	ns
	BL714xWH			1.2	2	μs

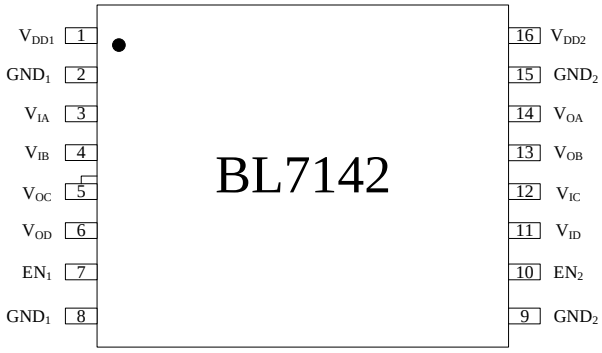
Note:

[a]$t_{sk(pp)}$is the difference of propagation delay time between different chips input in the same direction under the same supply voltage, temperature, input signal and load.

6. Pin function description

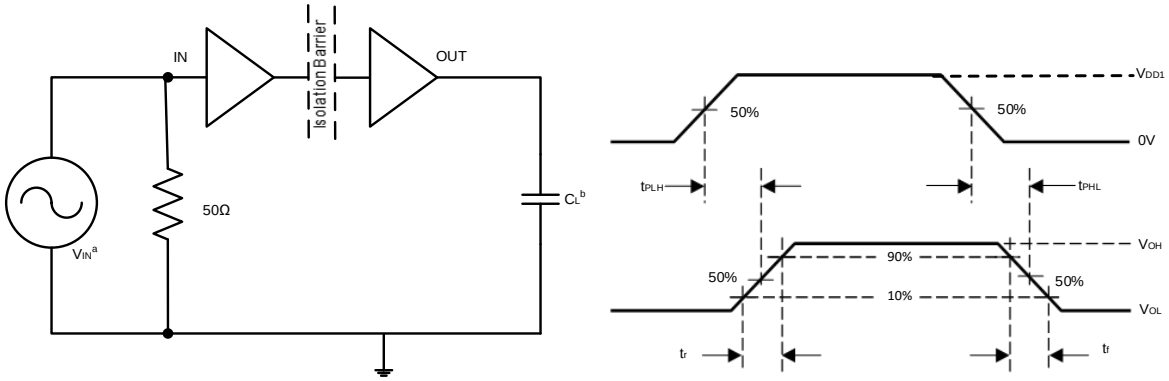






Pin number	Pin name	Function description
1	V_{DD1}	1 side power supply
2	GND_1	1 side reference ground
3	V_{IA}	Channel a input
4	V_{IB}	Channel B input
5	V_{IC}/V_{OC}	C channel input / C channel output
6	V_{ID}/V_{OD}	Input / D channel
7	NC/EN_1	No internal connection / 1 side enable high level
8	GND_1	1 side reference ground
9	GND_2	2-side reference ground
10	EN_2	2 side enable high level active or floating
11	V_{OD}/V_{ID}	D-channel output / D-channel input
12	V_{OC}/V_{IC}	Input / C channel
13	V_{OB}	B channel output
14	V_{OA}	A channel output
15	GND_2	2-side reference ground
16	V_{DD2}	2-side power supply

7. PARAMETER information measurement

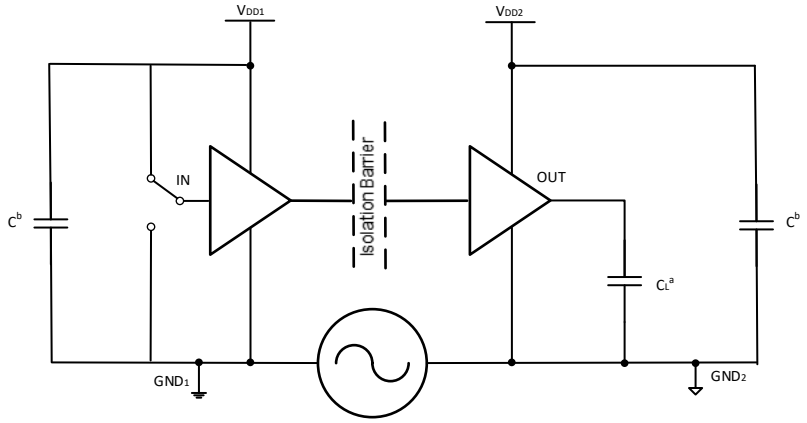


Note:

[a]signal generator provides input pulse with PRR ⩽ 50 kHz, duty cycle 50%, tr ⩽ 3 ns,⩽ 3 ns, Z= 50 Ω.The 50 Ω resistor in the figure is used to match the output impedance of signal generator, which is not needed in practical application.

[b]C_L= 15pF, including load capacitance and instrument capacitance.

Figure 7-1 timing characteristic test circuit and voltage waveform



Note:

[a]C_L= 15pF, including load capacitance and instrument capacitance.

[b]C is 0.1μBypass capacitance of F.

Figure 7-2 CMTI common mode transient immunity test circuit

8. Truth table

V_{DDI}	V_{DDO}	Input INX	Output enable ENX	Output outx	pattern
PU	PU	H	H or open	H	Normal operation mode: The state of its input and output channels follows
		L	H or open	L	
		Open	H or open	default	Default output mode: (L suffix is low, H suffix is high) If the input remains disconnected, the output remains at its default value
X	PU	X	L	Z	High impedance mode: If the output enable is connected to a low level, the output will be in a high resistance state
PD	PU	X	H or open	default	Default output mode: (L suffix is low, H suffix is high) $_{DDIa}$fault) if not power on
X	PD	X	X	uncertain	If $V_{DDOa}$is not energized, the output status is uncertain

Note:

[a]V_{DDO}=output side;V_{DDI} = input side V_{DD}.

[b]H is high level, l is low level, Z is high resistance, X is any level.

9. Reference circuit

Unlike optocouplers, external components are required to improve performance, provide bias, or limit current.

BL714x Series Digital Isolators only need two external V_{DD}bypass capacitors to work.

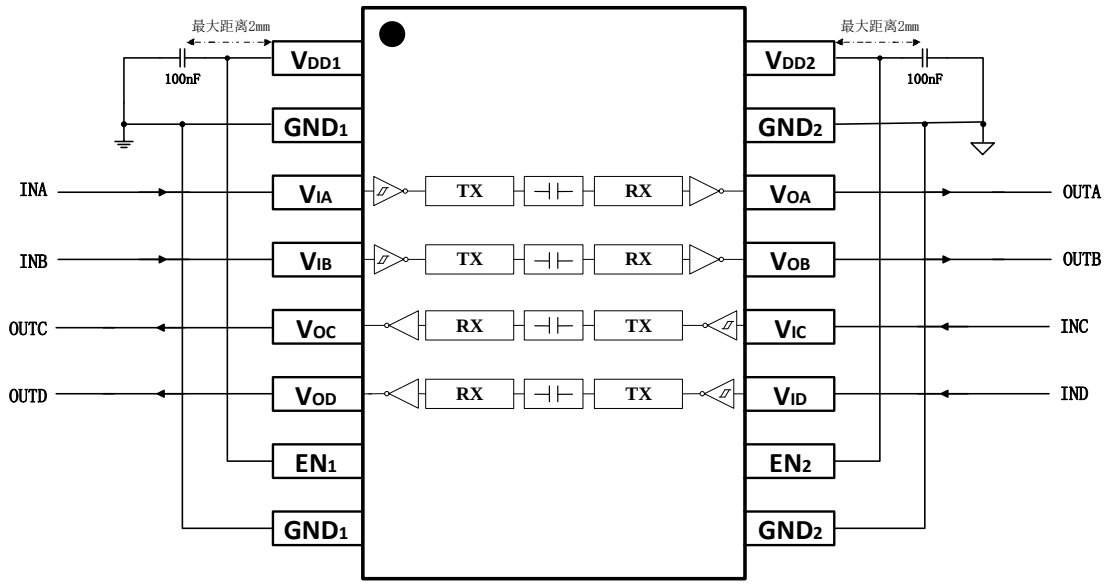


Figure 9-1 TYP application circuit of BL7142

10. Encapsulation information

10.1 SOIC-16 wide (W)

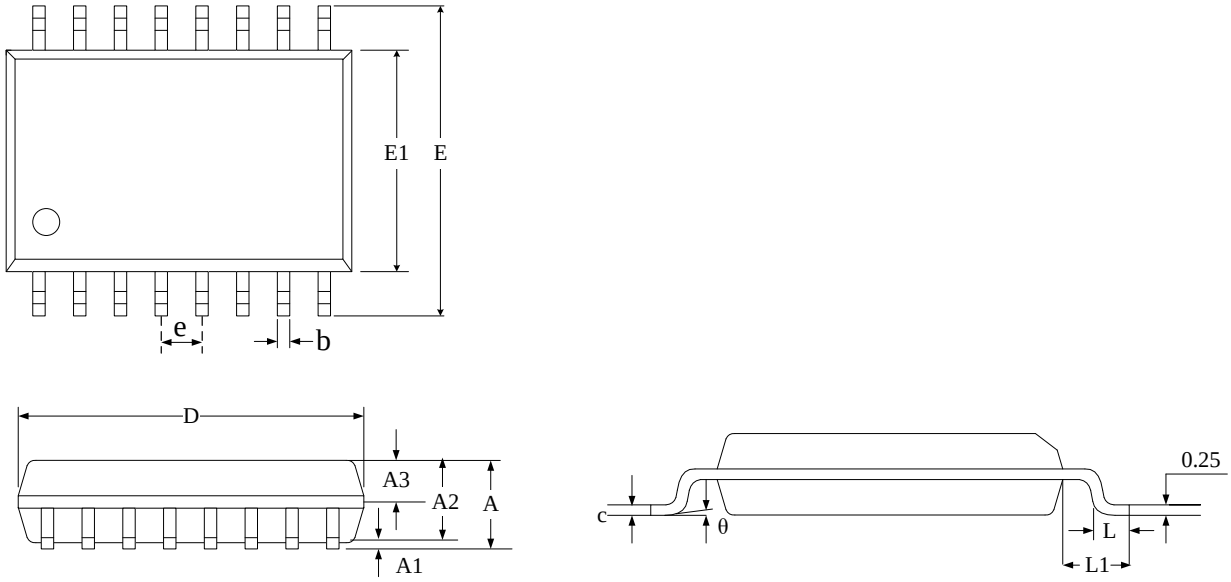


Figure 10-1 outline of SOIC-16 wide body package

Symbol	Size (mm)		
	MAX	nominal	MAX
A	—	—	2.65
A1	0.1	—	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	—	0.44
c	0.25	—	0.31
D	10.10	10.30	10.50
E	10.26	10.41	10.60
E1	7.30	7.50	7.70
e		1.27BSC	
L	0.55	—	0.85
L1		1.40BSC	
θ	0		8°

11. Ordering Guide

model	rate	Number	Forward /	Rated	Default level	encapsulation
BL7140WL	100Mbps	4	4/0	5000Vrms	low	SOIC-16 wide
BL7140WH	100Mbps	4	4/0	5000Vrms	high	SOIC-16 wide
BL7141WL	100Mbps	4	3/1	5000Vrms	low	SOIC-16 wide
BL7141WH	100Mbps	4	3/1	5000Vrms	high	SOIC-16 wide
BL7142WL	100Mbps	4	2/2	5000Vrms	low	SOIC-16 wide
BL7142WH	100Mbps	4	2/2	5000Vrms	high	SOIC-16 wide