SN74HC4066 Quadruple Bilateral Analog Switch

1 Features

- Wide Operating Voltage Range of 2 V to 6 V
- Typical Switch Enable Time of 18 ns
- Low Power Consumption, 20-µA Maximum I_{CC}
- Low Input Current of 1 µA Maximum
- High Degree of Linearity
- High On-Off Output-Voltage Ratio
- Low Crosstalk Between Switches
- Low On-State Impedance: 50-Ω Typical at V_{CC} = 6 V
- Individual Switch Controls

2 Applications

- Analog Signal Switching/Multiplexing:
  - Signal Gating, Modulator, Squelch Control, Demodulator, Chopper, Commutating Switch
- Digital Signal Switching/Multiplexing
  - Audio and Video Signal Routing
- Transmission-Gate Logic Implementation
- Analog-to-Digital and Digital-to-Analog Conversion
- Digital Control of Frequency, Impedance, Phase, and Analog-Signal Gain
- Motor Speed Control
- Battery Chargers
- DC-DC Converter

3 Description

The SN74HC4066 device is a silicon-gate CMOS quadruple analog switch designed to handle both analog and digital signals. Each switch permits signals with amplitudes of up to 6 V (peak) to be transmitted in either direction.

Each switch section has its own enable input control (C). A high-level voltage applied to C turns on the associated switch section.

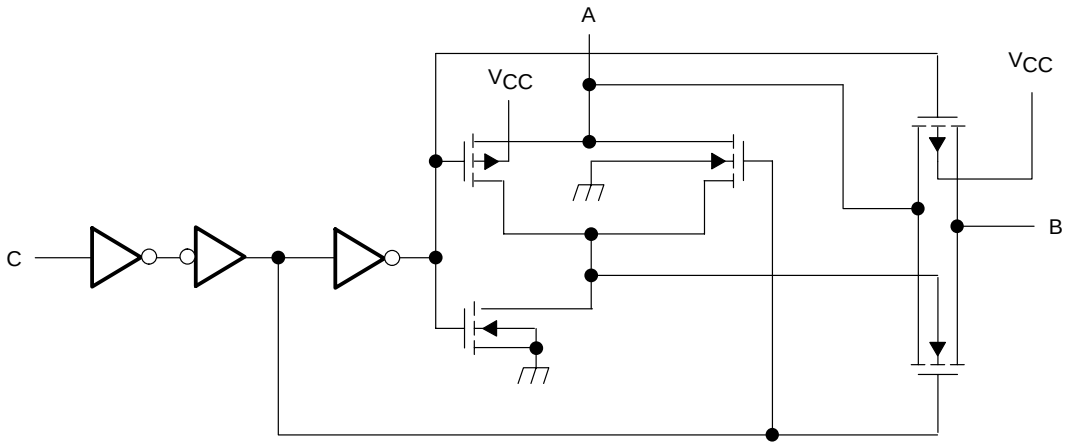
Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

Device Information(1)

PART NUMBER	PACKAGE (PINS)	BODY SIZE (NOM)
SN74HC4066D	SOIC (14)	8.65 mm × 3.91 mm
SN74HC4066DB	SSOP (14)	6.20 mm × 5.30 mm
SN74HC4066PW	TSSOP (14)	5..00 mm × 4.40 mm
SN74HC4066N	PDIP (14)	19.30 mm × 6.35 mm
SN74HC4066NS	SO (14)	10.30 mm × 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram, Each Switch (Positive Logic)



One of Four Switches

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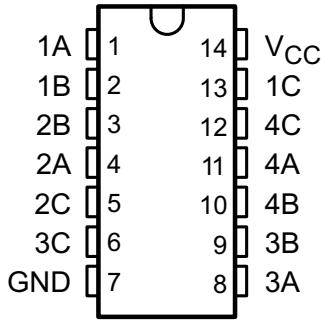
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (July 2003) to Revision H	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted *Ordering Information* table, see POA at the end of the datasheet.	1

5 Pin Configuration and Functions

D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	1A	I/O	Switch 1 input/output
2	1B	I/O	Switch 1 output/input
3	2B	I/O	Switch 2 output/input
4	2A	I/O	Switch 2 input/output
5	2C	I	Switch 2 control
6	3C	I	Switch 3 control
7	GND	—	Ground
8	3A	I/O	Switch 1 input/output
9	3B	I/O	Switch 1 output/input
10	4B	I/O	Switch 1 output/input
11	4A	I/O	Switch 1 input/output
12	4C	I	Switch 3 control
13	1C	I	Switch 1 control
14	V_{CC}	—	Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		–0.5	7	V
I_I	Control-input diode current	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I_I	I/O port diode current	$V_I < 0$ or $V_{I/O} > V_{CC}$		±20	mA
	On-state switch current	$V_{I/O}$ = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground unless otherwise specified.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. CDM value for N package only.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2 (2)	5	6	V
$V_{I/O}$	I/O port voltage		0		V_{CC}	V
V_{IH}	High-level input voltage, control inputs	V_{CC} = 2 V	1.5		V_{CC}	V
		V_{CC} = 4.5 V	3.15		V_{CC}	
		V_{CC} = 6 V	4.2		V_{CC}	
V_{IL}	Low-level input voltage, control inputs	V_{CC} = 2 V	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	
		V_{CC} = 6 V	0		1.2	
$\Delta t/\Delta v$	Input transition rise and fall time	V_{CC} = 2 V			1000	ns
		V_{CC} = 4.5 V			500	
		V_{CC} = 6 V			400	
T_A	Operating free-air temperature		–40		85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).
(2) With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

6.4 Thermal Information

THERMAL METRIC (1)		SN74HC4066					UNIT
		D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	89.4	103.6	53.2	87.6	118.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.5	55.6	40.5	45.4	47.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.6	50.8	33.1	46.3	60.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	17.2	21	25.3	15.8	5.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	43.4	50.3	33	46	59.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_A = –40 to +85 °C unless otherwise specified.

PARAMETER			TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
r_{on}	On-state switch resistance		I_T = –1 mA, V_I = 0 to V_{CC}, V_C = V_{IH} (see Figure 2)	T_A = 25 C	2 V		150		Ω
				T_A = 25 C	4.5 V		50	85	
				T_A = –40 to +85				106	
				T_A = 25 C	6 V		30		
$r_{on(p)}$	Peak on-state resistance		V_I = V_{CC} or GND, V_C = V_{IH}, I_T = –1 mA	T_A = 25 C	2 V		320		Ω
				T_A = 25 C	4.5 V		70	170	
				T_A = –40 to +85				215	
				T_A = 25 C	6 V		50		
I_I	Control input current		V_C = 0 or V_{CC}	T_A = –40 to +85	6 V		±0.1	±100	nA
				T_A = 25 C				±1000	
I_{soff}	Off-state switch leakage current		V_I = V_{CC} or 0, V_O = V_{CC} or 0, V_C = V_{IL} (see Figure 3)	T_A = –40 to +85	6 V			±0.1	µA
				T_A = 25 C				±5	
I_{son}	On-state switch leakage current		V_I = V_{CC} or 0, V_C = V_{IH} (see Figure 4)	T_A = –40 to +85	6 V			±0.1	µA
				T_A = 25 C				±5	
I_{CC}	Supply current		V_I = 0 or V_{CC}, I_O = 0	T_A = –40 to +85	6 V			2	µA
				T_A = 25 C				20	
C_i	Input capacitance	A or B	T_A = 25 C		5 V		9		pF
		C	T_A = –40 to +85				3	10	
			T_A = 25 C					10	
C_f	Feed-through capacitance	A to B	V_I = 0				0.5		pF
C_o	Output capacitance	A or B			5 V		9		pF

6.6 Switching Characteristics

T_A = –40 to +85 °C unless otherwise specified.

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	A or B	B or A	C_L = 50 pF (see Figure 5)	T_A = 25°C	2 V		10	60	ns
					T_A = –40 to +85				75	
					T_A = 25°C	4.5 V		4	12	
					T_A = –40 to +85				15	
					T_A = 25°C	6 V		3	10	
					T_A = –40 to +85				13	
t_{PZH}, t_{PZL}	Switch turn-on time	C	A or B	R_L = 1 kΩ, C_L = 50 pF (see Figure 6)	T_A = 25°C	2 V		70	180	ns
					T_A = –40 to +85				225	
					T_A = 25°C	4.5 V		21	36	
					T_A = –40 to +85				45	
					T_A = 25°C	6 V		18	31	
					T_A = –40 to +85				38	
t_{PLZ}, t_{PHZ}	Switch turn-off time	C	A or B	R_L = 1 kΩ, C_L = 50 pF (see Figure 6)	T_A = 25°C	2 V		50	200	ns
					T_A = –40 to +85				250	
					T_A = 25°C	4.5 V		25	40	
					T_A = –40 to +85				50	
					T_A = 25°C	6 V		22	34	
					T_A = –40 to +85				43	

Switching Characteristics (continued)

T_A = –40 to +85 °C unless otherwise specified.

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
f_I	Control input frequency	C	A or B	C_L = 15 pF, R_L = 1 kΩ, V_C = V_{CC} or GND, V_O = V_{CC} / 2 (see Figure 7)	T_A = 25°C	2 V		15		MHz
					T_A = 25°C	4.5 V		30		
					T_A = 25°C	6 V		30		
	Control feed-through noise	C	A or B	C_L = 50 pF, R_{in} = R_L = 600 Ω, V_C = V_{CC} or GND, f_{in} = 1 MHz (see Figure 8)	T_A = 25°C	4.5 V		15		mV (rms)
					T_A = 25°C	6 V		20		

6.7 Operating Characteristics

V_{CC} = 4.5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	C_L = 50 pF,	f = 1 MHz	45	pF
	Minimum through bandwidth, A to B or B to A(1) [20 log (V_O / V_I)] = –3 dB	C_L = 50 pF, V_C = V_{CC}	R_L = 600 Ω, (see Figure 9)	30	MHz
	Crosstalk between any switches(2)	C_L = 10 pF, f_{in} = 1 MHz	R_L = 50 Ω, (see Figure 10)	45	dB
	Feed through, switch off, A to B or B to A(2)	C_L = 50 pF, f_{in} = 1 MHz	R_L = 600 Ω, (see Figure 11)	42	dB
	Amplitude distortion rate, A to B or B to A	C_L = 50 pF, f_{in} = 1 kHz	R_L = 10 kΩ, (see Figure 12)	0.05%	

(1) Adjust the input amplitude for output = 0 dBm at f = 1 MHz. Input signal must be a sine wave.
(2) Adjust the input amplitude for input = 0 dBm at f = 1 MHz. Input signal must be a sine wave.

6.8 Typical Characteristics

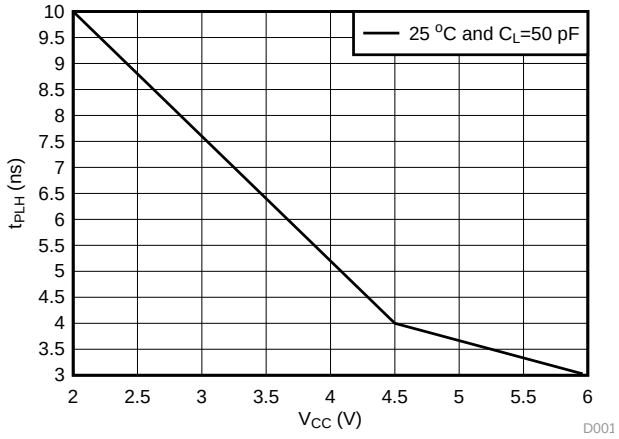


Figure 1. t_{PLH} vs V_{CC}

7 Parameter Measurement Information

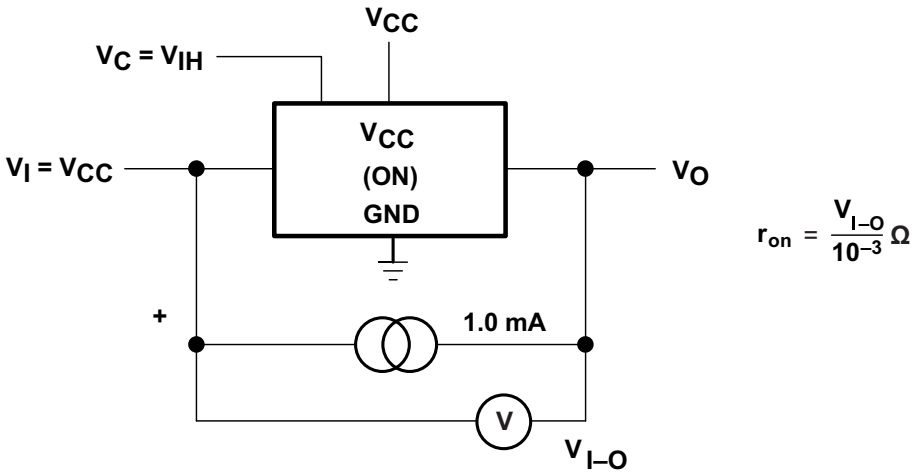
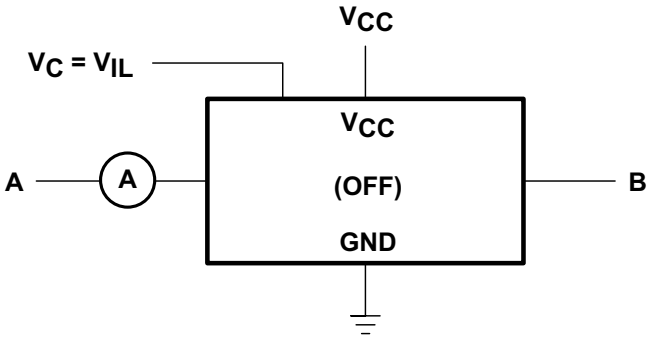
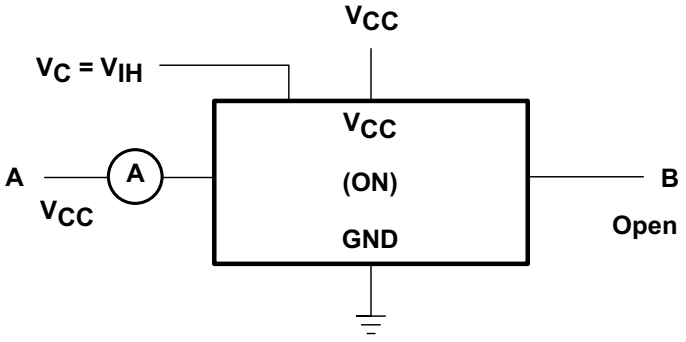


Figure 2. ON-State Resistance Test Circuit



$V_S = V_A - V_B$
CONDITION 1: $V_A = 0$, $V_B = V_{CC}$
CONDITION 2: $V_A = V_{CC}$, $V_B = 0$

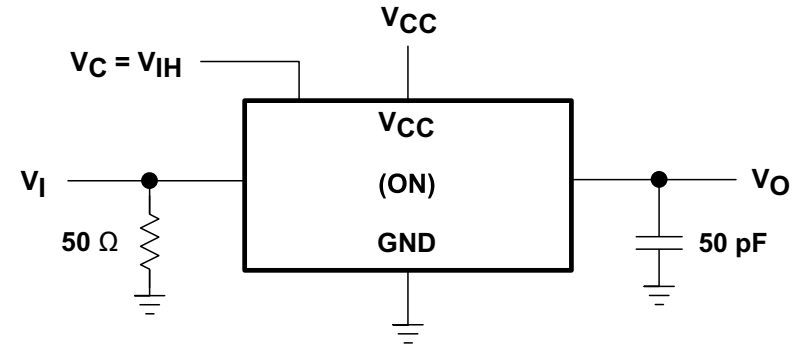
Figure 3. OFF-State Switch Leakage-Current Test Circuit



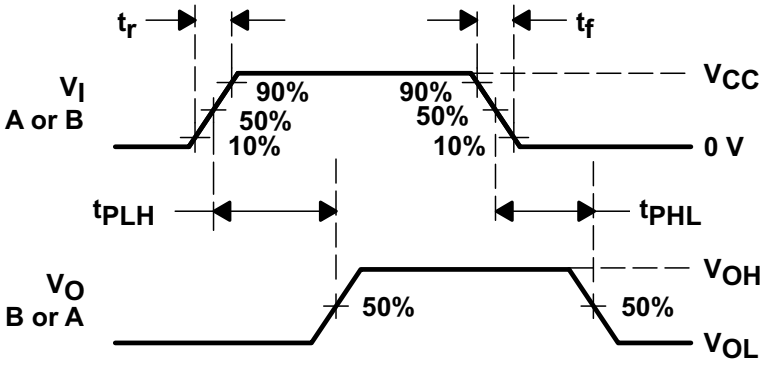
$V_A = V_{CC}$ TO GND

Figure 4. ON-State Leakage-Current Test Circuit

Parameter Measurement Information (continued)



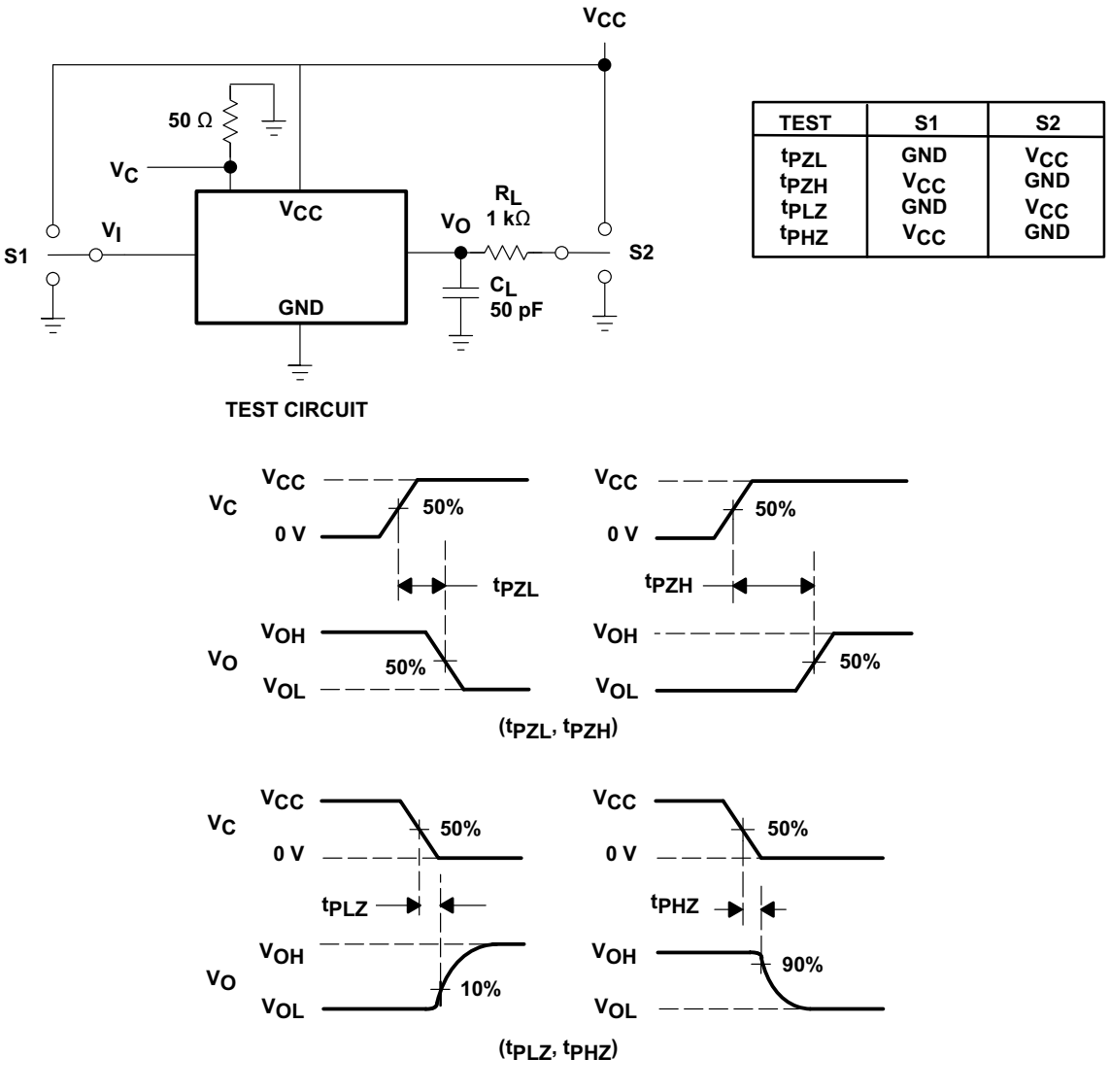
TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 5. Propagation Delay Time, Signal Input to Signal Output

Parameter Measurement Information (continued)



TEST	S1	S2
t_{PZL}	GND	V_{CC}
t_{PZH}	V_{CC}	GND
t_{PLZ}	GND	V_{CC}
t_{PHZ}	V_{CC}	GND

Figure 6. Switching Time (t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}), Control to Signal Output

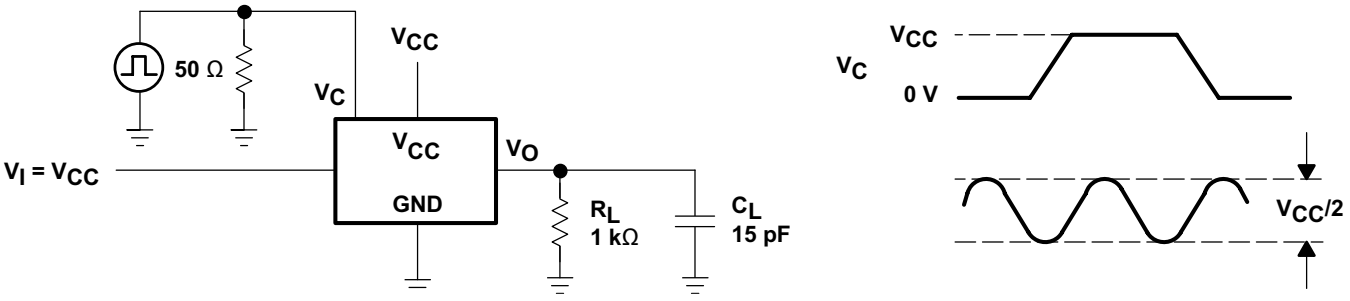


Figure 7. Control-Input Frequency

Parameter Measurement Information (continued)

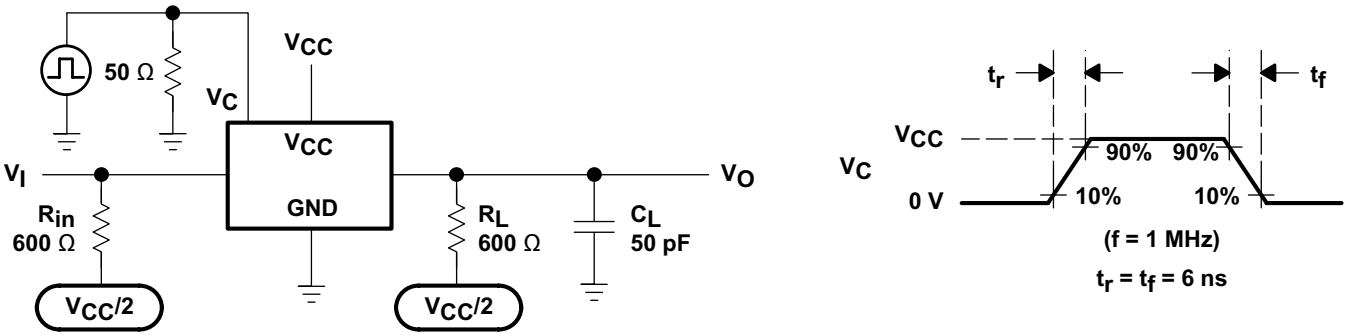


Figure 8. Control Feed-Through Noise

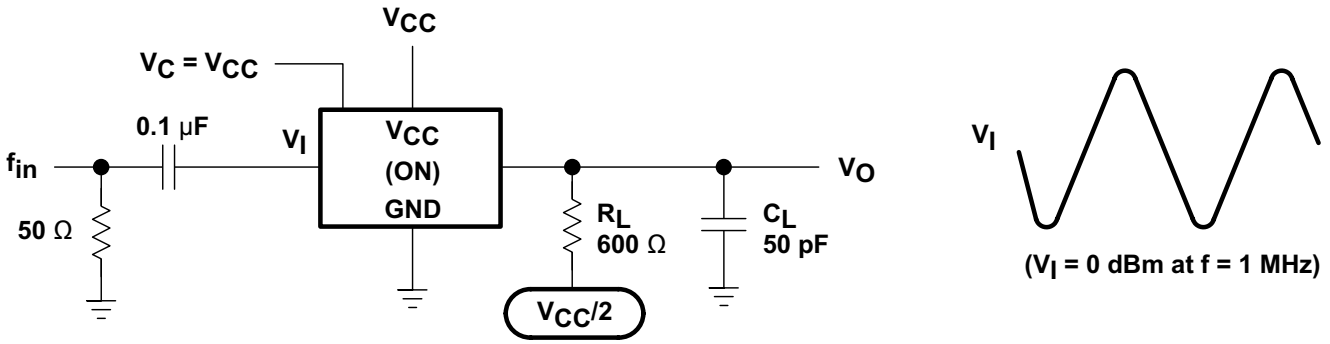


Figure 9. Minimum Through Bandwidth

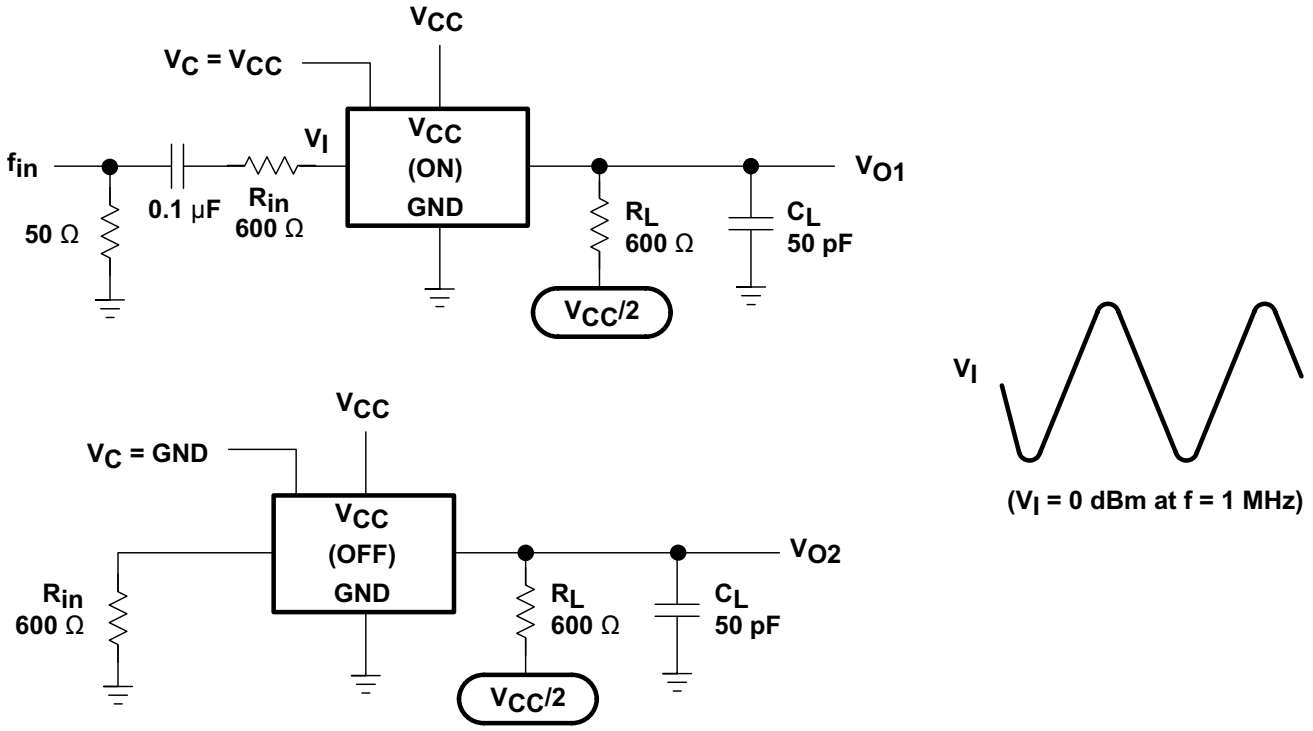


Figure 10. Crosstalk Between Any Two Switches

Parameter Measurement Information (continued)

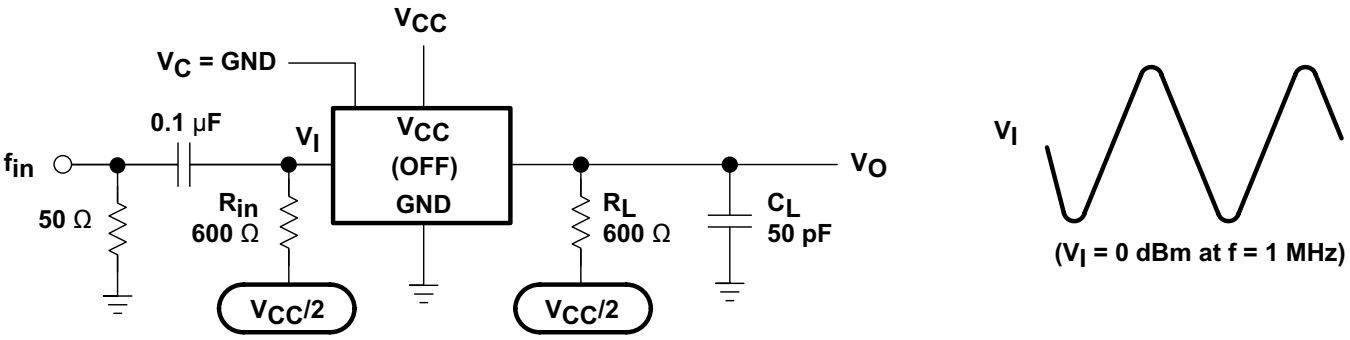


Figure 11. Feed Through, Switch OFF

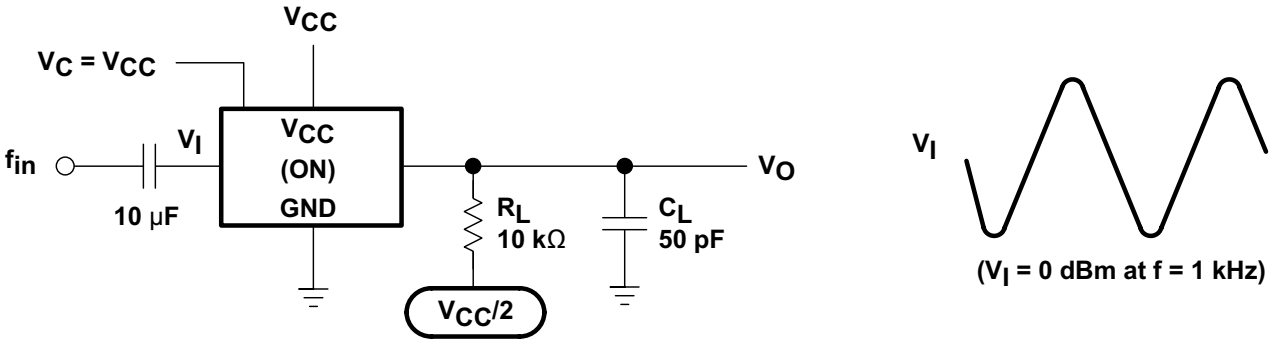


Figure 12. Amplitude-Distortion Rate

8 Detailed Description

8.1 Overview

The SN74HC4066 device is a silicon-gate CMOS quadruple analog switch designed for 2-V to 6-V VCC operation. It is designed to handle both analog and digital signals. Each switch permits signals with amplitudes of up to 6 V (peak) to be transmitted in either direction. A high-level voltage applied to the control pin C enables the respective switch to begin propagating signals across the device.

8.2 Functional Block Diagram

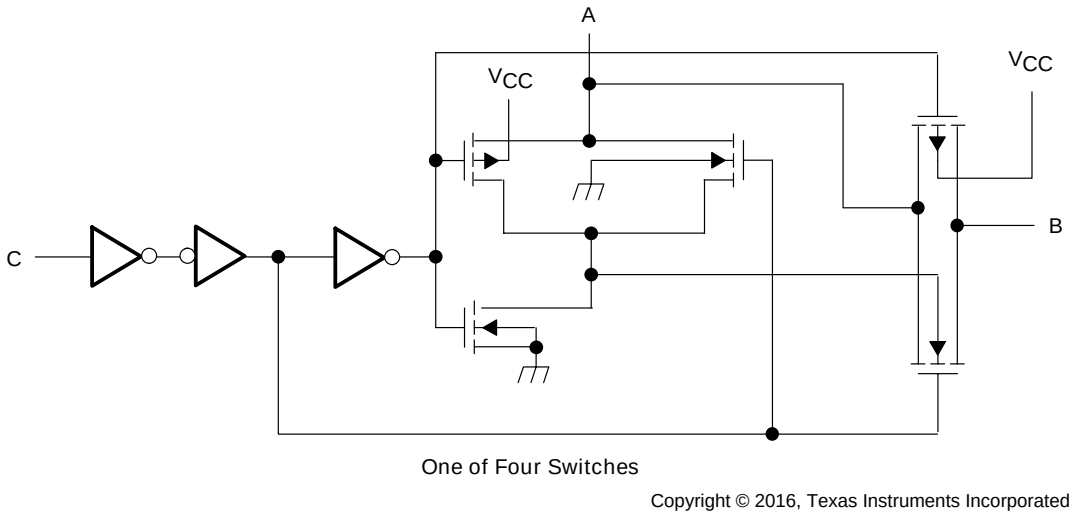


Figure 13. Logic Diagram, Each Switch (Positive Logic)

8.3 Feature Description

Each switch section has its own enable-input control (C). A high-level voltage applied to C turns on the associated switch section, with typically 18 ns of switch enable time. The SN74HC4066 has a wide operating voltage range of 2 V to 6 V. It has low power consumption, with 20-µA maximum I_{CC} and a low on-state impedance of 50 Ω. It also has low crosstalk between switches to minimize noise.

8.4 Device Functional Modes

Table 1 lists the functions for the SN74HC4066 device.

Table 1. Function Table (Each Switch)

INPUT CONTROL (C)	SWITCH
L	OFF
H	ON

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74HC4066 can be used in any situation where an dual SPST switch would be used and a solid-state, voltage controlled version is preferred.

9.2 Typical Application

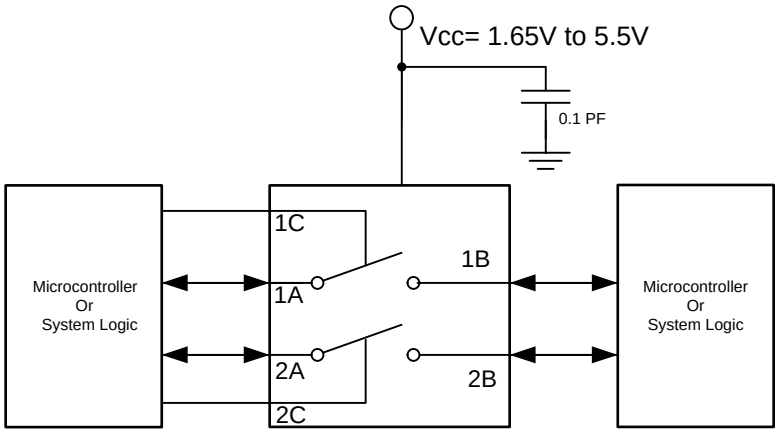


Figure 14. t_{PZH} vs V_{CC}

9.2.1 Design Requirements

The SN74HC4066 allows ON/OFF control of analog and digital signals with a digital control signal. All input signals should remain between 0 V and V_{CC} for optimal operation.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - For rise time and fall time specifications, see $\Delta t/\Delta v$ in *Recommended Operating Conditions*.
   - For specified high and low levels, see V_{IH} and V_{IL} in *Recommended Operating Conditions*.
2. Recommended Output Conditions:
   - On-state switch current should not exceed ±25 mA.

Typical Application (continued)

9.2.3 Application Curve

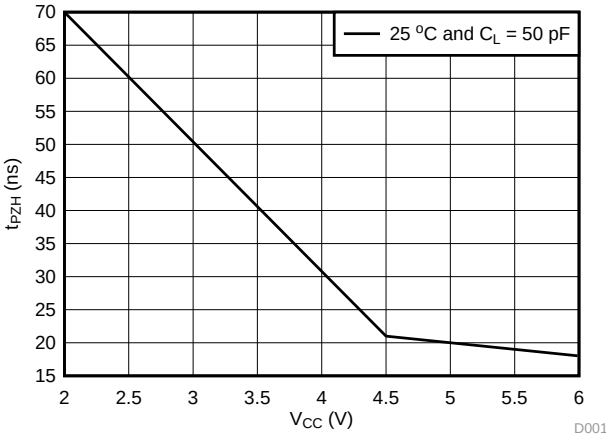


Figure 15. t_{PZH} vs V_{CC}

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-µF bypass capacitor. If there are multiple pins labeled V_{CC}, then a 0.01-µF or 0.022-µF capacitor is recommended for each V_{CC} because the VCC pins will be tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD}, TI recommends a 0.1-µF bypass capacitor for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace — resulting in the reflection.

NOTE

Not all PCB traces can be straight, and so they will have to turn corners. Figure 16 shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

11.2 Layout Example

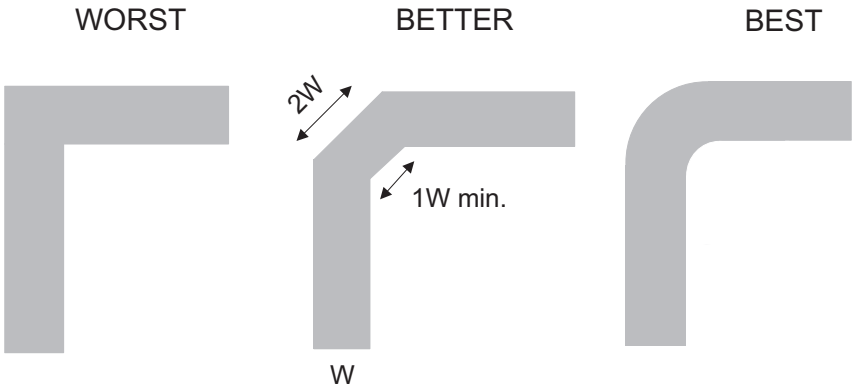


Figure 16. Trace Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs (SCBA004)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HC4066D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4066	Samples
SN74HC4066DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4066	Samples
SN74HC4066DBRE4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4066	Samples
SN74HC4066DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4066	Samples
SN74HC4066DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4066	Samples
SN74HC4066DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4066	Samples
SN74HC4066DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4066	Samples
SN74HC4066DT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4066	Samples
SN74HC4066N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC4066N	Samples
SN74HC4066NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC4066N	Samples
SN74HC4066NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4066	Samples
SN74HC4066PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4066	Samples
SN74HC4066PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4066	Samples
SN74HC4066PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4066	Samples
SN74HC4066PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4066	Samples
SN74HC4066PWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC4066	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

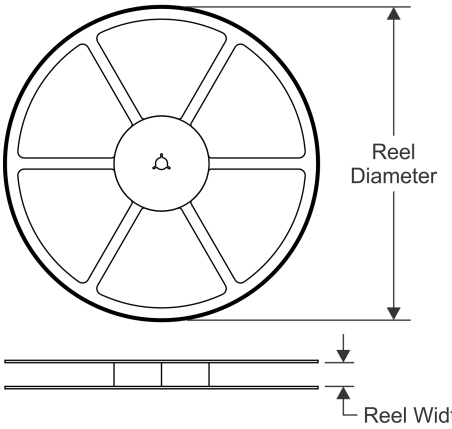
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

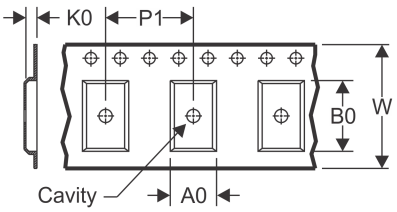
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

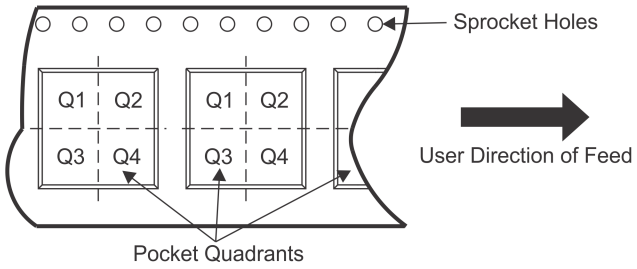


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

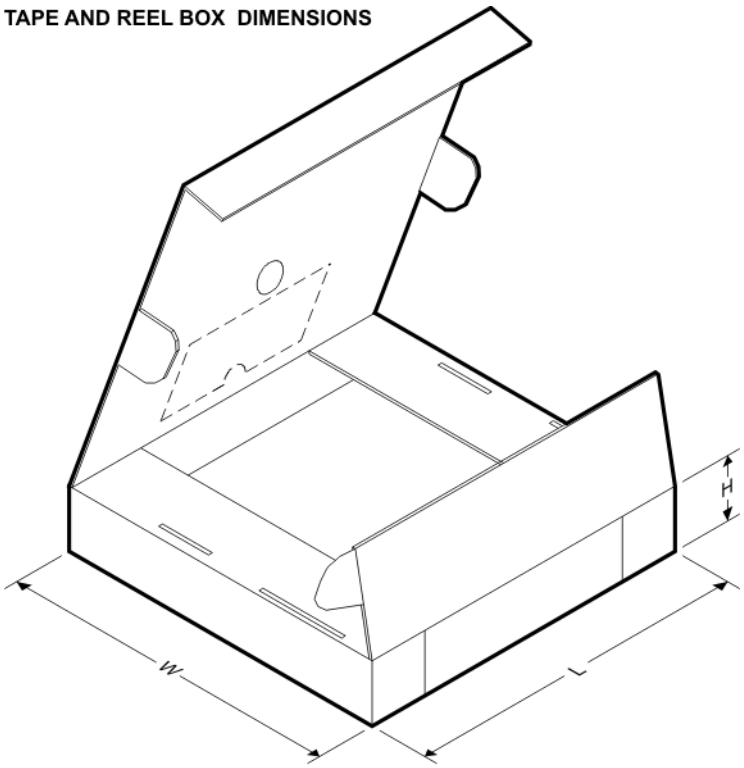
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC4066DBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74HC4066DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC4066DT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC4066NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74HC4066PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC4066PWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



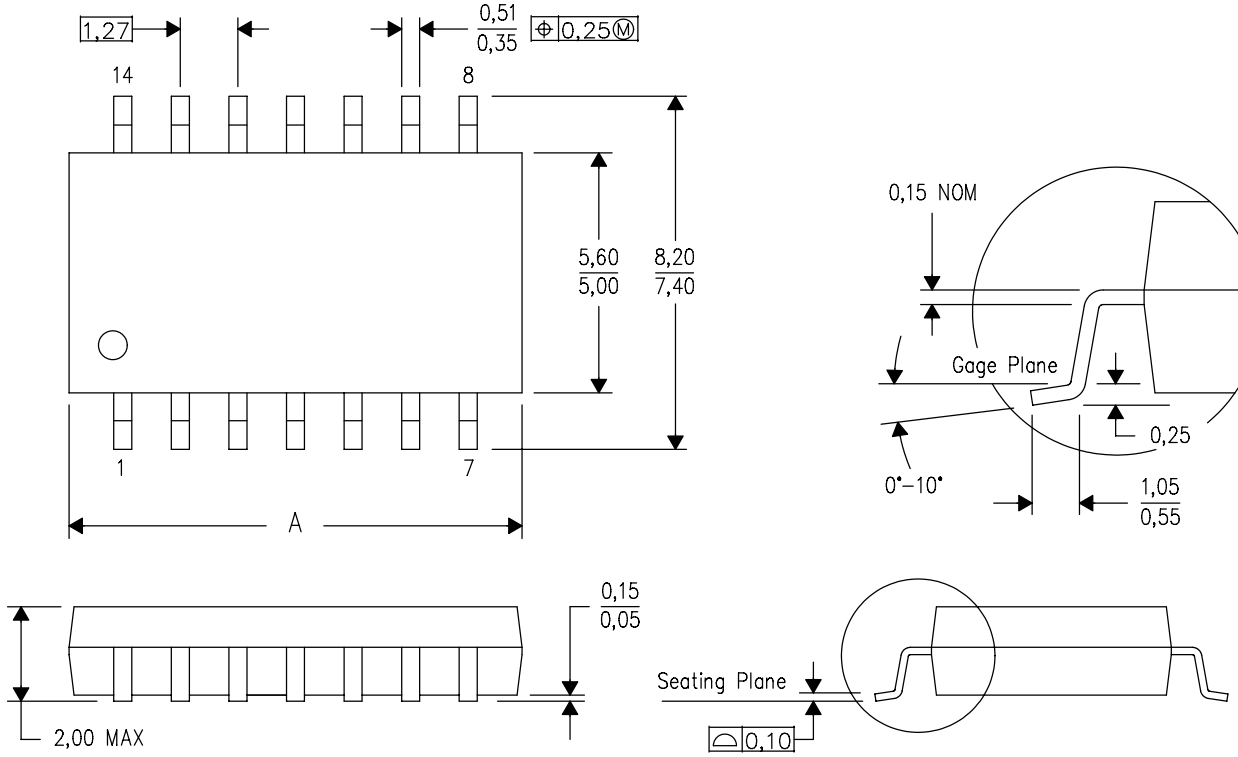
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC4066DBR	SSOP	DB	14	2000	367.0	367.0	38.0
SN74HC4066DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74HC4066DT	SOIC	D	14	250	367.0	367.0	38.0
SN74HC4066NSR	SO	NS	14	2000	367.0	367.0	38.0
SN74HC4066PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74HC4066PWT	TSSOP	PW	14	250	367.0	367.0	35.0

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

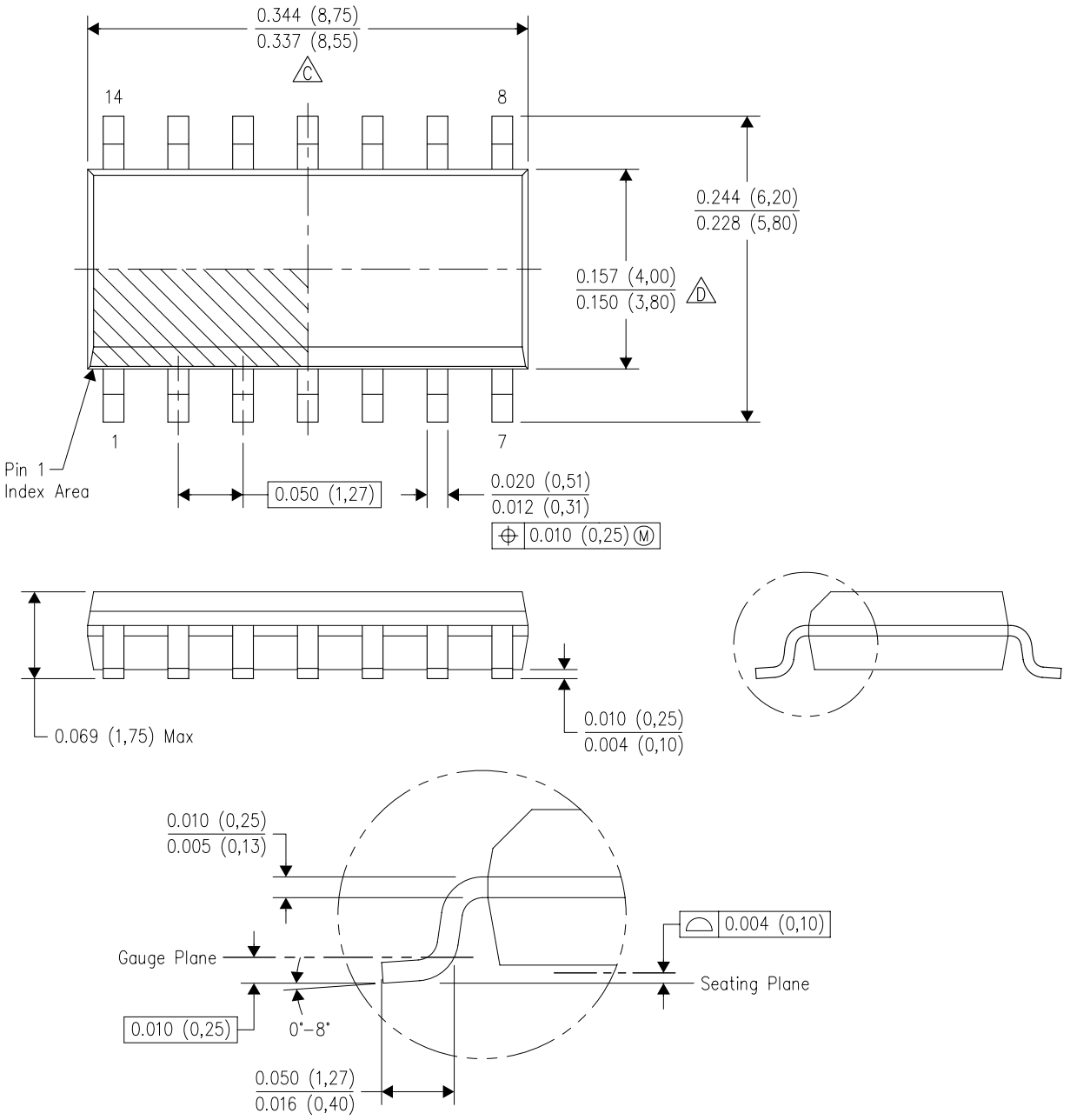


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

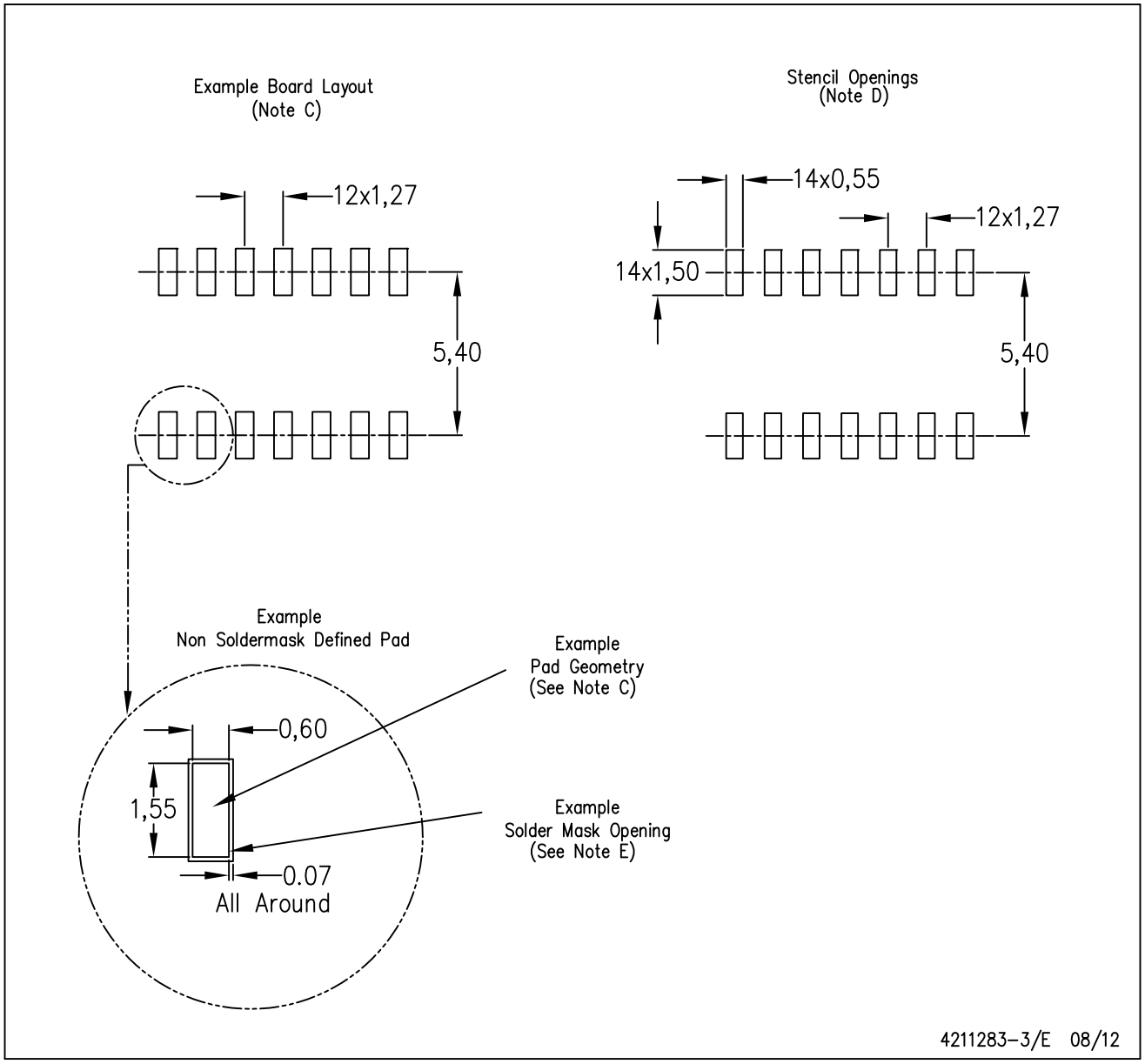
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

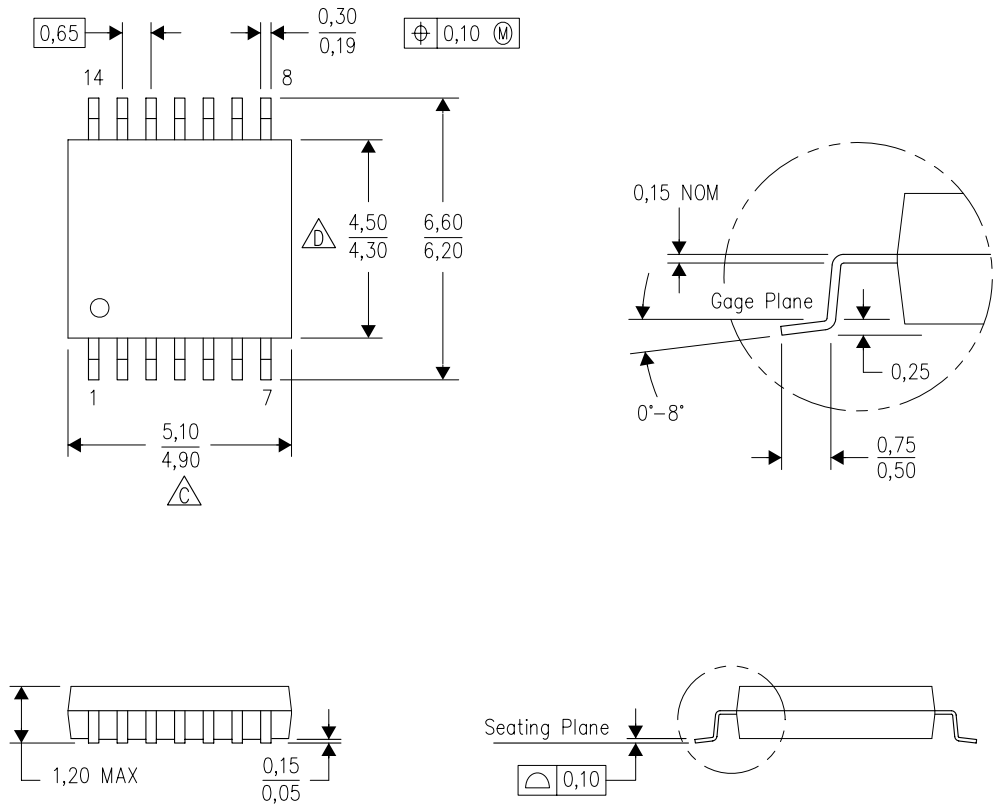
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

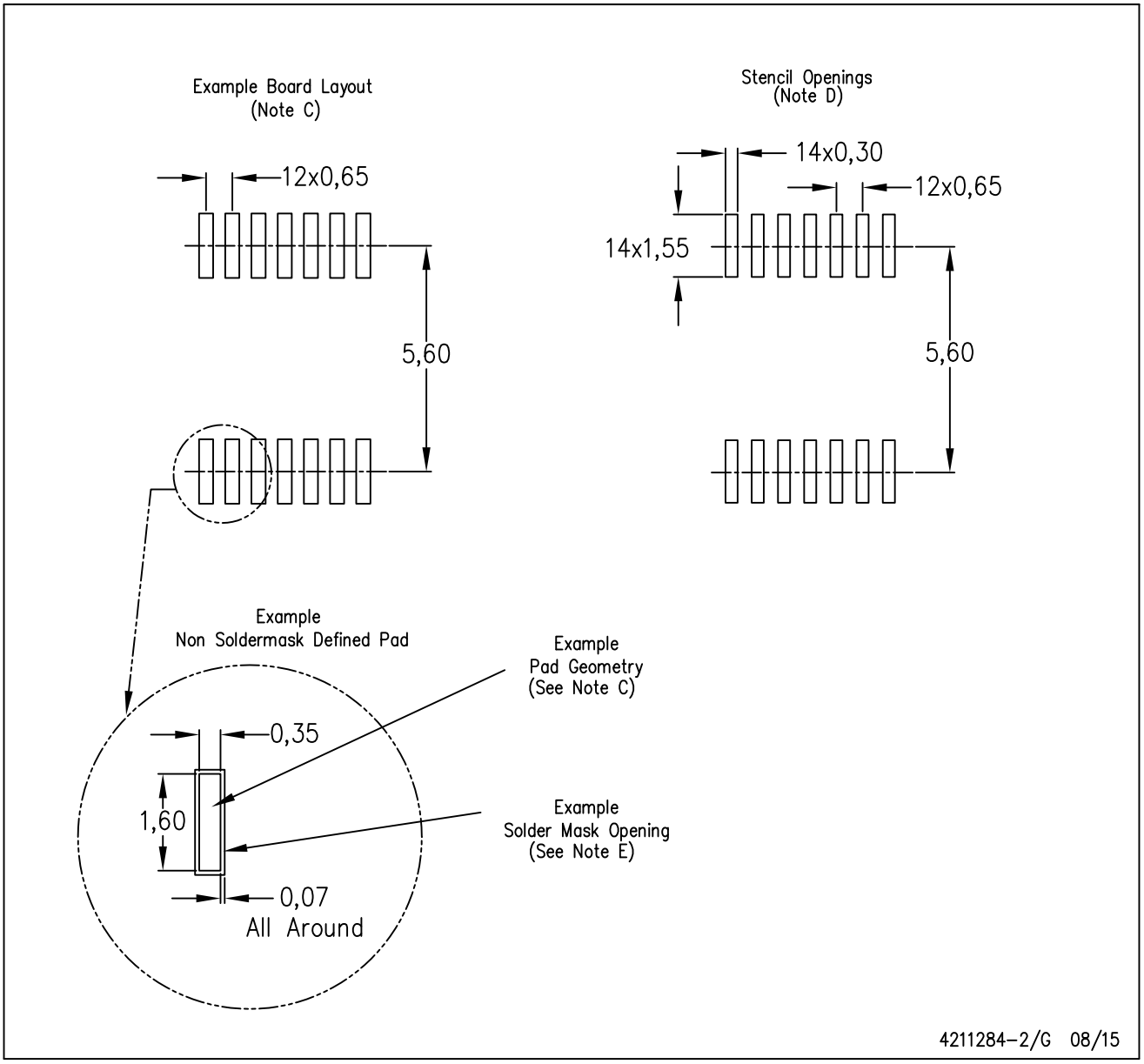
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

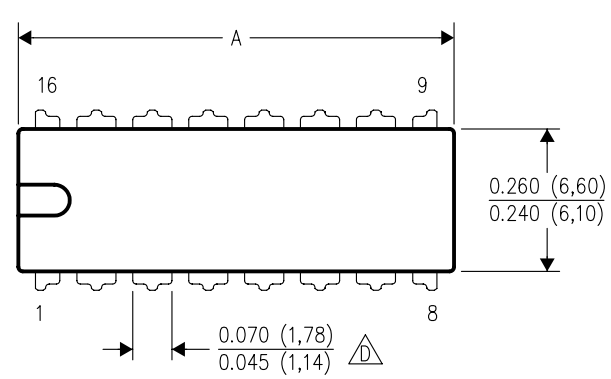


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

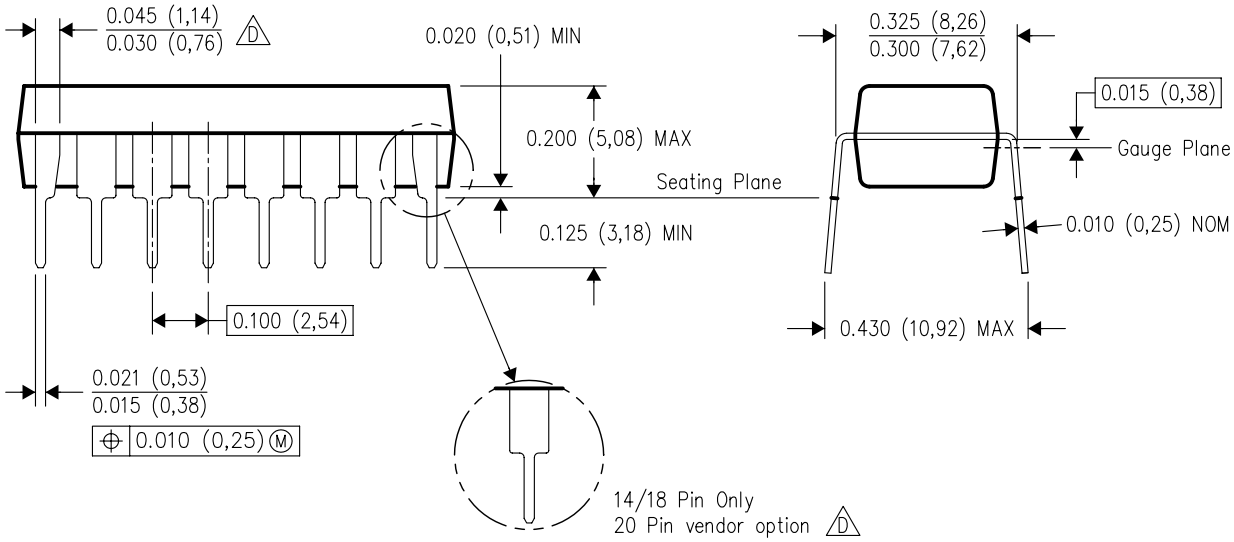
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



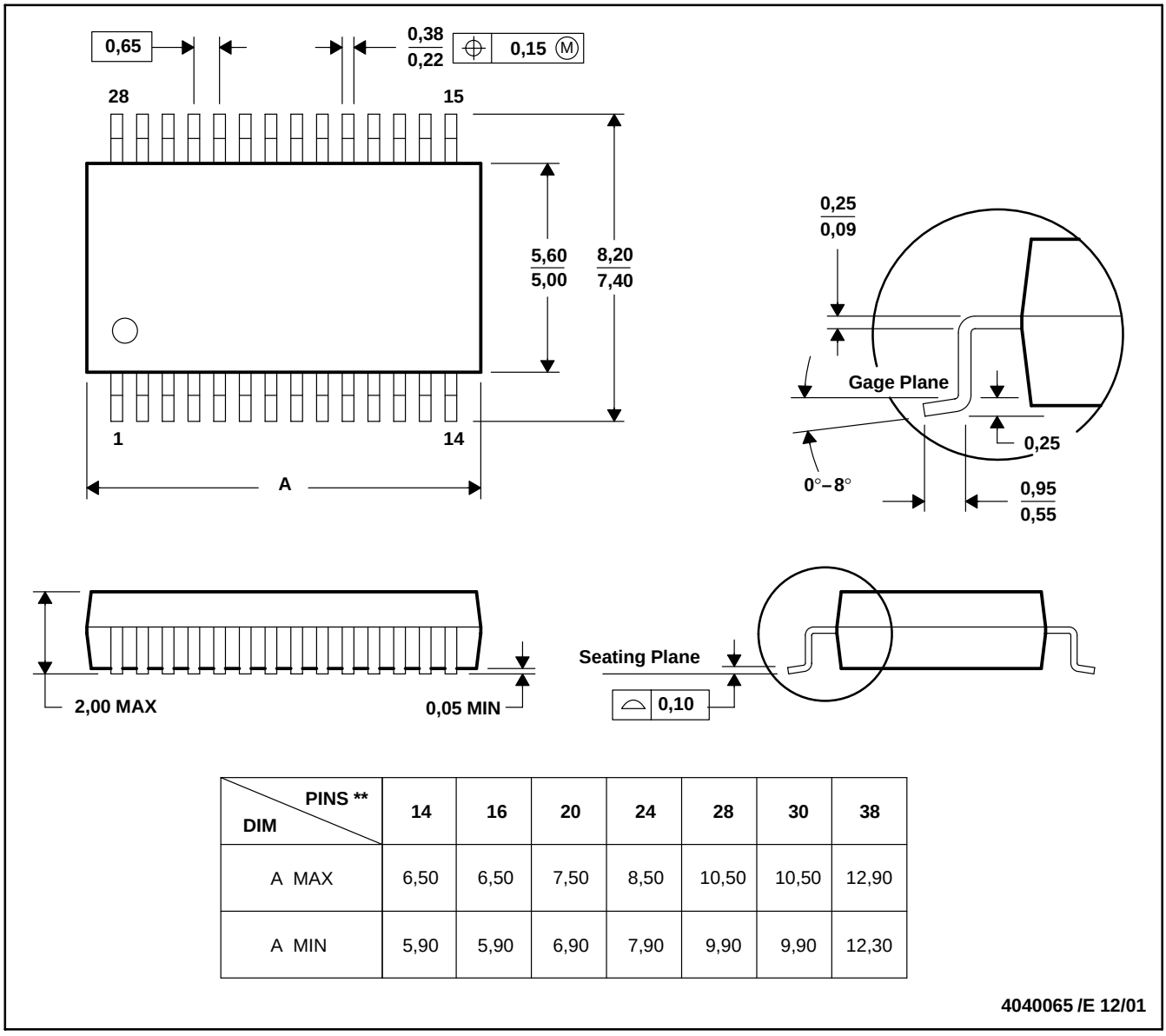
4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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