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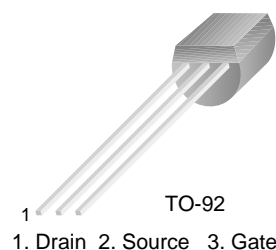
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PF5102

N-Channel Switch

Features

- This device is designed for low level analog switching, sample and hold circuits and chopper stabilized amplifiers.
- Sourced from process 51.
- See J111 for characteristics.



Absolute Maximum Ratings* $T_a = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Value	Units
V_{DG}	Drain-Gate Voltage	40	V
V_{GS}	Gate-Source Voltage	-40	V
I_{GF}	Forward Gate Current	50	mA
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

* These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES:

1. These ratings are based on a maximum junction temperature of 150 degrees C.
2. These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.

Thermal Characteristics $T_a = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Max.	Units
P_D	Total Device Dissipation Derate above 25°C	625 5.0	mW mW/ $^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	125	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	357	$^\circ\text{C}/\text{W}$

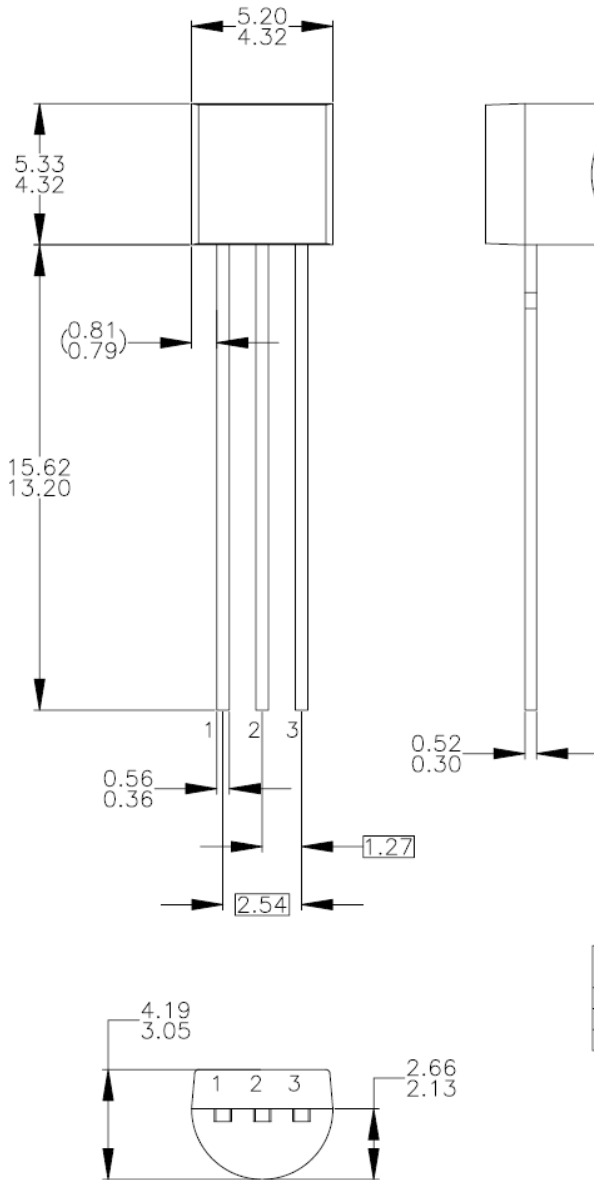
Electrical Characteristics $T_a = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Max.	Units
Off Characteristics					
$V_{(BR)GSS}$	Gate-Source Breakdown Voltage	$I_G = -1.0\mu\text{A}, V_{DS} = 0$	-40		V
I_{GSS}	Gate Reverse Current	$V_{GS} = -15\text{V}, V_{DS} = 0$ $V_{GS} = -15\text{V}, V_{DS} = 0, T_A = 125^\circ\text{C}$		-1.0 -0.2	nA μA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 15\text{V}, I_D = 1.0\text{nA}$	-0.7	-1.6	V
$V_{GS(f)}$	Gate-Source Forward Voltage	$I_G = 1.0\text{mA}, V_{DS} = 0$		1.0	V
On Characteristics					
I_{DSS}	Zero-Gate Voltage Drain Current *	$V_{DS} = 15\text{V}, V_{GS} = 0$	4.0	20	mA
Small Signal Characteristics					
g_{fs}	Forward Transfer Conductance	$V_{DS} = 15\text{V}, V_{GS} = 0, f = 1.0\text{KHz}$	11,000		μmhos
g_{oss}	Output Conductance	$V_{DS} = 15\text{V}, I_D = 500\mu\text{A}, f = 1.0\text{KHz}$		25	μmhos
C_{iss}	Input Capacitance	$V_{DG} = 15\text{V}, V_{GS} = 0, f = 1.0\text{MHz}$		16	pF
C_{rss}	Reverse Transfer Capacitance	$V_{DG} = 15\text{V}, V_{GS} = 0, f = 1.0\text{MHz}$		6	pF

* Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 1.0\%$

Physical Dimension

TO-92



NOTES: UNLESS OTHERWISE SPECIFIED

- A) DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DRAWING CONFORMS TO ASME Y14.5M-1994.
- D) TO-92 (92,94,96,97,98) PIN CONFIGURATION:

PIN	92			94			96			97			98		
	P	F	M	P	F	M	P	F	M	P	F	M	P	F	M
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G

LEGEND:

P - BIPOLAR E - EMITTER D - DRAIN
 F - JFET B - BASE S - SOURCE
 M - DMOS C - COLLECTOR G - GATE






- E) FOR PACKAGE 92, 94, 96, 97 AND 98:
PIN CONFIGURATION DRAIN "D" AND SOURCE "S"
ARE INTERCHANGEABLE AT JFET "F" OPTION.
- F) DRAWING FILENAME: MKT-ZA03DREV3.

Dimensions in Millimeters



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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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