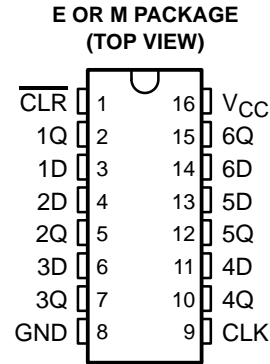


- AC Types Feature 1.5-V to 5.5-V Operation and Balanced Noise Immunity at 30% of the Supply Voltage
- Contains Six Flip-Flops With Single-Rail Outputs
- Buffered Inputs
- Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption
- Balanced Propagation Delays
- ±24-mA Output Drive Current
 - Fanout to 15 F Devices
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015
- Applications Include:
 - Buffer/Storage Registers
 - Shift Registers



description/ordering information

The CD74AC174 is a positive-edge-triggered D-type flip-flop with a direct clear ($\overline{\text{CLR}}$) input and is designed for 1.5-V to 5.5-V V_{CC} operation.

Information at the data (D) inputs that meets the setup time requirements is transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge of CLK. When CLK is at either the high or low level, the D input has no effect at the output.

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	PDIP – E	Tube	CD74AC174E	CD74AC174E
	SOIC – M	Tube	CD74AC174M	AC174M
		Tape and reel	CD74AC174M96	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{\text{CLR}}$	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q ₀



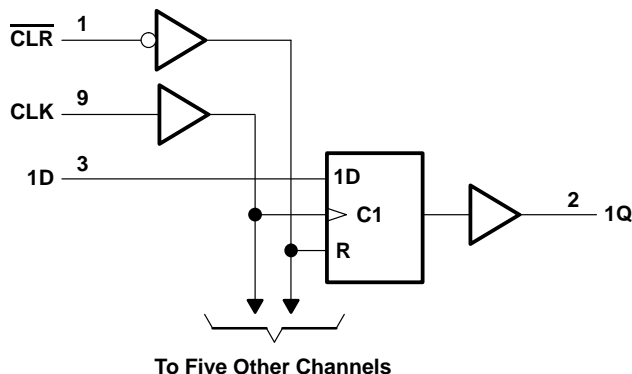
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

CD74AC174 HEX D-TYPE FLIP-FLOP WITH CLEAR

SCHS346 – APRIL 2003

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 6 V
Input clamp current, I_{IK} ($V_I < 0$ V or $V_I > V_{CC}$) (see Note 1)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ V or $V_O > V_{CC}$) (see Note 1)	± 50 mA
Continuous output current, I_O ($V_O > 0$ V or $V_O < V_{CC}$)	± 50 mA
Continuous current through V_{CC} or GND	± 150 mA
Package thermal impedance, θ_{JA} (see Note 2): E package	67°C/W
M package	73°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		$T_A = 25^\circ\text{C}$		$-55^\circ\text{C to } 125^\circ\text{C}$		$-40^\circ\text{C to } 85^\circ\text{C}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	1.5	5.5	1.5	5.5	1.5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 1.5$ V		1.2	1.2	1.2	1.2	V
		$V_{CC} = 3$ V		2.1	2.1	2.1	2.1	
		$V_{CC} = 5.5$ V		3.85	3.85	3.85	3.85	
V_{IL}	Low-level input voltage	$V_{CC} = 1.5$ V		0.3	0.3	0.3	0.3	V
		$V_{CC} = 3$ V		0.9	0.9	0.9	0.9	
		$V_{CC} = 5.5$ V		1.65	1.65	1.65	1.65	
V_I	Input voltage	0	V_{CC}	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 4.5$ V to 5.5 V		-24	-24	-24	-24	mA
I_{OL}	Low-level output current	$V_{CC} = 4.5$ V to 5.5 V		24	24	24	24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 1.5$ V to 3 V		50	50	50	50	ns/V
		$V_{CC} = 3.6$ V to 5.5 V		20	20	20	20	

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C		–55°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = –50 μA	1.5 V	1.4	1.4	1.4			V
			3 V	2.9	2.9	2.9			
			4.5 V	4.4	4.4	4.4			
		I _{OH} = –4 mA	3 V	2.58	2.4	2.48			
		I _{OH} = –24 mA	4.5 V	3.94	3.7	3.8			
		I _{OH} = –50 mA†	5.5 V		3.85				
		I _{OH} = –75 mA†	5.5 V			3.85			
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 50 μA	1.5 V		0.1		0.1		V
			3 V		0.1		0.1		
			4.5 V		0.1		0.1		
		I _{OL} = 12 mA	3 V		0.36		0.5	0.44	
		I _{OL} = 24 mA	4.5 V		0.36		0.5	0.44	
		I _{OL} = 50 mA†	5.5 V				1.65		
		I _{OL} = 75 mA†	5.5 V				1.65		
I _I	V _I = V _{CC} or GND	5.5 V		±0.1		±1		±1	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V		8		160		80	μA
C _i				10		10		10	pF

† Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

timing requirements over recommended operating free-air temperature range, V_{CC} = 1.5 V (unless otherwise noted)

		–55°C to 125°C		–40°C to 85°C		UNIT
		MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		8		9	MHz
t _w	Pulse duration	CLR low		50	44	ns
		CLK high or low		65	57	
t _{su}	Setup time before CLK↑	Data		2	2	ns
t _h	Hold time, data after CLK↑			38	33	ns
t _{rec}	Recovery time, before CLK↑	CLR↑		1.5	1.5	ns

CD74AC174
HEX D-TYPE FLIP-FLOP
WITH CLEAR

SCHS346 – APRIL 2003

timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3 V \pm 0.3 V$ (unless otherwise noted)

		-55°C to 125°C		-40°C to 85°C		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	68		77		MHz
t_w	Pulse duration	CLR low		4.9		ns
		CLK high or low		6.4		
t_{su}	Setup time before CLK↑	Data		2		ns
t_h	Hold time, data after CLK↑			3.7		ns
t_{rec}	Recovery time, before CLK↑	CLR↑		1.5		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5 V \pm 0.5 V$ (unless otherwise noted)

		-55°C to 125°C		-40°C to 85°C		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	95		108		MHz
t_w	Pulse duration	CLR low		3.5		ns
		CLK high or low		4.6		
t_{su}	Setup time before CLK↑	Data		2		ns
t_h	Hold time, data after CLK↑			2.6		ns
t_{rec}	Recovery time, before CLK↑	CLR↑		1.5		ns

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 1.5 V$, $C_L = 50 pF$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			8		9		MHz
t_{PLH}	CLK	Any Q	169		154		ns
t_{PHL}			169		154		
t_{PLH}	CLR	Any Q	181		165		ns
t_{PHL}			181		165		

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3 V \pm 0.3 V$, $C_L = 50 pF$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			68		77		MHz
t_{PLH}	CLK	Any Q	4.7 18.9		4.9 17.2		ns
t_{PHL}			4.7 18.9		4.9 17.2		
t_{PLH}	CLR	Any Q	5.1 20.3		5.2 18.5		ns
t_{PHL}			5.1 20.3		5.2 18.5		



switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			95		108		MHz
t_{PLH}	CLK	Any Q	3.4	13.5	3.5	12.3	ns
t_{PHL}			3.4	13.5	3.5	12.3	
t_{PLH}	$\overline{\text{CLR}}$	Any Q	3.6	14.5	3.7	13.2	ns
t_{PHL}			3.6	14.5	3.7	13.2	

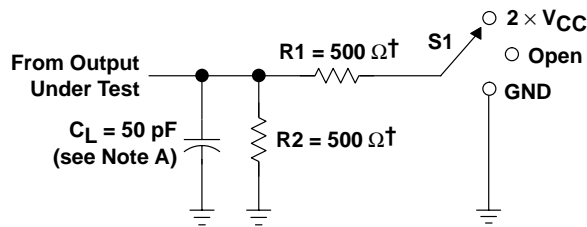
operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TYP	UNIT
C_{pd}	Power dissipation capacitance	37	pF

CD74AC174 HEX D-TYPE FLIP-FLOP WITH CLEAR

SCHS346 – APRIL 2003

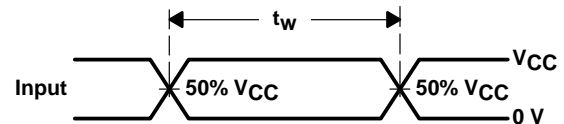
PARAMETER MEASUREMENT INFORMATION



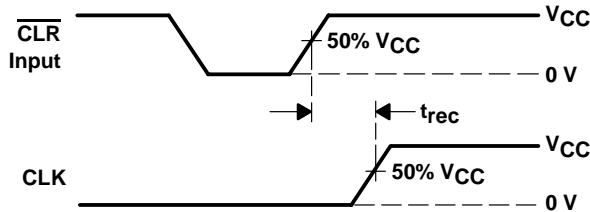
† When $V_{CC} = 1.5 \text{ V}$, $R_1 = R_2 = 1 \text{ k}\Omega$

LOAD CIRCUIT

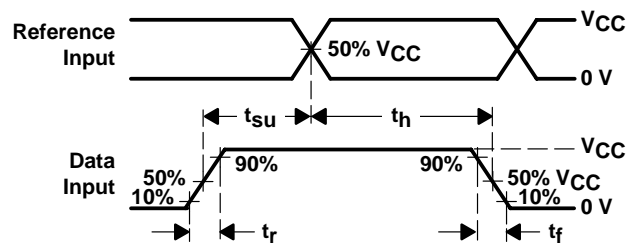
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



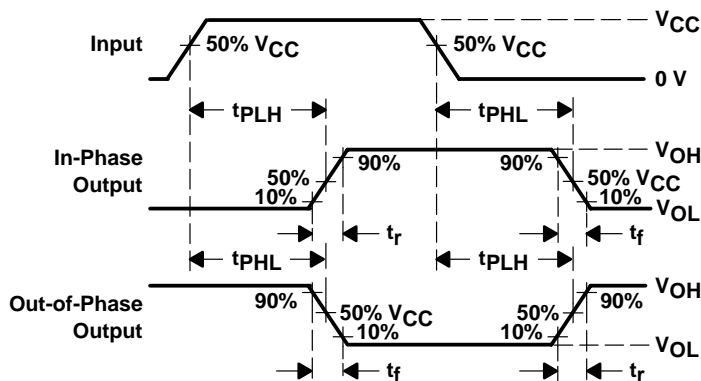
VOLTAGE WAVEFORMS
PULSE DURATION



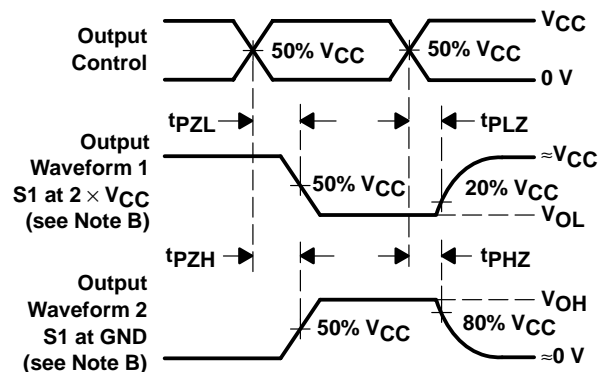
VOLTAGE WAVEFORMS
RECOVERY TIME



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and test-fixture capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$. Phase relationships between waveforms are arbitrary.
 - For clock inputs, f_{max} is measured with the input duty cycle at 50%.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74AC174E	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74AC174E	Samples
CD74AC174M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC174M	Samples
CD74AC174M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC174M	Samples
CD74AC174M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC174M	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC174M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC174M96	SOIC	D	16	2500	333.2	345.9	28.6

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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