10MHz to 80MHz, 10:1 LVDS Parallel-to-Serial Converter(Serializer)/ Serial-to-Parallel Converter(Deserializer)

PRODUCT DESCRIPTION

The MS1023 serializer and the MS1224 deserializer are a pair of 10-bit serial-to-parallel/parallel-to-serial converters, which are used to transmit and receive serial data at parallel word rates from 10MHz to 80MHz over LVDS differential backplanes. After loading the start/stop bits, it converts to a payload-encoded output with serial data rates between 120Mbps and 960Mbps.

When powering up, this pair of chips can be initialized by synchronization mode with internally generated SYNC sample signal or the deserializer is synchronized with random data. By using the synchronization mode, the deserializer can establish lock within specified and shorter time parameters.

When there are no data transfer requirements, the device can be set to enter the power-down mode. In addition, a mode is available to set the output pins in high-impedance state to avoid PLL loss of lock.

The operating temperature of the MS1023 and the MS1224 are from -40°C to 85°C.

SSOP28

FEATURES

- 100Mbps to 800Mbps Serial LVDS Data Payload Bandwidth at 10MHz to 80MHz System Clock
- Chip Power Dissipation < 550mW (Typ) at 80MHz Input
- Synchronization Mode for Locking Clock Quickly
- Lock Indicator
- No External Components Required for PLL
- SSOP28 Package
- Programmable Edge Trigger on Clock
- Flow-through Pinout for Easy PCB Layout

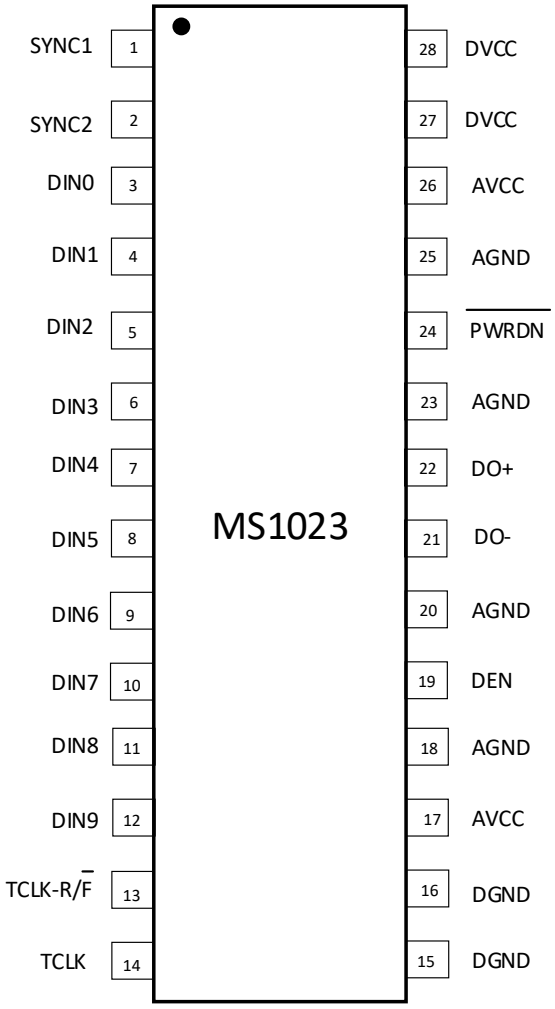
APPLICATIONS

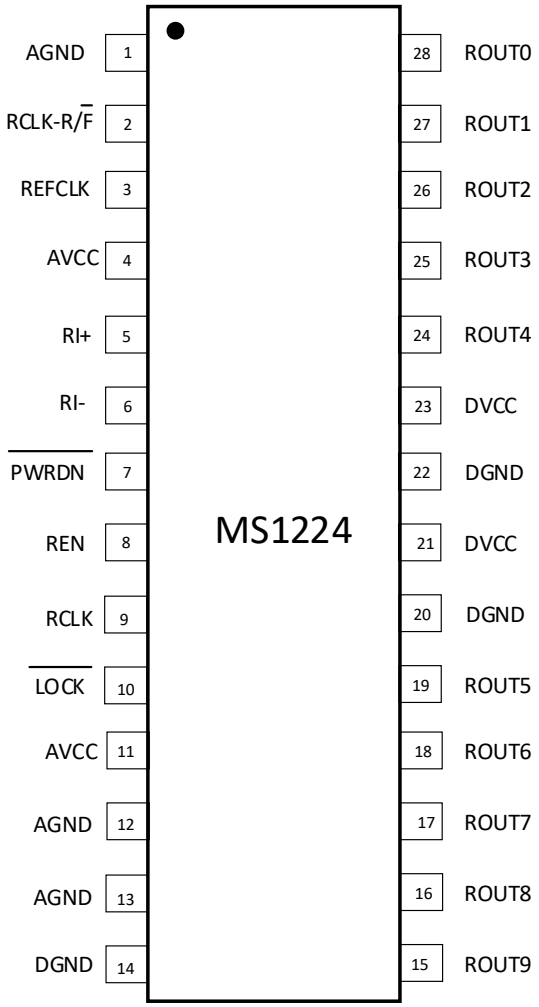
- Wireless Base Station
- Backplanes Interconnection
- Digital Subscriber Line Access Multiplexer

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS1023	SSOP28	MS1023
MS1224	SSOP28	MS1224

PIN CONFIGURATION



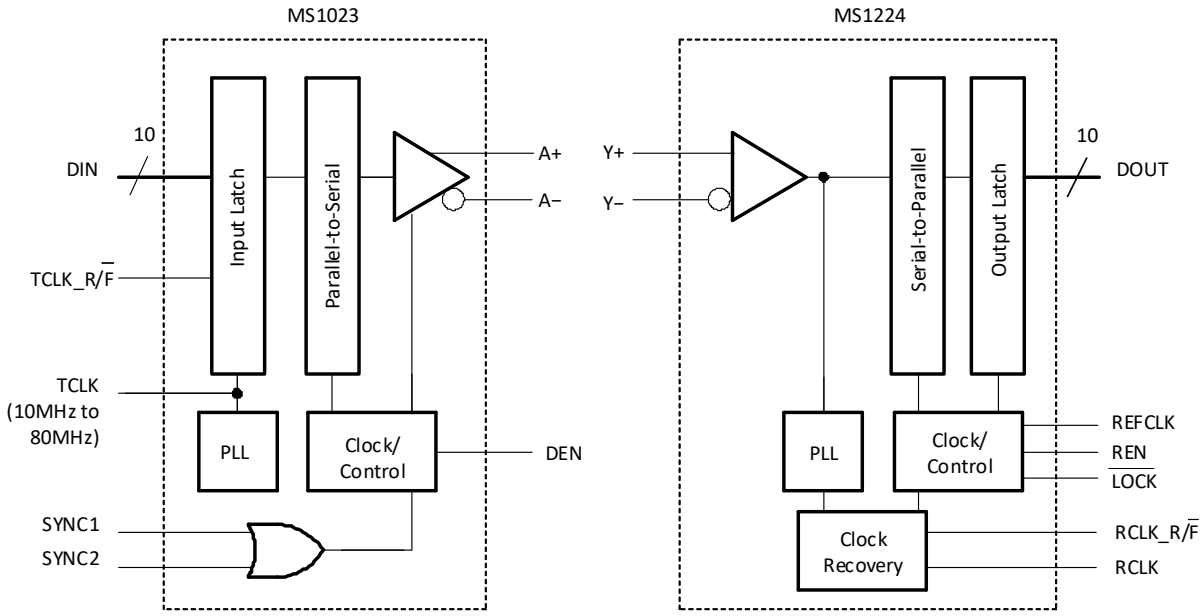


PIN DESCRIPTION

Pin	Name	Type	Description
MS1023			
1,2	SYNC1, SYNC2	I	SYNC1 and SYNC2 are ORed LVTTL Logical inputs. When at least one of pins is set high up for 6 TCLK cycles, the deserializer initiates transmission of at least 1026 SYNC samples. If after 1026 SYNC samples are sent, SYNC is still high, then the data transmission is continued until SYNC is low. And when SYNC is kept over 6 cycles, another 1026 SYNC samples are sent again.
3-12	DIN0-DIN9	I	Parallel LVTTL Digital Input
13	TCLK_R/$\overline{F}$	I	LVTTL Logic Input. Setting the pin low will ignore TCLK falling-edge data; Setting the pin high will ignore TCLK rising-edge data.
14	TCLK	I	LVTTL-Level Reference Clock Input. The MS1023 can receive 10MHz to 80MHz clock. TCLK ignores parallel data to input latch and provides a reference frequency for PLL at the same time.
15,16	DGND	-	Digital Circuit Ground
17,26	AVCC	-	Analog Circuit Power Supply (for PLL and Analog Circuit)
18,20,23,25	AGND	-	Analog Circuit Ground (for PLL and Analog Circuit)
19	DEN	I	LVTTL Logic Input. When it is low, enable LVDS serial output in high-impedance state; when it is high, enable serial data output.
21	DO-	O	Inverting LVDS Differential Output
22	DO+	O	Non-inverting LVDS Differential Output
24	$\overline{PWRDN}$	I	LVTTL Logic Input. Setting the pin low will turn off PLL, place the output in high-impedance state. And the device enters into low power-dissipation mode.
27,28	DVCC	-	Digital Circuit Power Supply

Pin	Name	Type	Description
MS1224			
1,12,13	AGND	-	Analog Circuit Ground (for PLL and Analog Circuit)
2	RCLK_R/$\overline{F}$	I	LVTTL Logic Input. Setting the pin low will ignore the RCLK falling-edge data; Setting the pin high will ignore the RCLK rising-edge data.
3	REFCLK	I	LVTTL Input. Provide REFCLK signal for PLL.
4,11	AVCC	-	Analog Circuit Power Supply (for PLL and Analog Circuit)
5	RI+	I	Serial Data Input, Non-inverting LVDS Differential Input
6	RI-	I	Serial Data Input, Inverting LVDS Differential Input
7	$\overline{PWRDN}$	I	LVTTL Logic Input. Setting the pin low will turn off PLL, place the output in high-impedance state. And the device enters into low power-dissipation mode. To enter into power-down mode, the pin must be set low for 16ns. As long as $\overline{PWRDN}$ is set to low, the device will enter into power-down mode.
8	REN	I	LVTTL Logic Input. Setting the pin low will make ROUT0-ROUT9 and RCLK in high-impedance state.
9	RCLK	O	LVTTL Output Recovered Clock. RCLK can ignore $R_{OUTX.}$
10	$\overline{LOCK}$	O	LVTTL Output. $\overline{LOCK}$ will be low when the deserializer PLL locks onto the embedded clock edge.
14,20,22	DGND	-	Digital Circuit Ground
28-24,19-15	ROUT0-ROUT9	O	Parallel LVTTL Data Output
21,23	DVCC	-	Digital Circuit Power Supply

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Range	Unit
V_{CC}		-3.0 ~ 4.0	V
LVTTL Input Voltage		-0.3 ~ V_{CC}+0.3	V
LVTTL Output Voltage		-0.3 ~ V_{CC}+0.3	V
LVDS Receiver Input Voltage		-0.3 ~ 3.9	V
LVDS Driver Output Voltage		-0.3 ~ 3.9	V
LVDS Output Short-circuit Duration		10	ms
ESD (HBM)		6k	V
ESD (MM)		200	V
Junction Temperature		150	°C
Storage Temperature	T_{stg}	-65 ~ 150	°C
Maximum Power Dissipation (T_A=25°C)		1.27	W
Power Dissipation Temperature Characteristics (T_A=25°C)		10.3	mW/°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Range			Unit
		Min	Typ	Max	
Power Supply	V_{CC}	3	3.3	3.6	V
Receiver Input Voltage Range		0		2.4	V
Receiver Input Common-mode Range	V_{CM}	V_{ID}/2		2.4-(V_{ID}/2)	
Power Supply Noise Voltage				100	mV_{PP}
Operating Temperature	T_A	-40	25	85	°C

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition	Min	Typ	Max	Unit
MS1023 LVCMOS/LVTTL DC						
High-level Input Voltage	V_{IH}		2		V_{CC}	V
Low-level Input Voltage	V_{IL}		GND		0.8	V
Input Clamp Voltage	V_{CL}	I_{CL}=-18mA		-0.86	-1.5	V
Input Current	I_{IN}	V_{IN}=0V or 3.6V	-200	±100	200	μA
MS1224 LVCMOS/LVTTL DC						
High-level Input Voltage	V_{IH}		2		V_{CC}	V
low-level Input Voltage	V_{IL}		GND		0.8	V
Input Clamp Voltage	V_{CL}	I_{CL}=-18mA		-0.62	-1.5	V
Input Current	I_{IN}	V_{IN}=0V or 3.6V	-200		200	μA
High-level Output Voltage	V_{OH}	I_{OH}=-5mA	2.2	3	V_{CC}	V
low-level Output Voltage	V_{OL}	I_{OL}=5mA	GND	0.25	0.5	V
Output Short-circuit Current	I_{OS}	V_{OUT}=0V	-15	-47	-85	mA
High-impedance Output Current	I_{OZ}	$\overline{PWRDN}$/REN=0.8V, V_{OUT}=0V or V_{CC}	-10	±1	10	μA
MS1023 LVDS DC						
Differential Output Voltage	V_{OD}	R_L=27Ω, See Figure1,2	350	450		mV
Differential Output Jitter Voltage	ΔV_{OD}				35	mV
Offset Voltage	V_{OS}		1.1	1.2	1.3	V
Offset Jitter Voltage	ΔV_{OS}			4.8	35	mV
Short-circuit Output Current	I_{OS}	D_O=0V,D_{INx}=high, $\overline{PWRDN}$/REN=2.4V		-10	-90	mA
High-impedance Output Current	I_{OZ}	$\overline{PWRDN}$/REN=0.8V, D_O=0V or V_{CC}	-10	±1	10	μA
Power-down Output Current	I_{OX}	V_{CC}=0V, D_O=0V or 3.6V	-20	±1	25	μA
Output Single-ended Capacitor	C_O				1±20%	pF
MS1224 LVDS DC						
Differential Threshold High-level Voltage	V_{TH}	V_{CM}=1.1V			50	mV
Differential Threshold Low-level Voltage	V_{TL}		-50			mV

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Input Current	I_{IN}	V_{IN}=2.4V, V_{CC}=0V or 3.6V		-10	±1	15	µA
		V_{IN}=0V, V_{CC}=0V or 3.6V		-10	±0.05	10	
Input Single-ended Capacitor	C_I				0.5±20%		pF
MS1023 Supply Current							
Serializer Power Supply Current	I_{CCD}	R_L=27Ω,	f=10MHz		20	25	mA
Worst Case		See Figure 3	f=80MHz		65	80	
Supply Current	I_{CCXD}	$\overline{PWRDN}$=0.8V			200	500	µA
MS1224 Supply Current							
Deserializer Power Supply	I_{CCR}	C_L=15pF	f=10MHz		15	35	mA
Current Worst Case		See Figure 5	f=80MHz		90	105	
Deserializer Power Supply in Power-down Mode	I_{CCXR}	$\overline{PWRDN}$=0.8V, REN=0.8V			0.36	1	mA

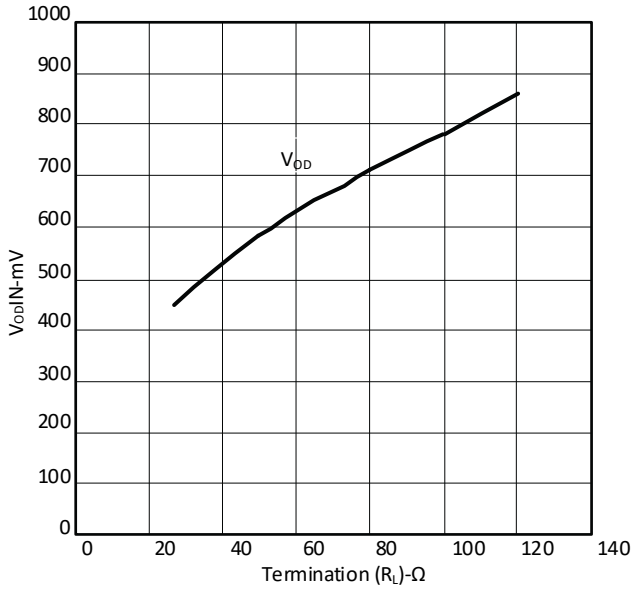


Figure 1. Typical V_{OD} Curve

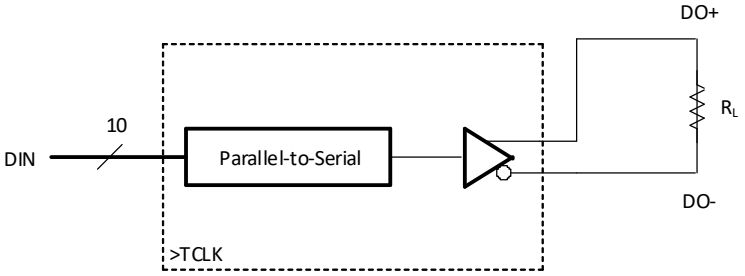


Figure 2. V_{OD} Output Diagram

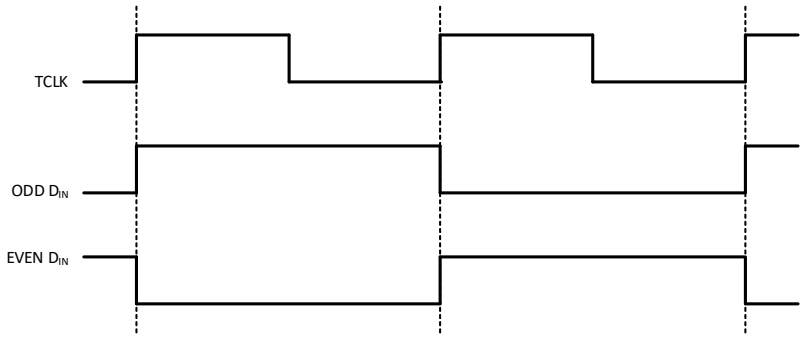


Figure 3. Worst-case Serializer I_{CC} Test Mode

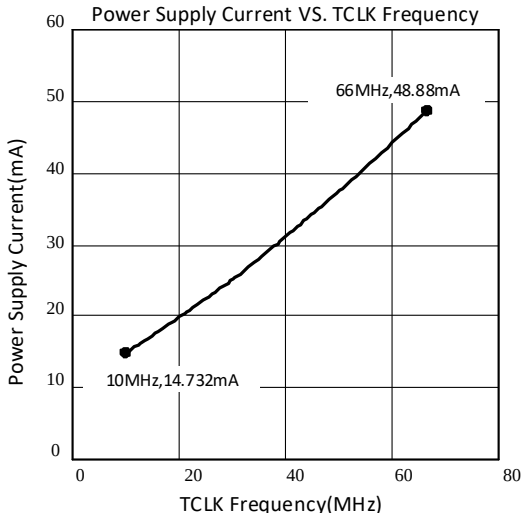


Figure 4. Power Supply Current VS. TCLK Frequency

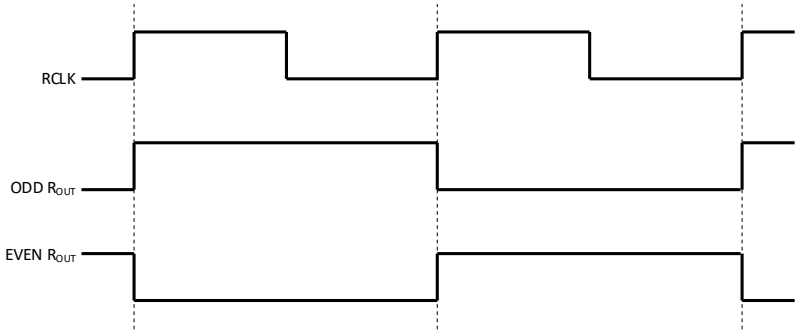


Figure 5. Worst-case Deserializer I_{CC} Test Mode

Device Start-up Procedure

Figure 6 shows that $\overline{\text{PWRDN}}$ pin keeps logic 0 on both serializer and deserializer until the power supply has reached at least 3V.

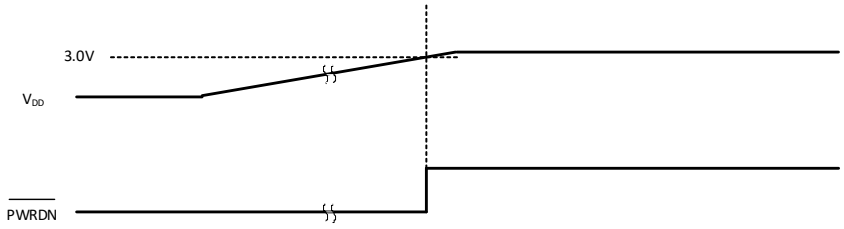


Figure 6. Device Start-up

Serializer Timing Requirements for TCLK

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Clock Period	t_{TCP}		15.15	T	100	ns
Clock High-level Time	t_{TCIH}		0.4T	0.5T	0.6T	ns
Clock Low-level Time	t_{TCIL}		0.4T	0.5T	0.6T	ns
TCLK Edge Time	$t_{t(CLK)}$	See Figure 7		3	6	ns
TCLK Input Jitter	t_{JIT}	See Figure 8			150	ps
Frequency Tolerance	F_t		-100		+100	ppm

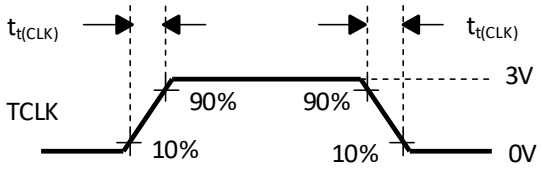


Figure 7. Serializer Input Clock Transition Time

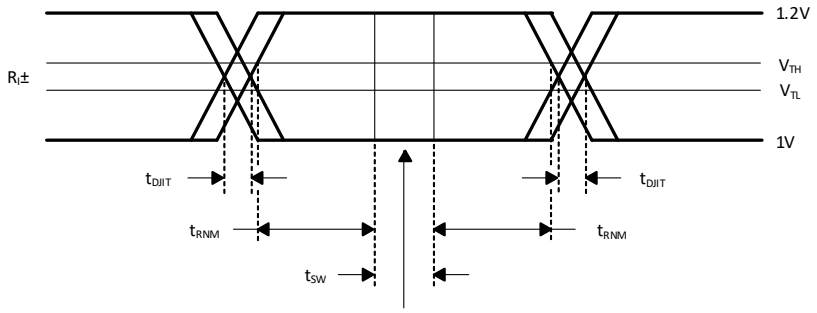


Figure 8. LVDS Input Margin Sampling

Serializer Switching Characteristics

Using previously proposed operating conditions, unless given test conditions.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Rising-edge Transition Time	$t_{TLH(L)}$	R_L=27Ω, C_L=10pF to GND,		0.2	0.4	ns
Falling-edge Transition Time	$t_{LTH(L)}$	See Figure 9		0.25	0.4	ns
Data Setup Time	$t_{su(DI)}$	See Figure 10	0.5			ns
Data Hold Time	$t_{su(DI)}$		4			ns
High-to-High-impedance Delay	$t_{d(HZ)}$	R_L=27Ω, C_L=10pF to GND, See Figure 11,12		2.5	5	ns
Low-to-High-impedance Delay	$t_{d(LZ)}$			2.5	5	
High-to-High-impedance-to-High Delay	$t_{d(ZH)}$			5	10	
High-to-High-impedance-to-Low Delay	$t_{d(ZL)}$			6.5	10	

Parameter	Symbol	Condition	Min	Typ	Max	Unit
SYNC Pulse Duration	$t_{w(SPW)}$	See Figure 13	6×t_{TCP}			ns
Serializer PLL Lock Time	$t_{(PLD)}$		1026×t_{TCP}			ns
Serializer Delay	$t_{d(S)}$	See Figure 14	t_{TCP}+1	t_{TCP}+2	t_{TCP}+3	ns
Deterministic Jitter Amplitude	t_{DJIT}	R_L=27Ω, C_L=10pF to GND			230	ps
					150	
Random Jitter Amplitude	t_{RJIT}	R_L=27Ω, C_L=10pF to GND		10	9	ps

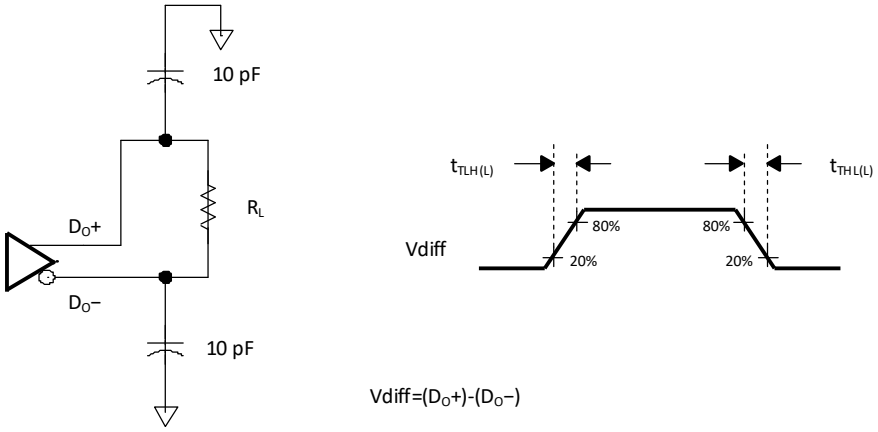


Figure 9. Serializer LVDS Output Load and Transition Time

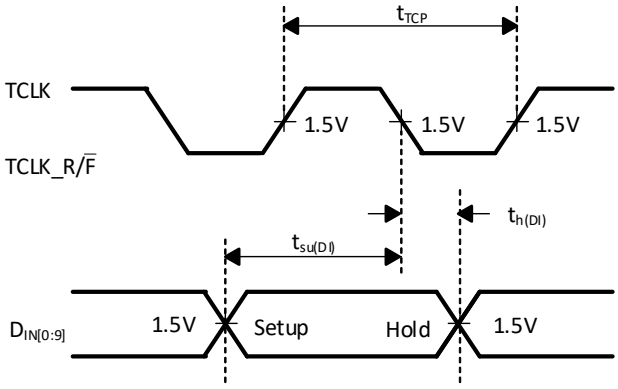


Figure 10. Serializer Setup/Hold Time

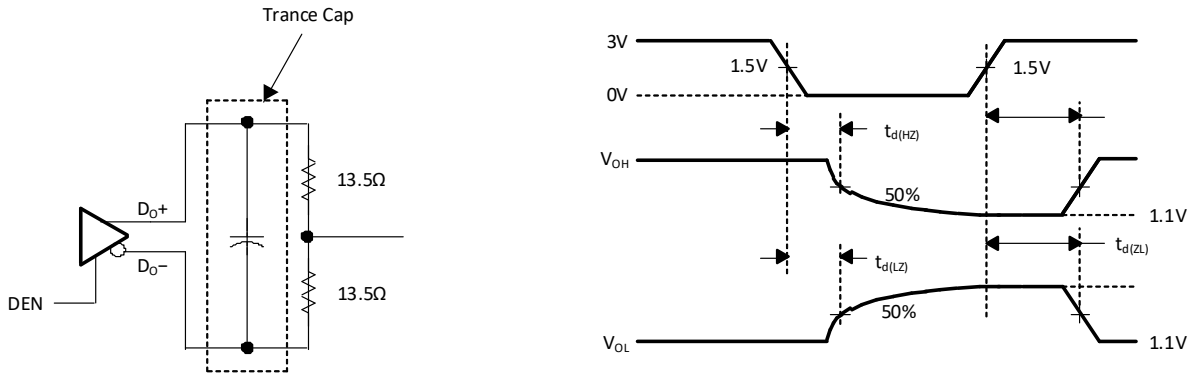


Figure 11. Serializer High-impedance-state Test Circuit and Timing

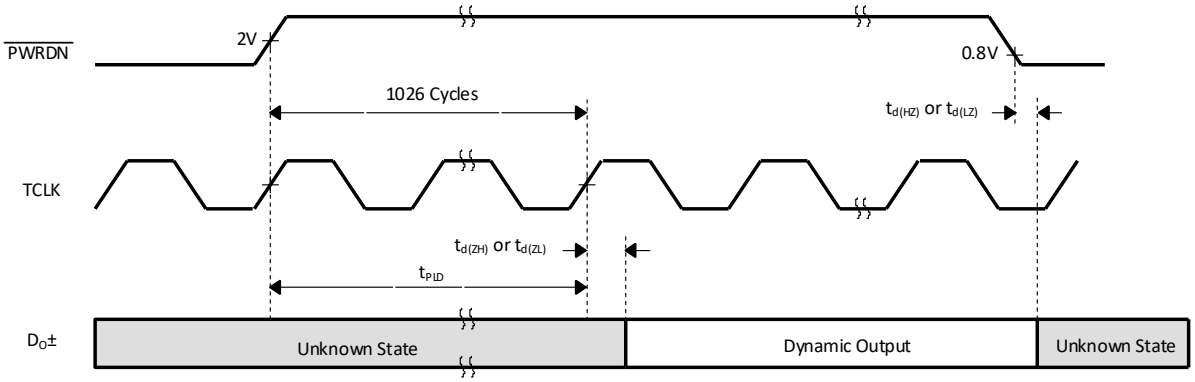


Figure 12. Serializer PLL Lock Time and $\overline{\text{PWRDN}}$ High-impedance-state Delay

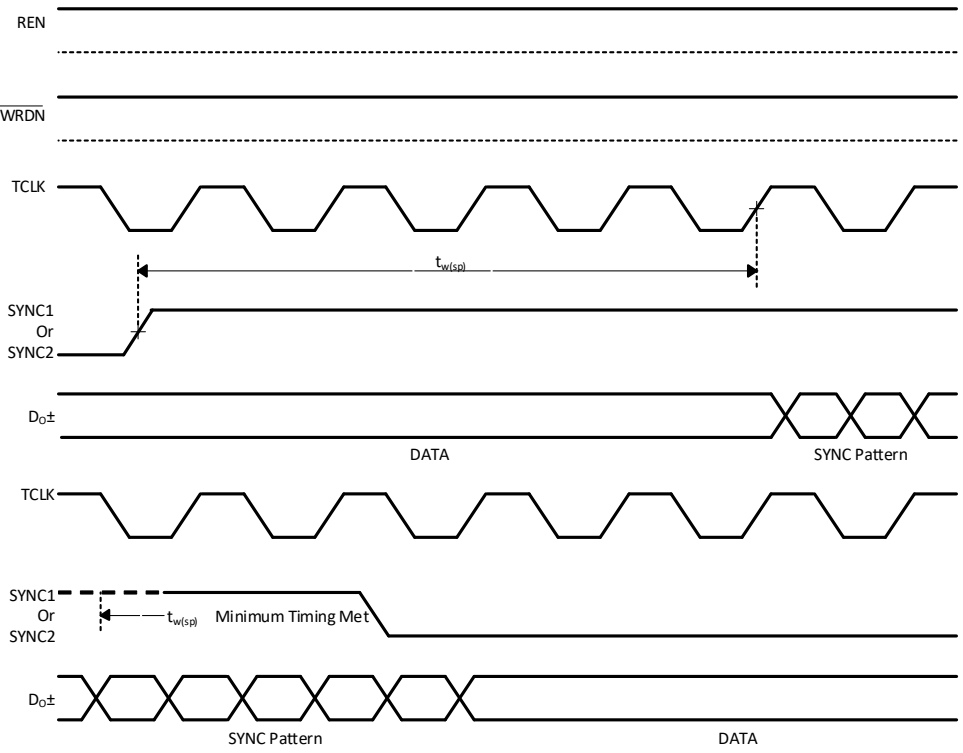


Figure 13. SYNC Timing Delay

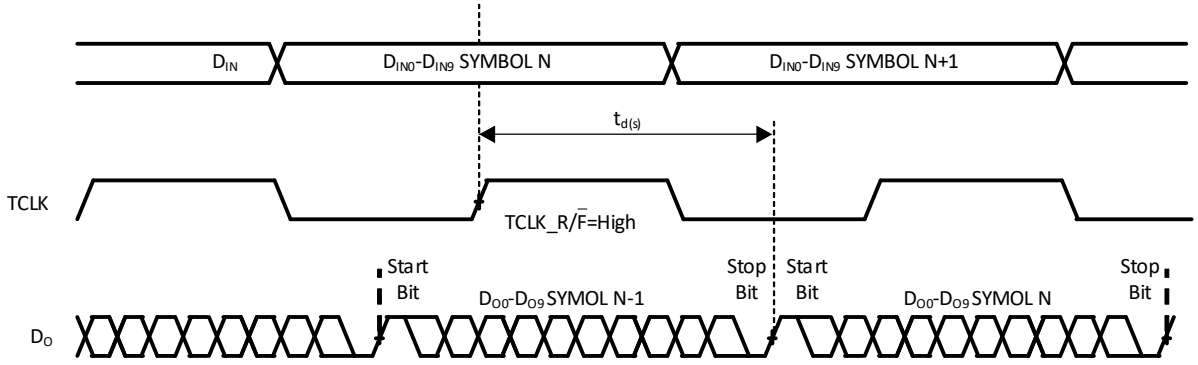


Figure 14. Serializer Delay

Deserializer Timing Requirements for REFCLK

Using previously proposed working conditions, unless given test conditions.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
REFCLK Period	t_{RFCP}		15.15	T	100	ns
REFCLK Duty Cycle	t_{RFDC}		30	50	70	%
REFCLK Edge Time	$t_{t(RF)}$			3	6	ns
Frequency Tolerance	F_t		-100		+100	ppm

Deserializer Switching Characteristics

Parameter	Symbol	Condition	Pin/Frequency	Min	Typ	Max	Unit
Receiver Output Clock Period	$t_{(RCP)}$	$t_{(RCP)}=t_{(TCP)}$, See Figure 14	RCLK	15.15		100	ns
Low-to-High Transition Time	$t_{TLH(C)}$	CL=15pF, See Figure 15	R_{OUT0}-R_{OUT9}, $\overline{LOCK}$, RCLK		1.2	2.5	ns
High-to-Low Transition Time	$t_{THL(C)}$				1.1	2.5	ns
Deserializer Delay	$t_{d(D)}$	Room Temperature, 3.3V, See Figure 16	10MHz	$1.75\times t_{(RCP)}$ +4.2		$1.75\times t_{(RCP)}$ +12.6	ns
			80MHz	$1.75\times t_{(RCP)}$ +7.4		$1.75\times t_{(RCP)}$ +9.7	
ROUTX Data Valid before RCLK	$t_{(ROS)}$	See Figure 17	RCLK 10MHz	$0.4\times t_{(RCP)}$	$0.5\times t_{(RCP)}$		ns
			RCLK 80MHz	$0.4\times t_{(RCP)}$	$0.5\times t_{(RCP)}$		
ROUTX Data Valid after RCLK	$t_{(ROH)}$		10MHz	$-0.4\times t_{(RCP)}$	$-0.5\times t_{(RCP)}$		
			80MHz	$-0.4\times t_{(RCP)}$	$-0.5\times t_{(RCP)}$		
Clock Duty Cycle	$t_{(RDC)}$			40	50	60	%
High-to-High-impedance Delay	$t_{d(HZ)}$	See Figure 18	R_{OUT0}-R_{OUT9}		6.5	8	ns
Low-to-High-impedance Delay	$t_{d(LZ)}$				4.7	8	
High-impedance-to-High Delay	$t_{d(HR)}$				5.3	8	
High-impedance-to-Low Delay	$t_{d(ZL)}$				4.7	8	

Parameter	Symbol	Condition	Pin/Frequency	Min	Typ	Max	Unit
Deserializer PLL Lock Time	$t_{(DSR1)}$	See Figure 19,20	10MHz			$850\times t_{RFCP}$	μs
			80MHz			$850\times t_{RFCP}$	
	$t_{(DSR2)}$		10MHz			2	
			80MHz			0.303	
High-impedance-to-High Delay (Start-up)	$t_{d(ZHLK)}$		$\overline{LOCK}$			3	ns
Deserializer Noise Limit	t_{RNM}	See Figure 8	10MHz		3680		ps

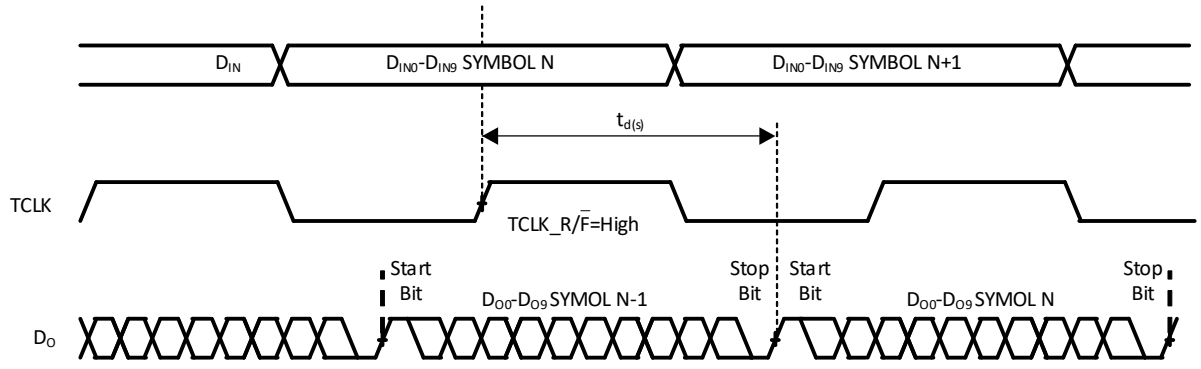


Figure 14. Serializer Delay

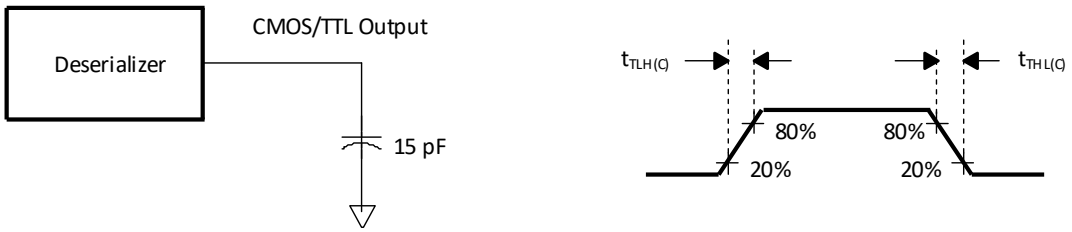


Figure 15. Deserializer CMOS/TTL Output Load and Transmission Time

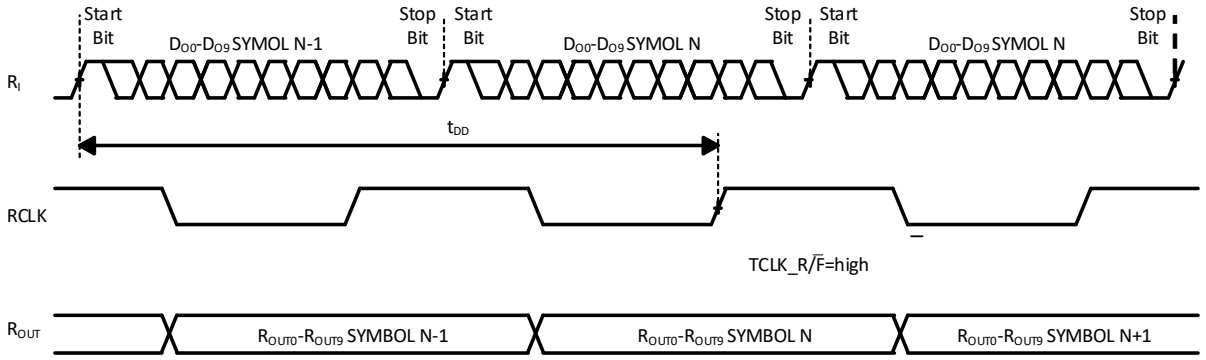


Figure 16. Deserializer Delay

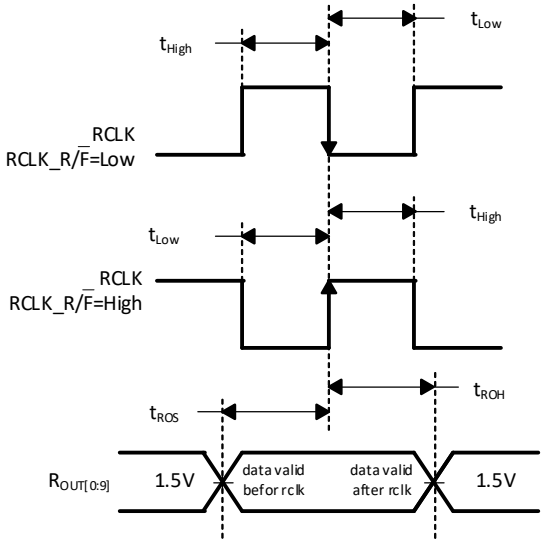


Figure 17. Deserializer Data Valid Output Timing

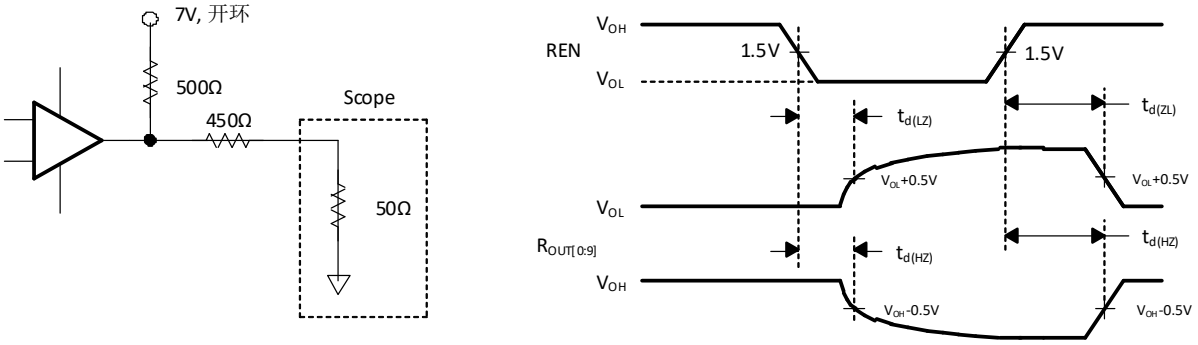


Figure 18. Deserializer High-impedance-state Test Circuit and Timing

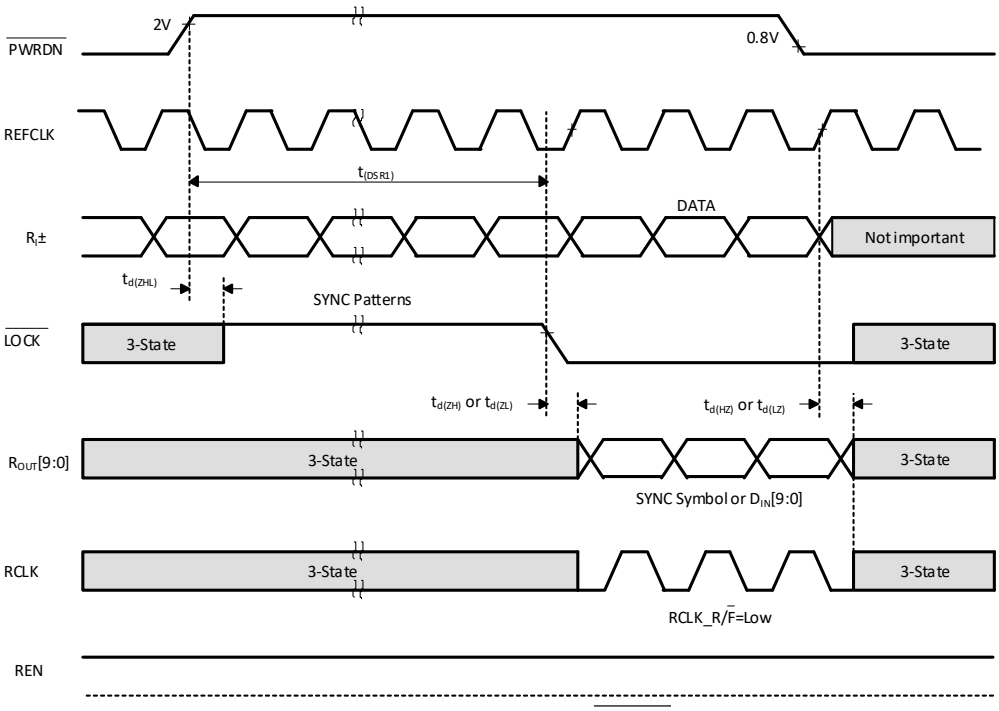


Figure 19. Deserializer PLL Lock Time and $\overline{\text{PWRDN}}$ 3-state Delay

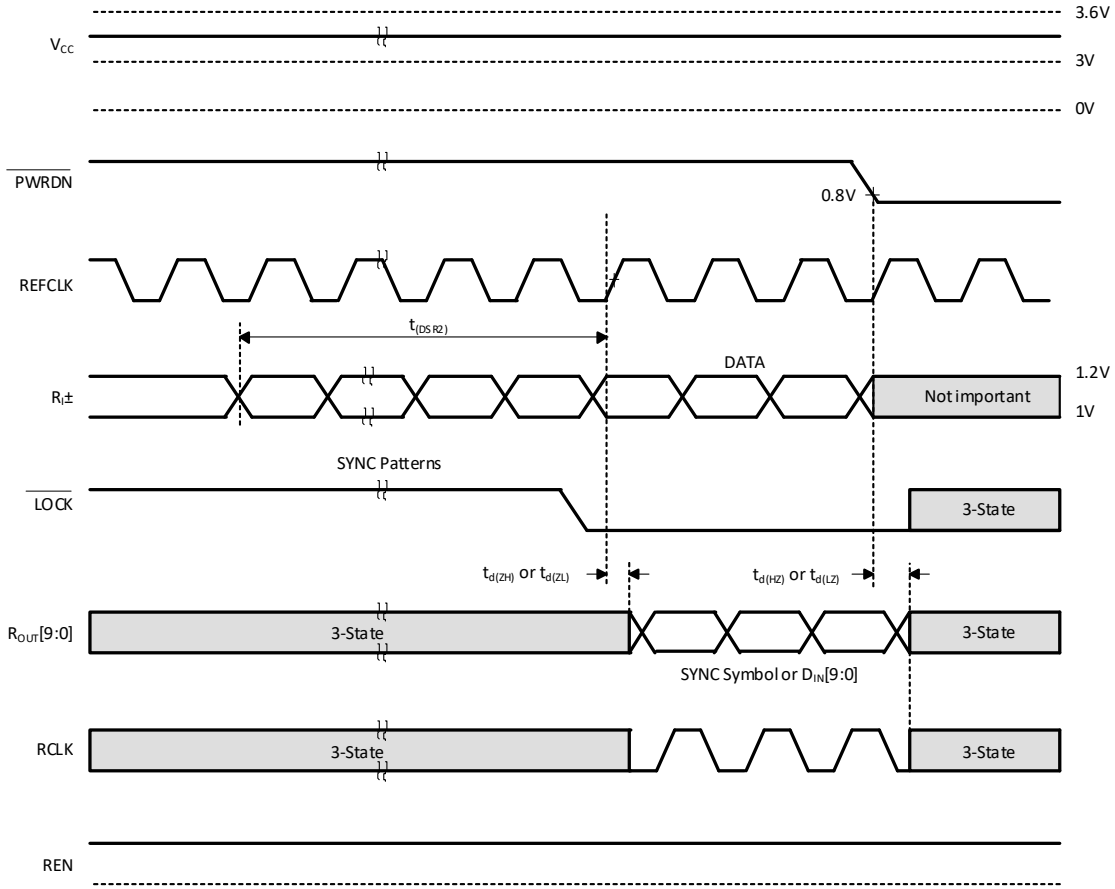


Figure 20. Deserializer PLL Lock Time during Synchronization

FUNCTION DESCRIPTION

The MS1023 and the MS1224 are a pair of 10-bit serializer/deserializer chips, which is designed for transmitting data over differential backplanes or unshielded twisted pair (UTP) from 10MHz to 80MHz. This pair of chips has five operation modes: initialization mode, synchronization mode, data transmission mode, power-down mode and high-impedance transmission mode. Each operation mode is described in sections below.

Initialization Mode

Before data transmission is started, the device must be initiated. The initialization is related to the synchronization of the serializer and the lock of local clock for deserializer PLL.

When Vcc is applied to the serializer or the deserializer, output response is in high-impedance state. At the same time, internal power supply circuit makes the internal circuit disabled. When Vcc reaches 2.45V, PLL in starts to lock the local clock. For serializer, the local clock is the transmit clock (TCLK) provided by an external clock source. For deserializer, local clock must correspond to the input of REFCLK pin. When PLL locks to TCLK, the serializer outputs remain in the high-impedance state.

Synchronization Mode

To receive valid data, the deserializer PLL must be synchronized to the serializer. Synchronization can be completed in the following two ways:

Fast Synchronization: The serializer has the ability to send specified SYNC sample signal, which consists of six ones and six zeros, whose value conversions are determined by input clock rate. SYNC sample transmission enables the deserializer to lock to the serializer signal within a certain time frame. The SYNC1 and SYNC2 inputs of the serializer determines whether SYNC sample signals is transmitted or not. When continuously receiving valid SYNC1 or SYNC2 pulse (time width exceeds 6 clock cycles), SYNC sample signals will be sent.

When the deserializer detects edge transitions at the LVDS input, it will try to lock to embedded clock information. The deserializer $\overline{\text{LOCK}}$ output remains high, and PLL locks to input data or SYNC sample signals from the serializer at the same time. When the deserializer locks to LVDS data, the $\overline{\text{LOCK}}$ output goes low. When $\overline{\text{LOCK}}$ is low, the deserializer starts to recover LVDS input data. One way is to directly connect the deserializer $\overline{\text{LOCK}}$ output to SYNC1 or SYNC2.

Random-lock Synchronization: The deserializer can attain clock from the data stream without requiring the serializer to send specified synchronization mode signal, which allows the MS1224 to operate in open-loop application. It is important that the deserializer supports hot insertion during operation. In the open-loop or hot-insertion case, it is assumed that data is essentially random. Therefore, because lock time varies depending on the characteristics of data stream, so the precise time can not be predicted. When the deserializer starts up, the first constrain on the random lock time is the initial phase between input data and REFCLK.

The data in the data stream can also affect lock time. If a special mode is repetitive, the deserializer may enter false lock recognizing input data mode as start/stop bits, which is known as repetitive multitransition (RMT). See Figure 21 for RMTexample. RMT is formed when more than one low-high transitions occur per clock cycle over multiple cycles. In the worst case, the deserializer may lock to data mode instead of clock. The deserializer includes circuit, which can detect possible error clock. Through detection, the circuit prevents the output from becoming active until the potential false clock changes. It is observed that RMT mode only affects the lock time of the deserializer. At the same time, once the deserializer is locked, RMT mode can not affect the deserializer state (even though same data boundary happens per cycle). The deserializer can not lock until it finds a special/four consecutive clocks of data boundary (STOP/START bits) at the same position.

The deserializer keeps locked until it can not detect the same data boundary (STOP/START bits) for consecutive four clock cycles. Then, the deserializer unlocks and finds new data boundary (STOP/START bits). In the case of loss of synchronization, the $\overline{LOCK}$ output goes high and the outputs (including RCLK) are in high-impedance state. The user system should monitor $\overline{LOCK}$ pin to prevent a loss of synchronization. When detecting the loss of lock, if the reset lock cannot be completed within a specified time, it is desirable to send SYNC sample signals for resynchronization. However, the deserializer can lock to random data as mentioned above.

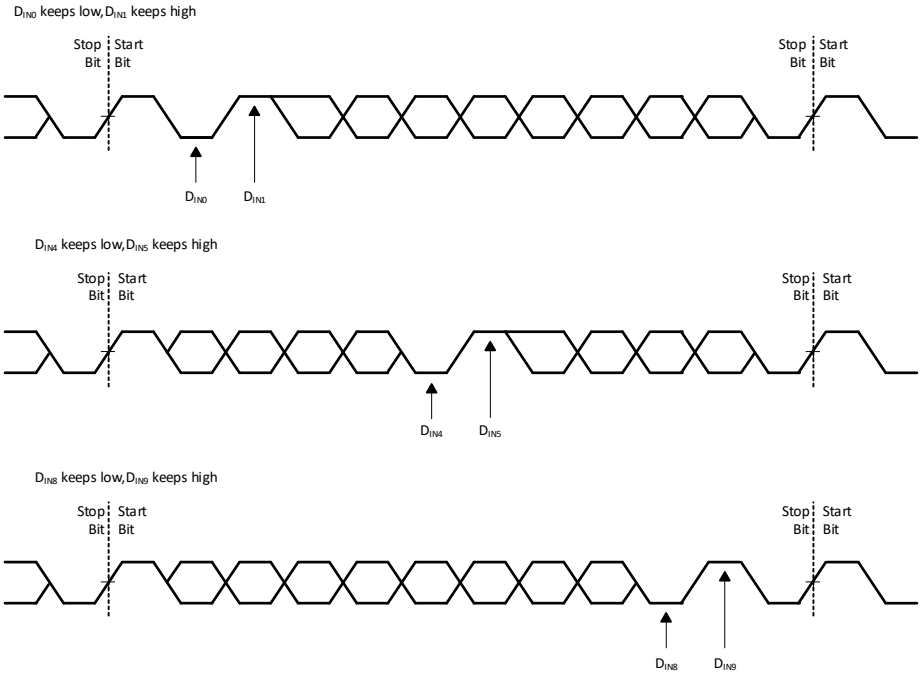


Figure 21. RMT Mode Example

Data Transmission Mode

After initialization and synchronization are completed, the serializer receives parallel data from DIN0 to DIN9. The serializer locks to input data using the clock. TCLK_R/$\overline{F}$ pin select edge to filter input data. If any one of SYNC inputs is high over 6 TCLK cycles, DIN0-DIN9 data will be ignored regardless of the selected clock edge and 1026 clock cycles of SYNC sample signals are sent.

After determing the used clock edge, a start and stop bit are embedded in the registers of per-frame data. The start bit keeps high and the stop bit keeps low. In the serial data stream, the start and stop bits are as embedded clock information.

The serializer transmits serial data and the embedded clock bits (10+2bits) at 12 times the TCLK frequency. For example, if TCLK is 80MHz, the serial rate is 80×12 = 960Mbps. Because there are only 10 bits input data, the valid data rates should be 10 times the TCLK frequency. For example, if the clock is 80MHz, the valid data rate is 80×10 = 800Mbps. While data source provided for TCLK is between 10MHz and 80MHz.

The deserializer output (DO±) can drive point-to-point connection or limited multipoint or multidrop backplanes. When the enable pin (DEN) and $\overline{\text{PWRDN}}$ are high, SYNC1 and SYNC2 are low, the outputs transmit normal data. When DEN is low, the serializer outputs are in high-impedance state.

Once the deserializer is synchronized to the serializer, the $\overline{\text{LOCK}}$ pin output is low. The deserializer locks to embedded clock and also uses the clock to recover the serialized data. ROUT data is valid when $\overline{\text{LOCK}}$ is low, so the ROUT0-ROUT9 is valid. The ROUT0-ROUT9 is ignored by RCLK. The special RCLK polarity is determined by the RCLK_R/$\overline{F}$. When the clock is 80MHz, the outputs of the ROUT0-ROUT9, $\overline{\text{LOCK}}$ and the RCLK can drive three-terminated CMOS input gates (the total capacitors connected to three pins are 15pF).

Power-down Mode

When there is no transmission requirement, the power-down mode can be used. The power-down state that the serializer and the deserilizer use is a kind of low power-dissipation sleep mode and can reduce power dissipation. When $\overline{\text{PWRDN}}$ and DEN are set low, the deserializer enters power-down mode. When $\overline{\text{PWRDN}}$ is low, the serializer enters power-down mode. In power-down mode, PLL and output are in high-impedance state, which makes the load current disabled and reduces power supply current to microampere level (μA level). To exit power-down mode, must drive $\overline{\text{PWRDN}}$ high.

Before the valid data exchanges between the serializer and the deserializer recover, the devices connected to each other must be initialized and synchronized again. The initialization of the serializer takes 1026 TCLK cycles. The deserializer initializes and drives $\overline{\text{LOCK}}$ high until locks to LVDS clock.

High-impedance Mode

When DEN is set low, the serializer is in high-impedance state, which makes all output pins in high-impedance state. When drive DEN high, the serializer returns to the previous state, and all other control pins (SYNC1,SYNC2, $\overline{\text{PWRDN}}$,TCLK_R/$\overline{\text{F}}$) remain static at the same time. When the REN pin is set low, the deserializer enters the high-impedance state. Correspondingly, the output pins of receiver chip (ROUT0-ROUT9) and RCLK enter the high-impedance state. The $\overline{\text{LOCK}}$ remains active to track the status of PLL.

Table 1. Serial-to-Parallel Truth Table

Input		Output		
$\overline{\text{PWRDN}}$	REB	ROUT (0:9)[1]	$\overline{\text{LOCK}}$ [2]	RCLK[1,3]
H	H	Z	H	Z
H	H	Active	L	Active
L	×	Z	Z	Z
H	L	Z	Active	Z

Note:

1. When $\overline{\text{LOCK}}$ is set high, ROUT and RCLK are in unknown state.
2. $\overline{\text{LOCK}}$ output reflects the state that the deserializer deals with data stream.
3. RCLK active indicates that the RCLK is working if the deserializer is locked. RCLK timing related to ROUT is determined by RCLK_R/$\overline{\text{F}}$.

Bias Fault Protection for the MS1224

The MS1224 has an input threshold sensitivity of ±50mV, which allows the MS1224 to have greater differential noise limit input. However, in the case where the receiver is not passively driven, the increased sensitivity of the MS1224 may recognize noise as input signal and cause unpredictable lock. This may occur when the input is floating. The MS1224 has an on-chip fault protection circuit that drives input and $\overline{\text{LOCK}}$ signal high. The response time of fault protection circuit depends on the characteristics of internal connected circuit.

TYPICAL APPLICATION DIAGRAM

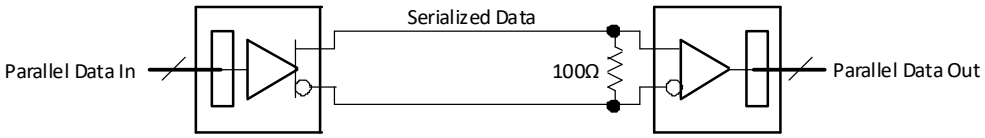


Figure 22. Single-ended Point-to-point Connection

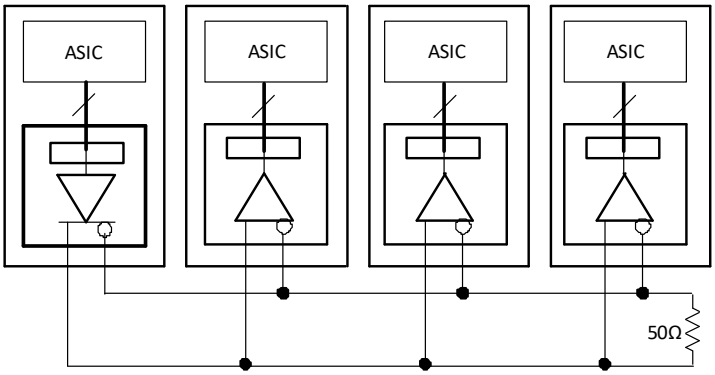
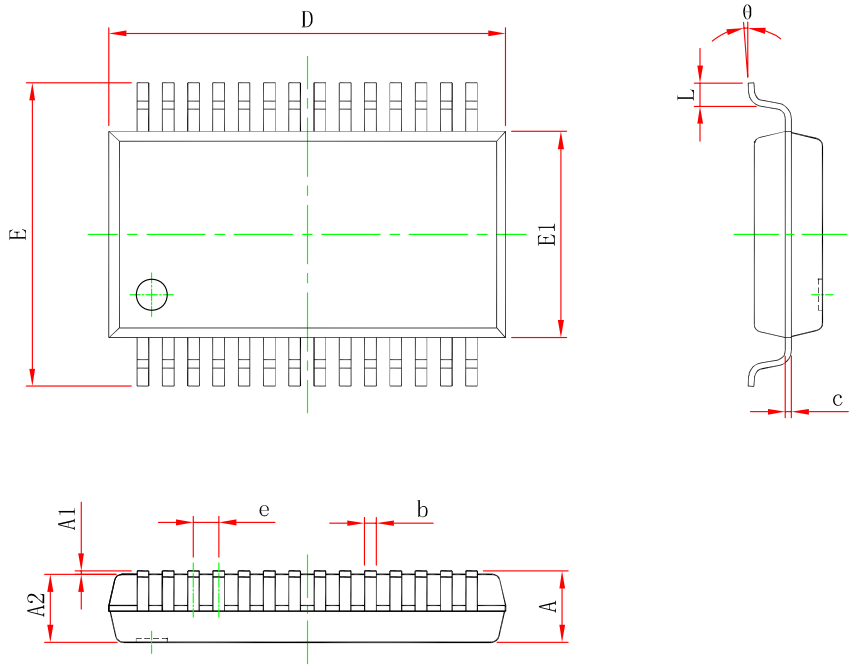


Figure 23. Multiconnection Configuration

PACKAGE OUTLINE DIMENSIONS

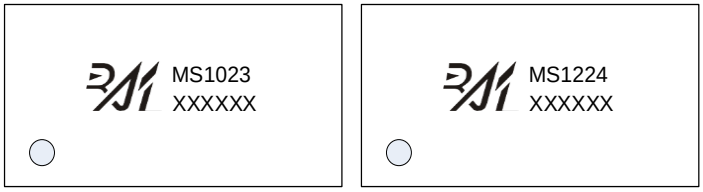
SSOP28



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	-	2.000	-	0.079
A1	0.050	-	0.002	-
A2	1.650	1.850	0.065	0.073
b	0.220	0.380	0.009	0.015
c	0.090	0.250	0.004	0.010
D	9.900	10.500	0.390	0.413
E	7.400	8.200	0.291	0.323
E1	5.000	5.600	0.197	0.220
e	0.650BSC		0.026BSC	
L	0.550	0.950	0.022	0.037
θ	0°	8°	0°	8°

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description



Product Name: MS1023, MS1224

Product Code: XXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specifications

Device	Package	Piece/Reel	Reel/Box	Piece /Box	Box/Carton	Piece/Carton
MS1023	SSOP28	2500	1	2500	8	20000
MS1224	SSOP28	2500	1	2500	8	20000

STATEMENT

- All Revision Rights of Datasheets Reserved for Ruimeng. Don’ t release additional notice.

  Customer should get latest version information and verify the integrity before placing order.
- When using Ruimeng products to design and produce, purchaser has the responsibility to observe safety standard and adopt corresponding precautions, in order to avoid personal injury and property loss caused by potential failure risk.
- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1、The operator shall ground through the anti-static wristband.

2、The equipment shell must be grounded.

3、The tools used in the assembly process must be grounded.

4、Must use conductor packaging or anti-static materials packaging or transportation.

+86-571-89966911

Rm701, No.9 Building, No. 1 WeiYe Road, Puyan Street, Binjiang District, Hangzhou, Zhejiang

http:// www.relmon.com