



# Ultra-Low Noise, Precision OPERATIONAL AMPLIFIERS

## FEATURES

- **LOW NOISE:**  $4.5\text{nV}/\sqrt{\text{Hz}}$  max at 1kHz
- **LOW OFFSET:** 100 $\mu\text{V}$  max
- **LOW DRIFT:** 0.4 $\mu\text{V}/^\circ\text{C}$
- **HIGH OPEN-LOOP GAIN:** 117dB min
- **HIGH COMMON-MODE REJECTION:** 100dB min
- **HIGH POWER-SUPPLY REJECTION:** 94dB min
- **FITS OP-07, OP-05, AD510, AND AD517 SOCKETS**

## APPLICATIONS

- PRECISION INSTRUMENTATION
- DATA ACQUISITION
- TEST EQUIPMENT
- PROFESSIONAL AUDIO EQUIPMENT
- TRANSDUCER AMPLIFIERS
- RADIATION HARD EQUIPMENT

## DESCRIPTION

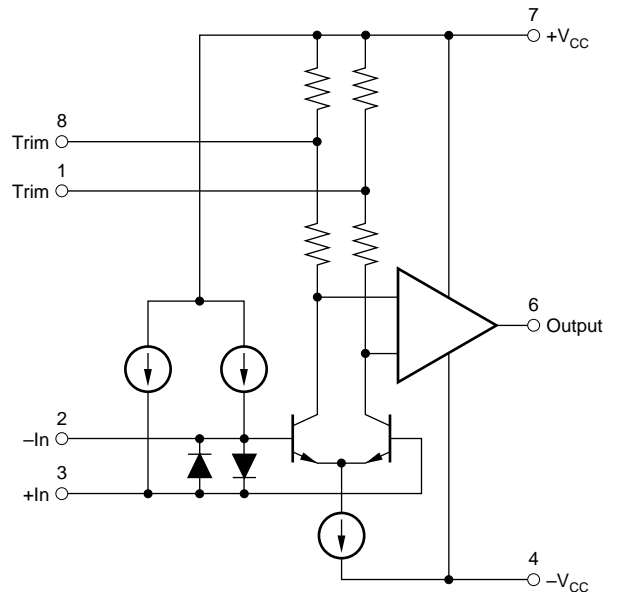
The OPA27 and OPA37 are ultra-low noise, high-precision monolithic operational amplifiers.

Laser-trimmed thin-film resistors provide excellent long-term voltage offset stability and allow superior voltage offset compared to common zener-zap techniques.

A unique bias current cancellation circuit allows bias and offset current specifications to be met over the full  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  temperature range.

The OPA27 is internally compensated for unity-gain stability. The decompensated OPA37 requires a closed-loop gain  $\geq 5$ .

The Texas Instruments' OPA27 and OPA37 are improved replacements for the industry-standard OP-27 and OP-37.



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## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Supply Voltage .....	±22V
Internal Power Dissipation <sup>(2)</sup> .....	500mW
Input Voltage .....	±V <sub>CC</sub>
Output Short-Circuit Duration <sup>(3)</sup> .....	Indefinite
Differential Input Voltage <sup>(4)</sup> .....	±0.7V
Differential Input Current <sup>(4)</sup> .....	±25mA
Storage Temperature Range .....	-55°C to +125°C
Operating Temperature Range .....	-40°C to +85°C
Lead Temperature:	
P (soldering, 10s) .....	+300°C
U (soldering, 3s) .....	+260°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Maximum package power dissipation versus ambient temperature. (2) To common with ±V<sub>CC</sub> = 15V. (4) The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

## PACKAGE/ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	PACKAGE-LEAD	$\theta_{JA}$	PACKAGE DRAWING	PACKAGE MARKING
OPA27	DIP-8	100°C/W	P	OPA27GP
OPA27	SO-8	160°C/W	D	OPA27U
OPA37	DIP-8	100°C/W	P	OPA37GP
OPA37	SO-8	160°C/W	D	OPA37U

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

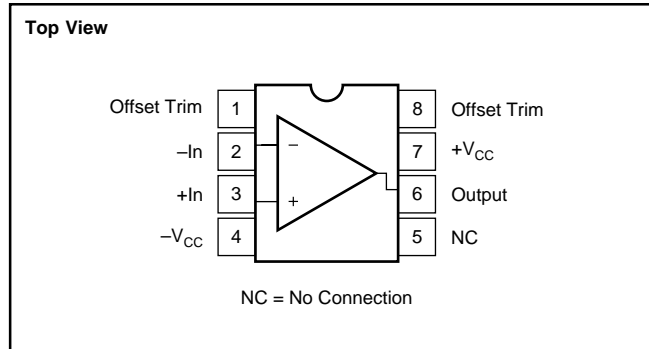


## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PIN CONFIGURATION



# ELECTRICAL CHARACTERISTICS

At  $V_{CC} = \pm 15V$  and  $T_A = +25^\circ C$ , unless otherwise noted.

PARAMETER	CONDITIONS	OPA27 OPA37			UNITS
		MIN	TYP	MAX	
<b>INPUT NOISE</b> <sup>(6)</sup> Voltage, $f_o = 10Hz$ $f_o = 30Hz$ $f_o = 1kHz$ $f_B = 0.1Hz$ to $10Hz$ Current, <sup>(1)</sup> $f_o = 10Hz$ $f_o = 30Hz$ $f_o = 1kHz$			3.8 3.3 3.2 0.09 1.7 1.0 0.4	8.0 5.6 4.5 0.25	$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$ $\mu V_{PP}$ $pA/\sqrt{Hz}$ $pA/\sqrt{Hz}$ $pA/\sqrt{Hz}$
<b>OFFSET VOLTAGE</b> <sup>(2)</sup> Input Offset Voltage Average Drift <sup>(3)</sup> Long Term Stability <sup>(4)</sup>  Supply Rejection	$T_{A\ MIN}$ to $T_{A\ MAX}$   $\pm V_{CC} = 4$ to $18V$ $\pm V_{CC} = 4$ to $18V$		$\pm 25$ $\pm 0.4$ 0.4  120 $\pm 1$	$\pm 100$ $\pm 1.8^{(6)}$ 2.0   $\pm 20$	$\mu V$ $\mu V/^\circ C$ $\mu V/mo$  dB $\mu V/V$
<b>BIAS CURRENT</b> Input Bias Current			$\pm 15$	$\pm 80$	nA
<b>OFFSET CURRENT</b> Input Offset Current			10	75	nA
<b>IMPEDANCE</b> Common-Mode				$2 \parallel 2.5$	$G\Omega \parallel pF$
<b>VOLTAGE RANGE</b> Common-Mode Input Range Common-Mode Rejection	$V_{IN} = \pm 11VDC$	$\pm 11$ 100	$\pm 12.3$ 122		V dB
<b>OPEN-LOOP VOLTAGE GAIN, DC</b>	$R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	117	124 124		dB dB
<b>FREQUENCY RESPONSE</b> Gain-Bandwidth Product <sup>(5)</sup>  Slew Rate <sup>(5)</sup>  Settling Time, 0.01%	OPA27 OPA37 $V_O = \pm 10V,$ $R_L = 2k\Omega$ OPA27, $G = +1$ OPA37, $G = +5$ OPA27, $G = +1$ OPA37, $G = +5$	$5^{(6)}$ $45^{(6)}$   $1.7^{(6)}$ $11^{(6)}$	8 63   1.9 11.9 25 25		MHz MHz  V/ $\mu s$ V/ $\mu s$ $\mu s$ $\mu s$
<b>RATED OUTPUT</b> Voltage Output  Output Resistance Short Circuit Current	$R_L \geq 2k\Omega$ $R_L \geq 600\Omega$ DC, Open Loop $R_L = 0\Omega$	$\pm 12$ $\pm 10$	$\pm 13.8$ $\pm 12.8$ 70 25		V V $\Omega$ mA
<b>POWER SUPPLY</b> Rated Voltage Voltage Range, Derated Performance Current, Quiescent	$I_O = 0mADC$	$\pm 4$	$\pm 15$  3.3	$\pm 22$ 5.7	VDC VDC mA
<b>TEMPERATURE RANGE</b> Specification Operating		$-40$ $-40$		$+85$ $+85$	$^\circ C$ $^\circ C$

NOTES: (1) Measured with industry-standard noise test circuit (Figures 1 and 2). Due to errors introduced by this method, these current noise specifications should be used for comparison purposes only. (2) Offset voltage specification are measured with automatic test equipment after approximately 0.5 seconds from power turn-on. (3) Unnulled or nulled with  $8k\Omega$  to  $20k\Omega$  potentiometer. (4) Long-term voltage offset vs time trend line does not include warm-up drift. (5) Typical specification only on plastic package units. Slew rate varies on all units due to differing test methods. Minimum specification applies to open-loop test. (6) This parameter specified by design.

# ELECTRICAL CHARACTERISTICS (Cont.)

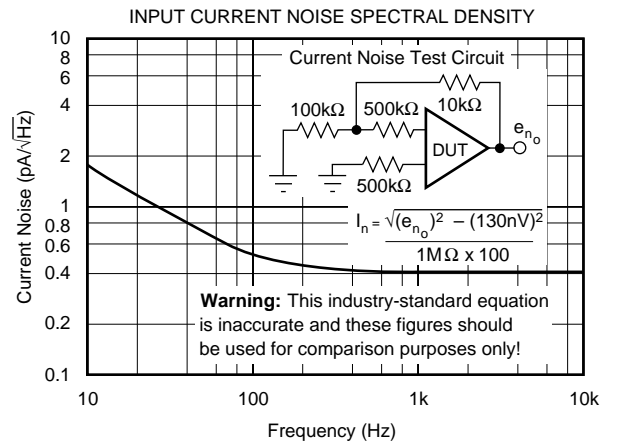
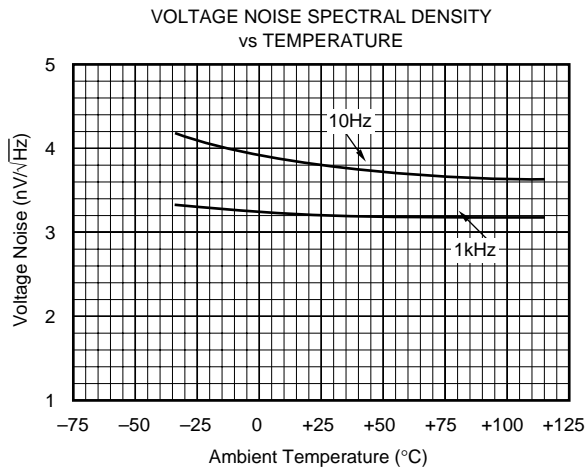
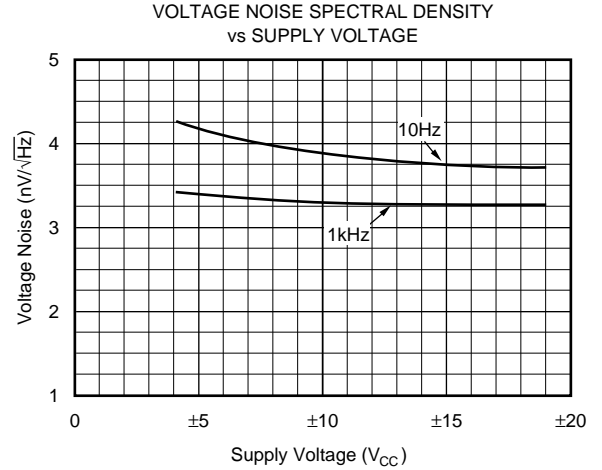
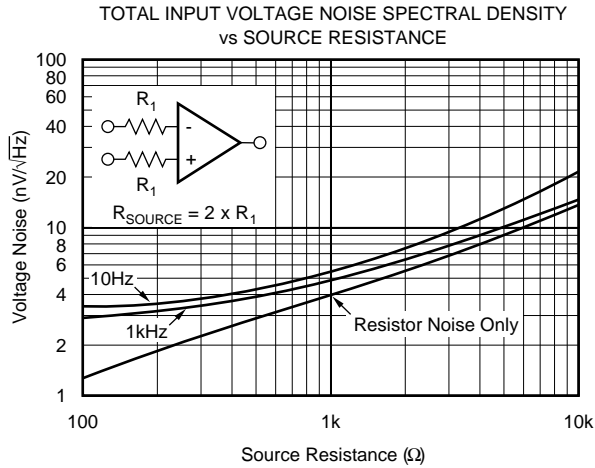
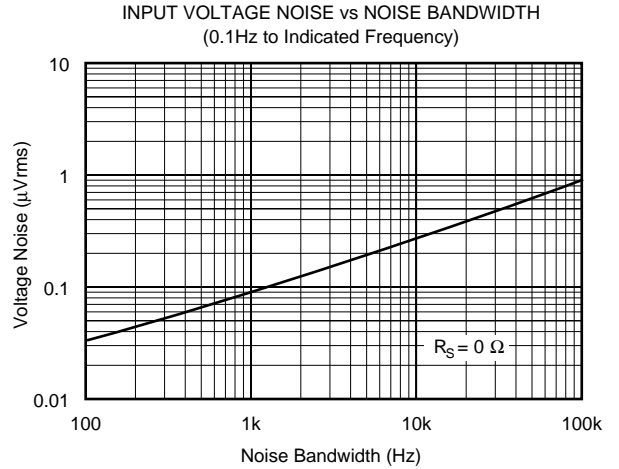
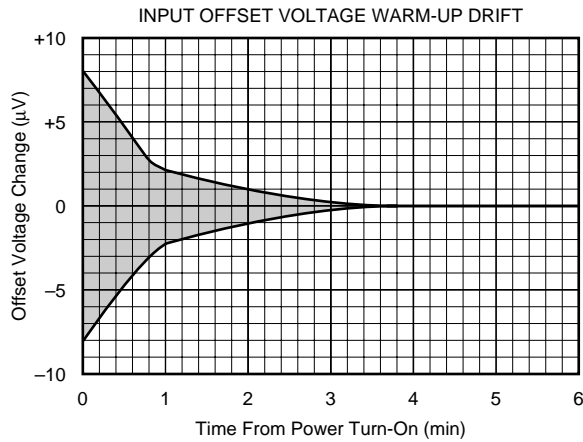
At  $V_{CC} = \pm 15V$  and  $-40^{\circ}C \leq T_A \leq +85^{\circ}C$ , unless otherwise noted.

PARAMETER	CONDITIONS	OPA27 OPA37			UNITS
		MIN	TYP	MAX	
<b>INPUT VOLTAGE</b> <sup>(1)</sup> Input Offset Voltage Average Drift <sup>(2)</sup> Supply Rejection	$T_{A\ MIN}$ to $T_{A\ MAX}$ $\pm V_{CC} = 4.5$ to $18V$ $\pm V_{CC} = 4.5$ to $18V$		$\pm 48$ $\pm 0.4$	$\pm 220^{(3)}$ $\pm 1.8^{(3)}$	$\mu V$ $\mu V/^{\circ}C$ dB
<b>BIAS CURRENT</b> Input Bias Current			$\pm 21$	$\pm 150^{(3)}$	nA
<b>OFFSET CURRENT</b> Input Offset Current			20	$135^{(3)}$	nA
<b>VOLTAGE RANGE</b> Common-Mode Input Range Common-Mode Rejection	$V_{IN} = \pm 11VDC$	$\pm 10.5^{(3)}$ $96^{(3)}$	$\pm 11.8$ 122		V dB
<b>OPEN-LOOP GAIN, DC</b> Open-Loop Voltage Gain	$R_L \geq 2k\Omega$	$113^{(3)}$	120		dB
<b>RATED OUTPUT</b> Voltage Output Short Circuit Current	$R_L = 2k\Omega$ $V_O = 0VDC$	$\pm 11.0^{(3)}$	$\pm 13.4$ 25		V mA
<b>TEMPERATURE RANGE</b> Specification		-40		+85	$^{\circ}C$

NOTES: (1) Offset voltage specification are measured with automatic test equipment after approximately 0.5s from power turn-on. (2) Unnulled or nulled with 8k $\Omega$  to 20k $\Omega$  potentiometer. (3) This parameter specified by design.

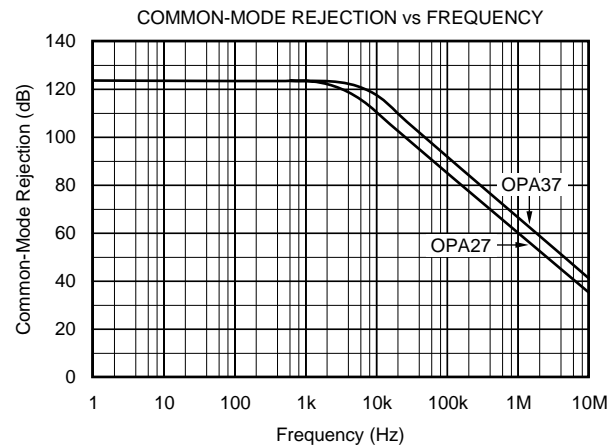
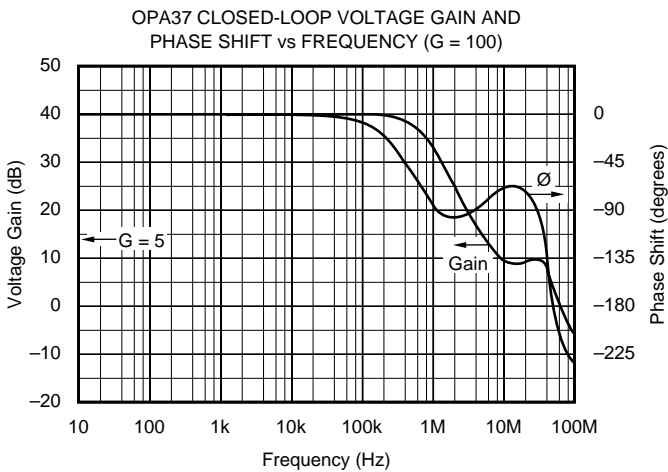
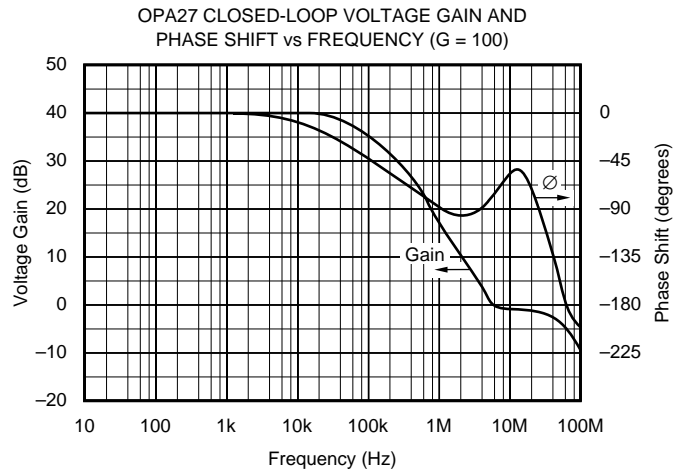
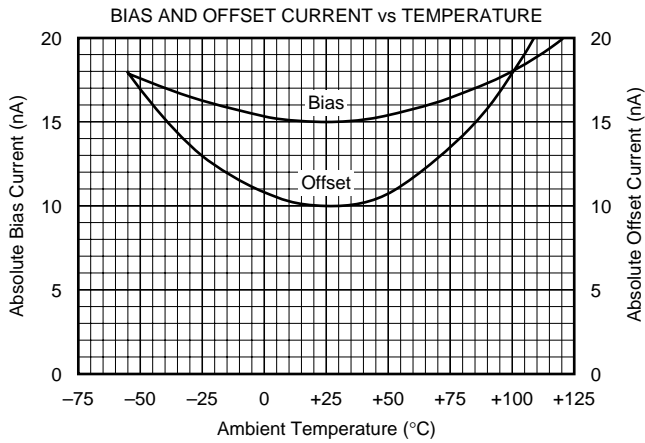
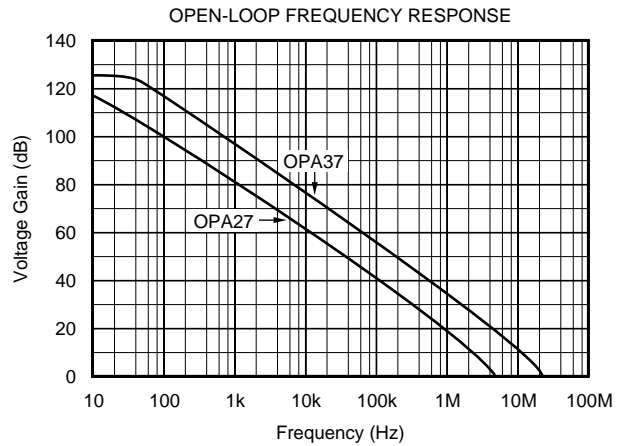
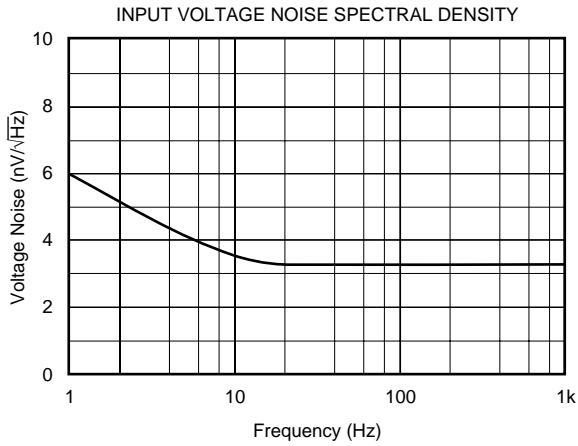
# TYPICAL CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$ ,  $\pm V_{CC} = \pm 15\text{VDC}$ , unless otherwise noted.



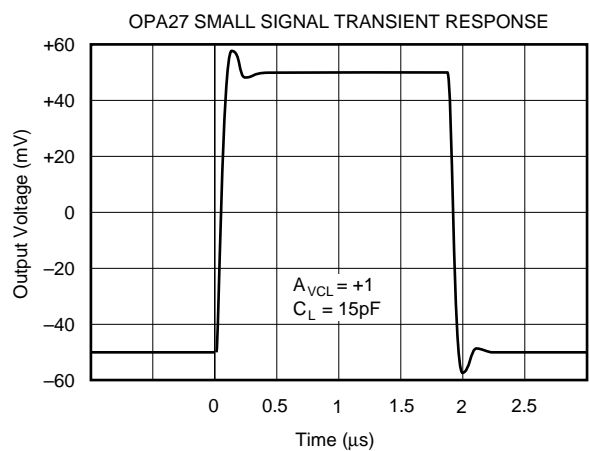
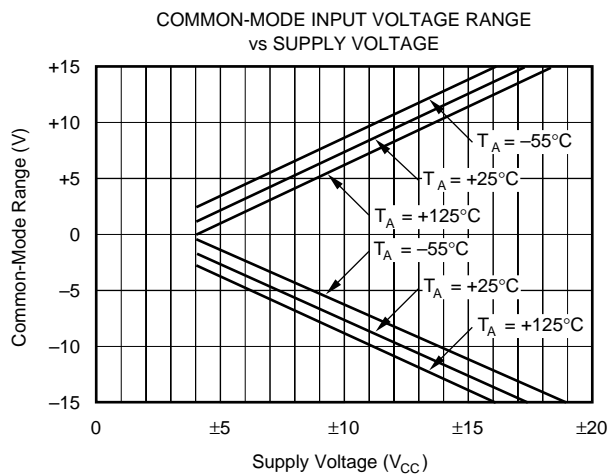
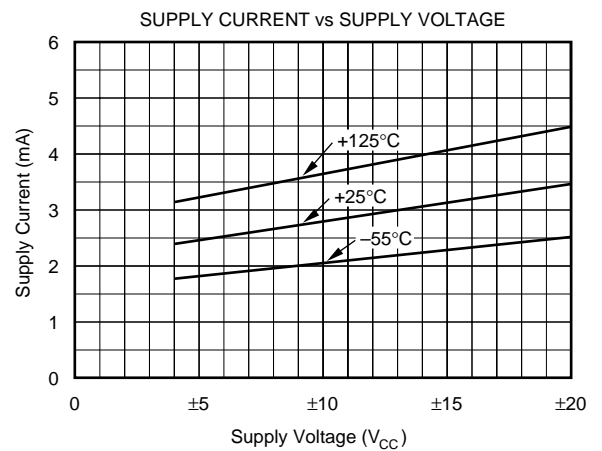
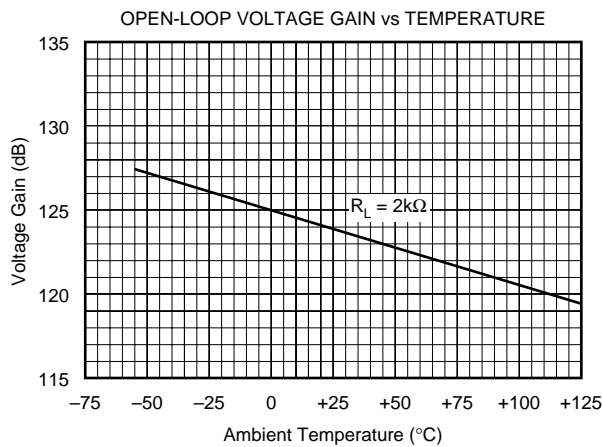
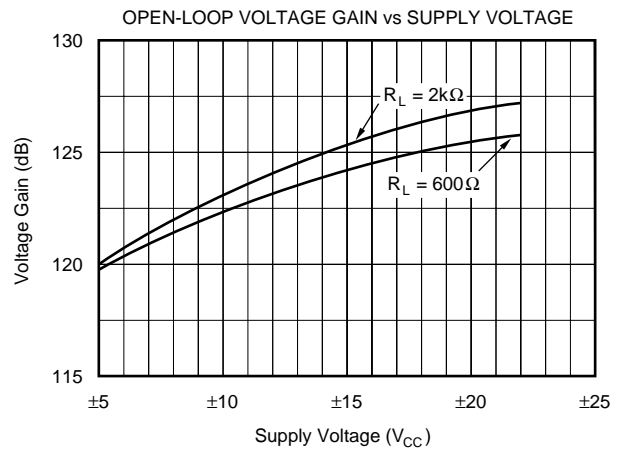
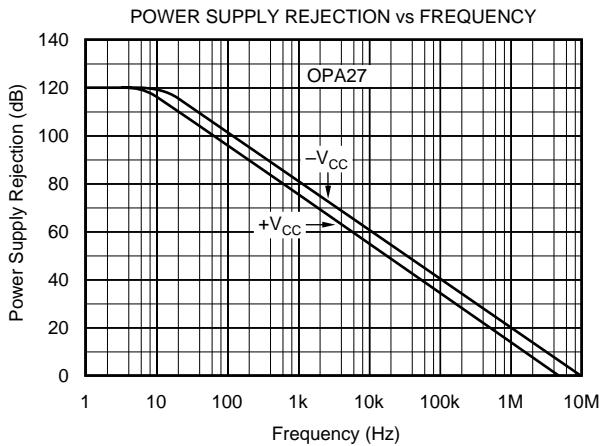
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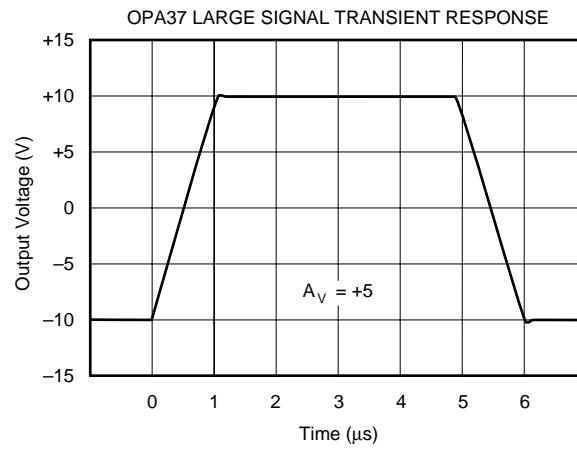
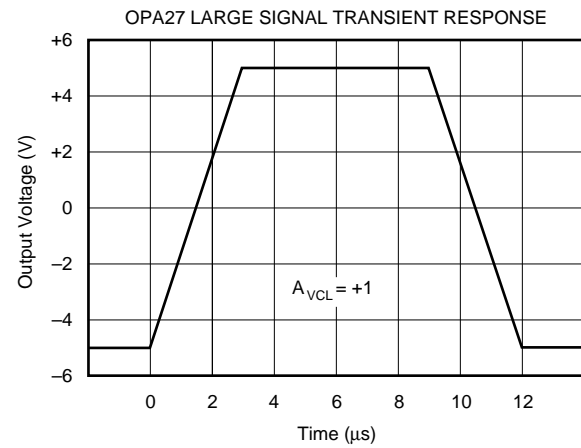
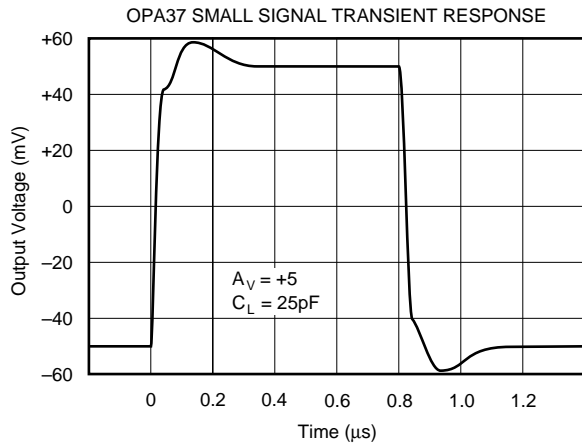
# TYPICAL CHARACTERISTICS (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $\pm V_{CC} = \pm 15\text{VDC}$ , unless otherwise noted.



# TYPICAL PERFORMANCE CURVES (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $\pm V_{CC} = \pm 15\text{VDC}$ , unless otherwise noted.





# APPLICATIONS INFORMATION

## OFFSET VOLTAGE ADJUSTMENT

The OPA27 and OPA37 offset voltages are laser-trimmed and require no further trim for most applications. Offset voltage drift will not be degraded when the input offset is nulled with a 10kΩ trim potentiometer. Other potentiometer values from 1kΩ to 1MΩ can be used, but  $V_{OS}$  drift will be degraded by an additional 0.1μV/°C to 0.2μV/°C. Nulling large system offsets by use of the offset trim adjust will degrade drift performance by approximately 3.3μV/°C per millivolt of offset. Large system offsets can be nulled without drift degradation by input summing.

The conventional offset voltage trim circuit is shown in Figure 3. For trimming very small offsets, the higher resolution circuit shown in Figure 4 is recommended.

The OPA27 and OPA37 can replace 741-type operational amplifiers by removing or modifying the trim circuit.

## THERMOELECTRIC POTENTIALS

The OPA27 and OPA37 are laser-trimmed to microvolt-level input offset voltages, and for very-low input offset voltage drift.

Careful layout and circuit design techniques are necessary to prevent offset and drift errors from external thermoelectric potentials. Dissimilar metal junctions can generate small EMFs if care is not taken to eliminate either their sources (lead-to-PC, wiring, etc.) or their temperature difference (see Figure 11).

Short, direct mounting of the OPA27 and OPA37 with close spacing of the input pins is highly recommended. Poor layout can result in circuit drifts and offsets which are an order of magnitude greater than the operational amplifier alone.

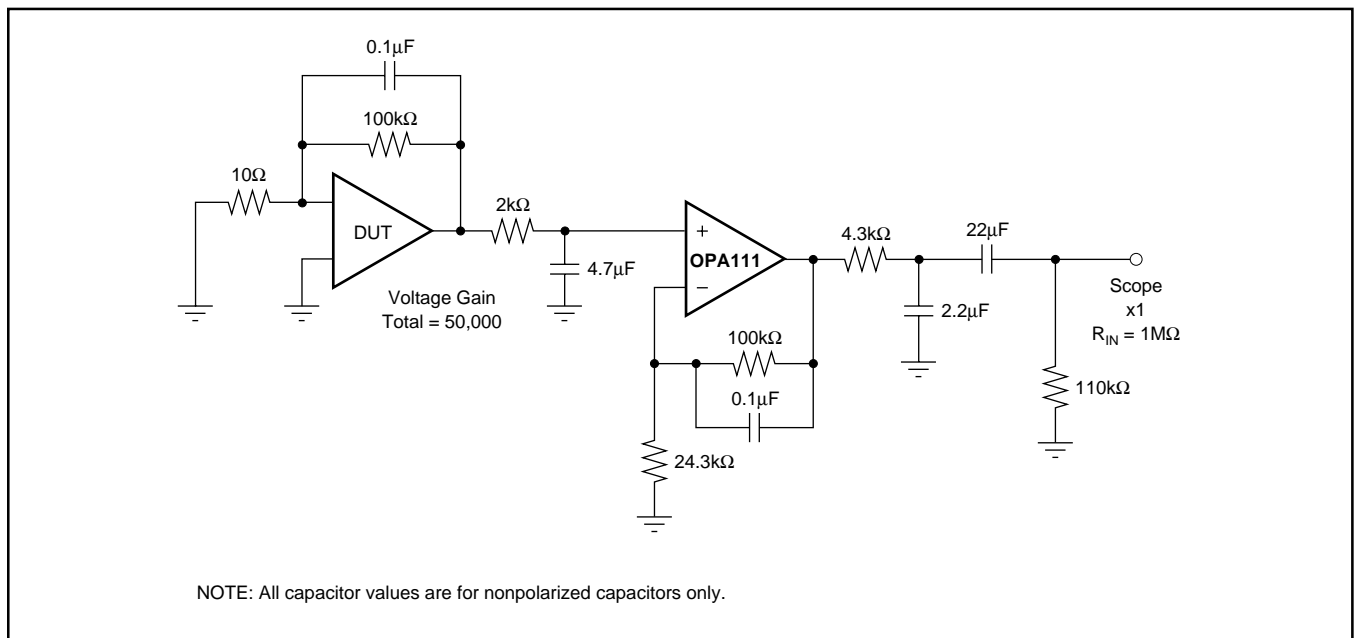


FIGURE 1. 0.1Hz to 10Hz Noise Test Circuit.

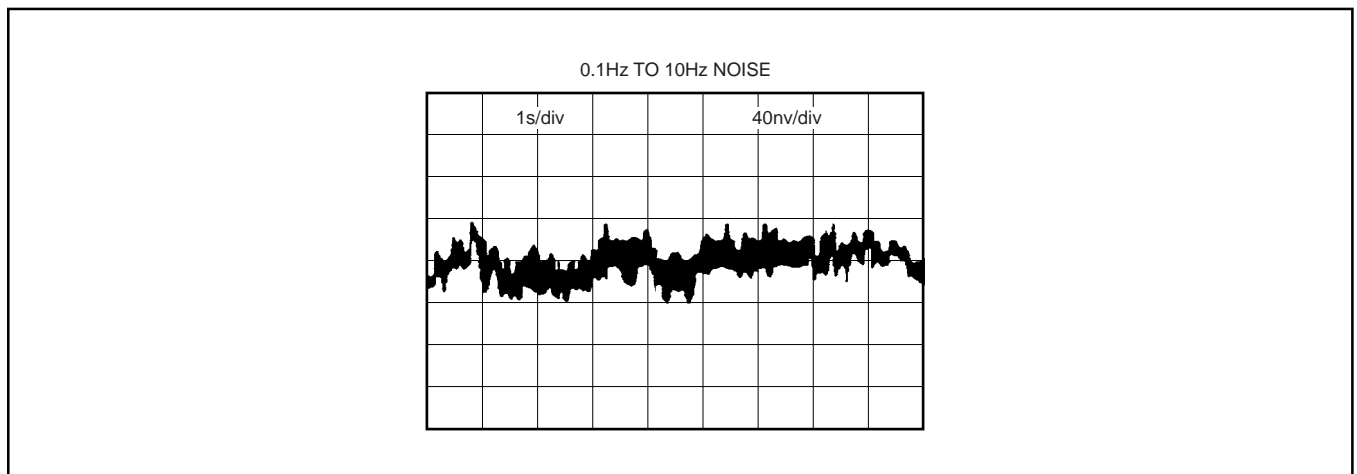


FIGURE 2. Low Frequency Noise.

## NOISE: BIPOLAR VERSUS FET

Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases, so consider the effect of source resistance on overall operational amplifier noise performance. At low source impedances, the lower voltage noise of a bipolar operational amplifier is superior, but at higher impedances the high current noise of a bipolar amplifier becomes a serious liability. Above about 15kΩ, the OPA111 low-noise FET operational amplifier is recommended for lower total noise than the OPA27, as shown in Figure 5.

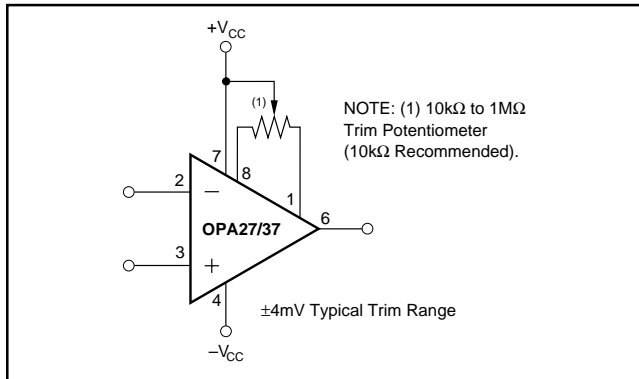


FIGURE 3. Offset Voltage Trim.

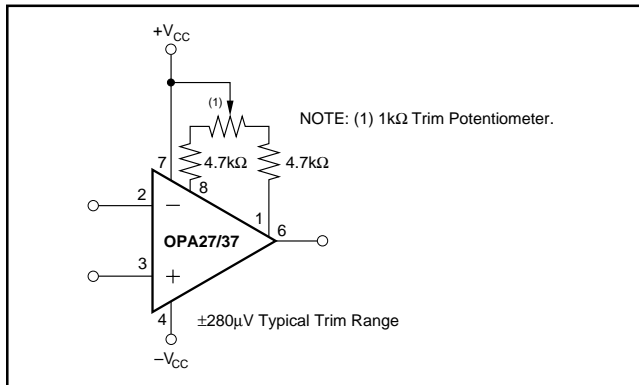


FIGURE 4. High Resolution Offset Voltage Trim.

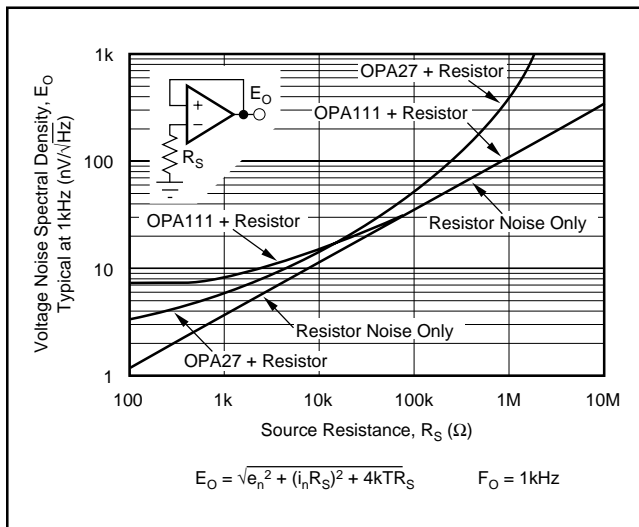


FIGURE 5. Voltage Noise Spectral Density Versus Source Resistance.

## COMPENSATION

Although internally compensated for unity-gain stability, the OPA27 may require a small capacitor in parallel with a feedback resistor ( $R_F$ ) which is greater than 2kΩ. This capacitor will compensate the pole generated by  $R_F$  and  $C_{IN}$  and eliminate peaking or oscillation.

## INPUT PROTECTION

Back-to-back diodes are used for input protection on the OPA27 and OPA37. Exceeding a few hundred millivolts differential input signal will cause current to flow, and without external current limiting resistors, the input will be destroyed.

Accidental static discharge, as well as high current, can damage the amplifier's input circuit. Although the unit may still be functional, important parameters such as input offset voltage, drift, and noise may be permanently damaged, as will any precision operational amplifier subjected to this abuse.

Transient conditions can cause feedthrough due to the amplifier's finite slew rate. When using the OPA27 as a unity-gain buffer (follower) a feedback resistor of 1kΩ is recommended, as shown in Figure 6.

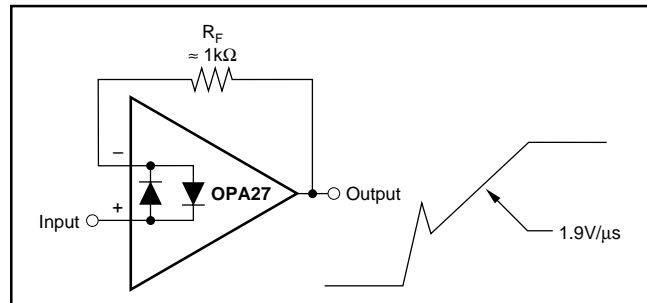


FIGURE 6. Pulsed Operation.

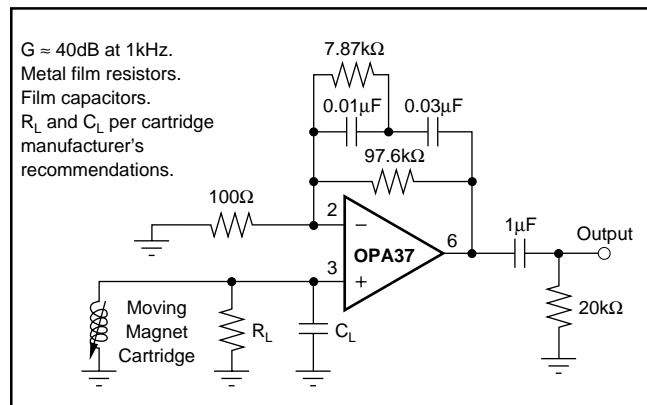


FIGURE 7. Low-Noise RIAA Preamplifier.

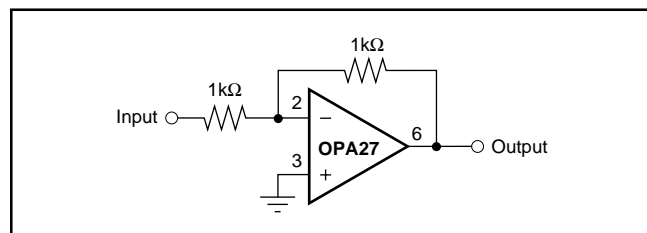


FIGURE 8. Unity-Gain Inverting Amplifier.

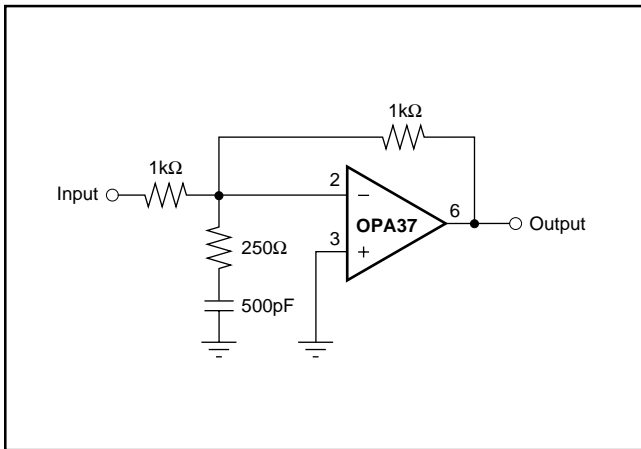


FIGURE 9. High Slew Rate Unity-Gain Inverting Amplifier.

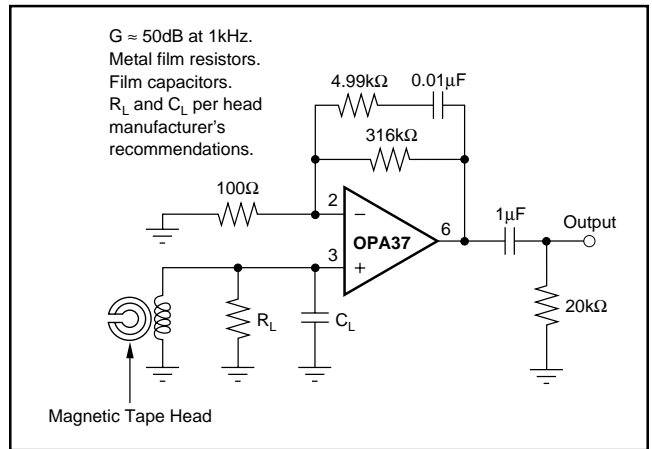


FIGURE 10. NAB Tape Head Preamplifier.

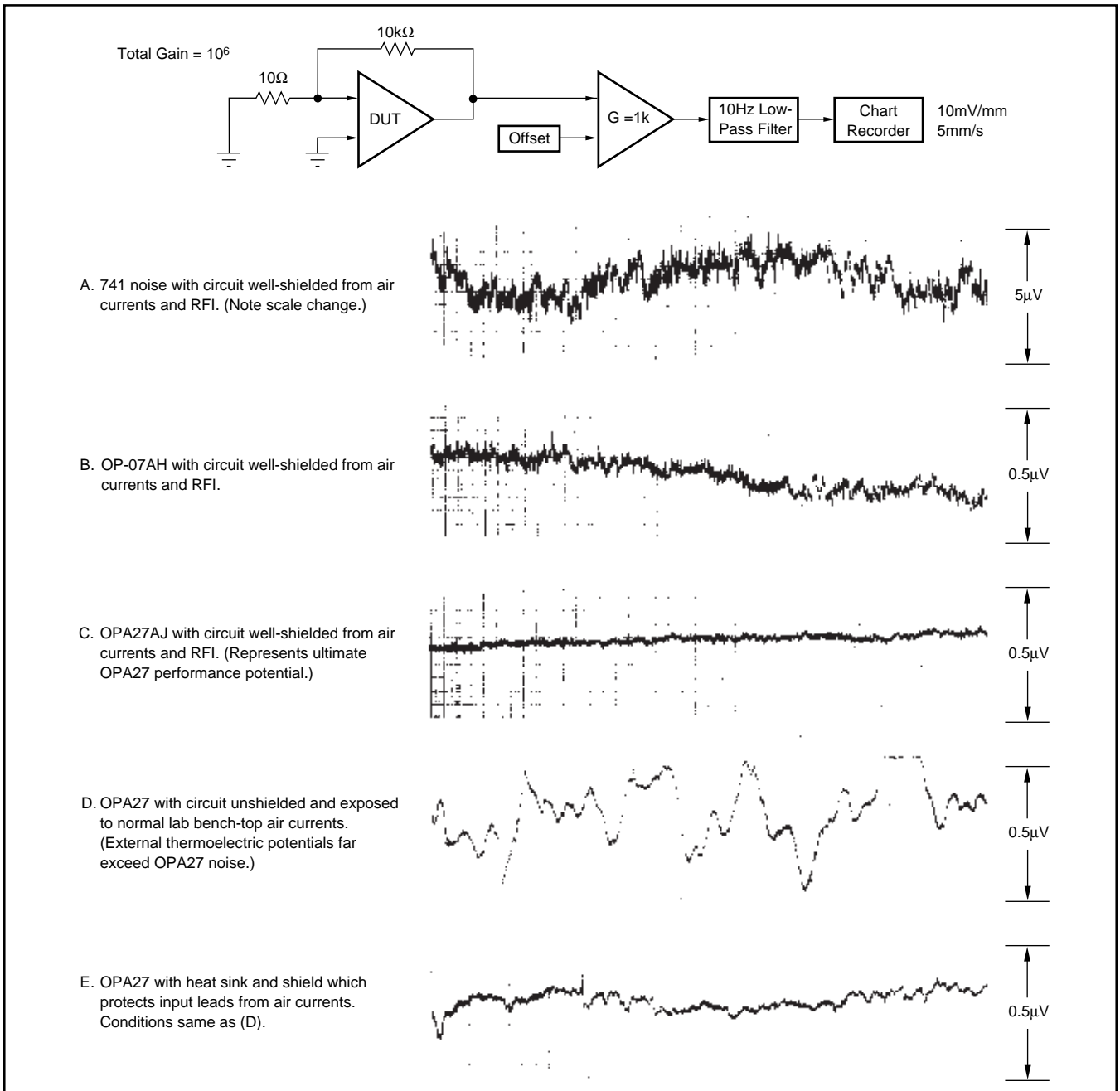


FIGURE 11. Low Frequency Noise Comparison.

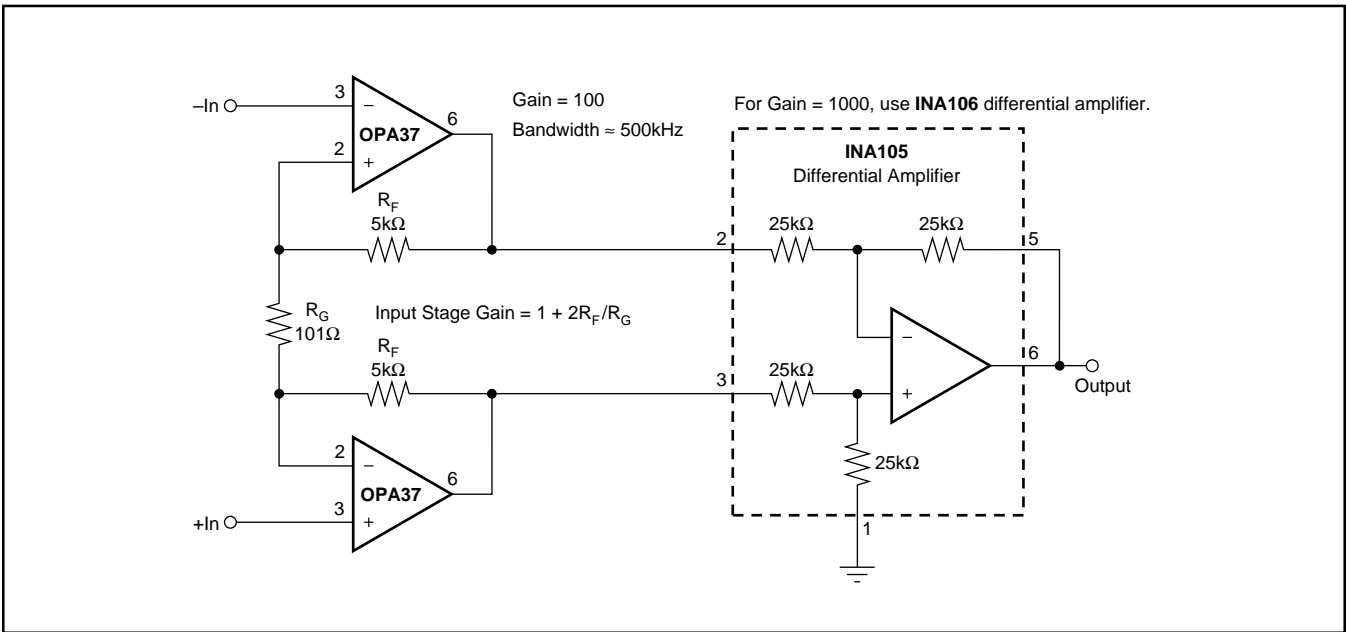


FIGURE 12. Low Noise Instrumentation Amplifier.

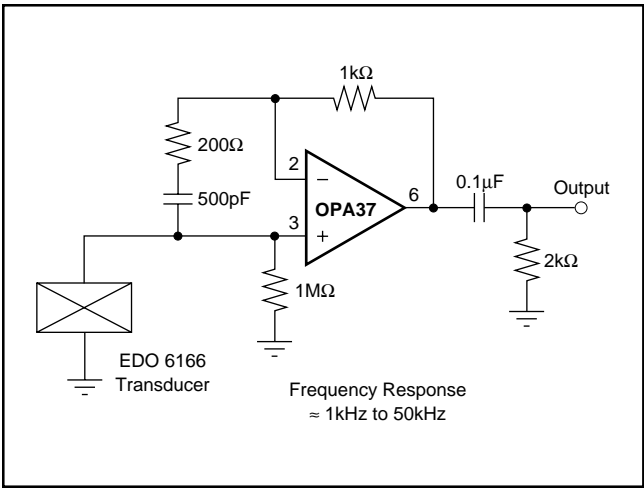


FIGURE 13. Hydrophone Preamplifier.

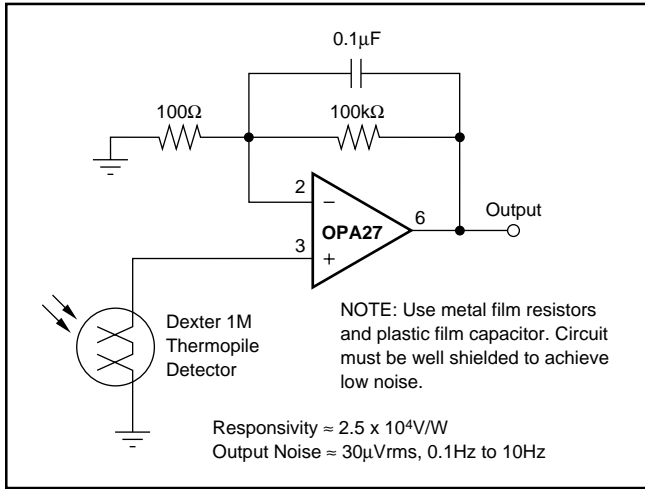


FIGURE 14. Long-Wavelength Infrared Detector Amplifier.

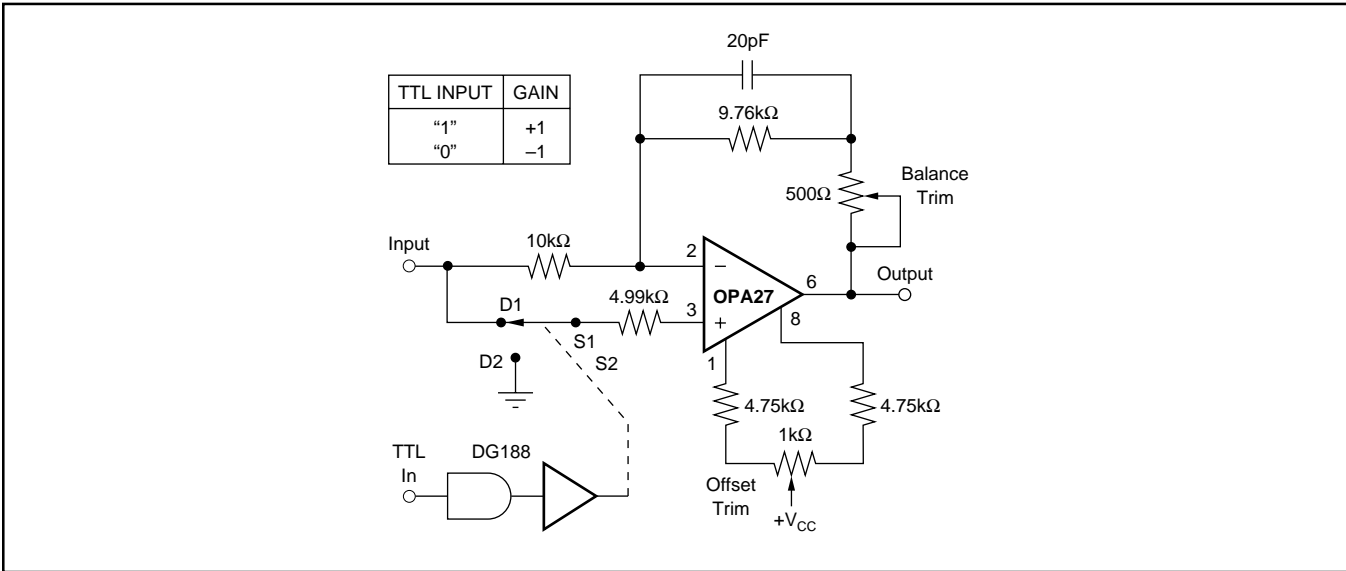


FIGURE 15. High Performance Synchronous Demodulator.

Gain =  $-1010\text{V/V}$   
 $V_{OS} \approx 2\mu\text{V}$   
 Drift  $\approx 0.07\mu\text{V}/^\circ\text{C}$   
 $e_n \approx 1\text{nV}/\sqrt{\text{Hz}}$  at 10Hz  
            $0.9\text{nV}/\sqrt{\text{Hz}}$  at 100Hz  
            $0.87\text{nV}/\sqrt{\text{Hz}}$  at 1kHz  
 Full Power Bandwidth  $\approx 180\text{kHz}$   
 Gain Bandwidth  $\approx 500\text{MHz}$   
 Equivalent Noise Resistance  $\approx 50\Omega$

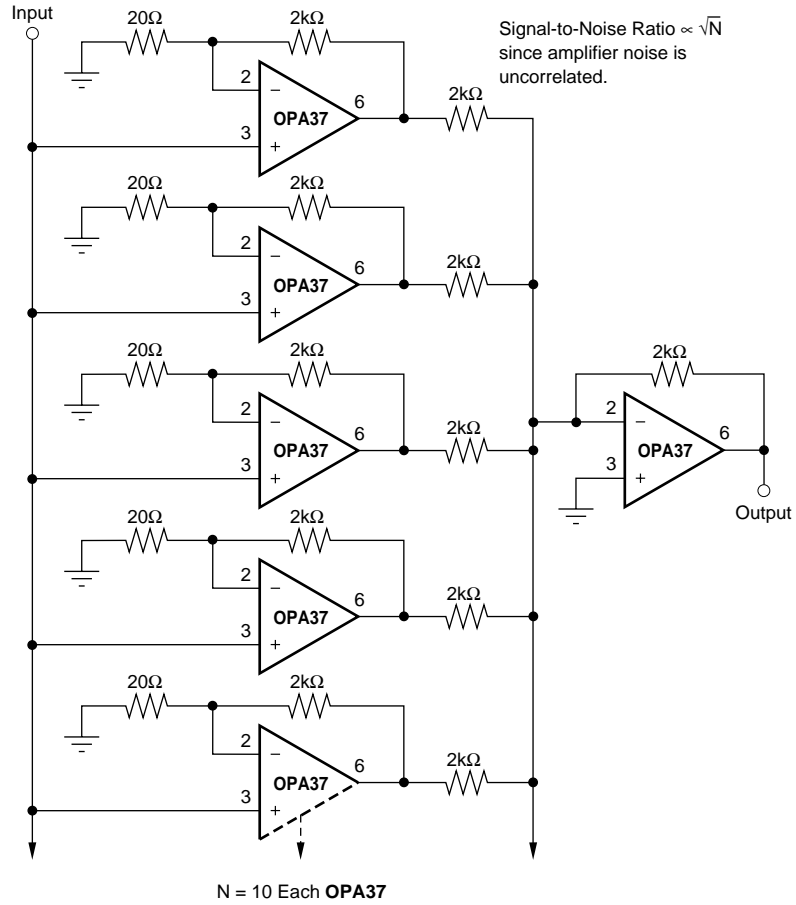


FIGURE 16. Ultra-Low Noise “N”-Stage Parallel Amplifier.

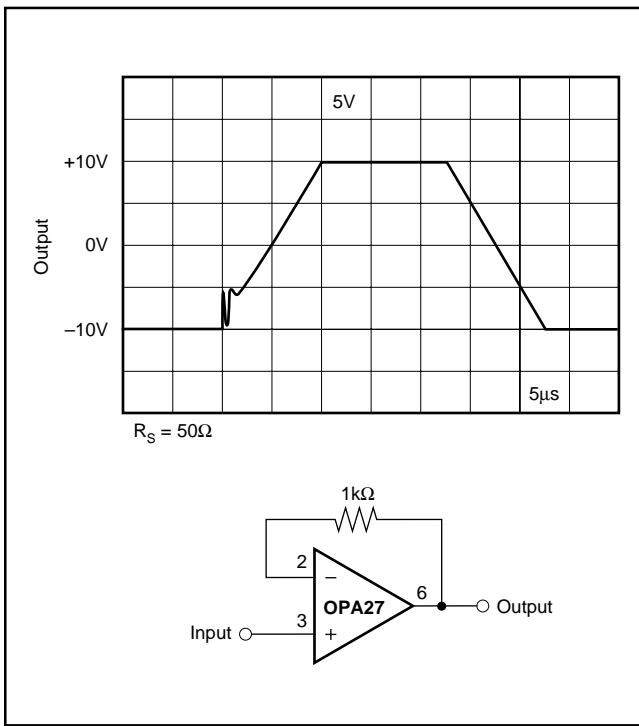


FIGURE 17. Unity-Gain Buffer.

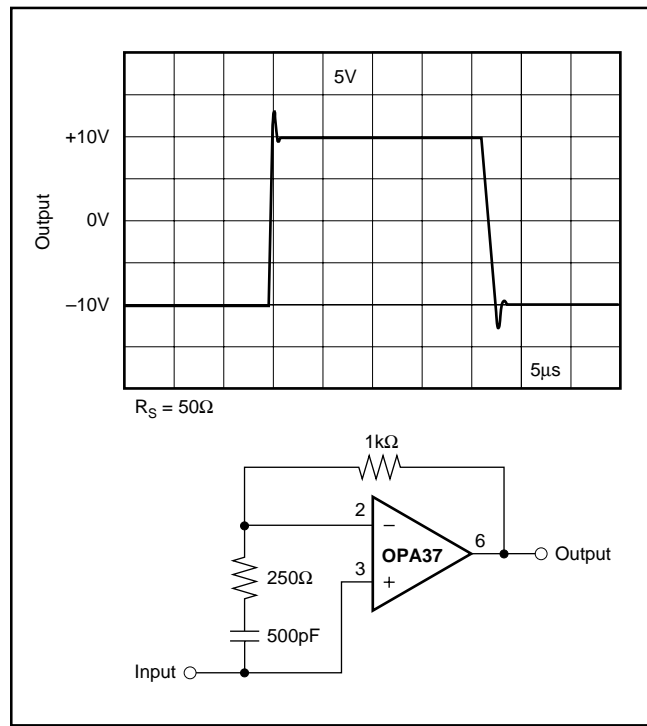


FIGURE 18. High Slew Rate Unity-Gain Buffer.

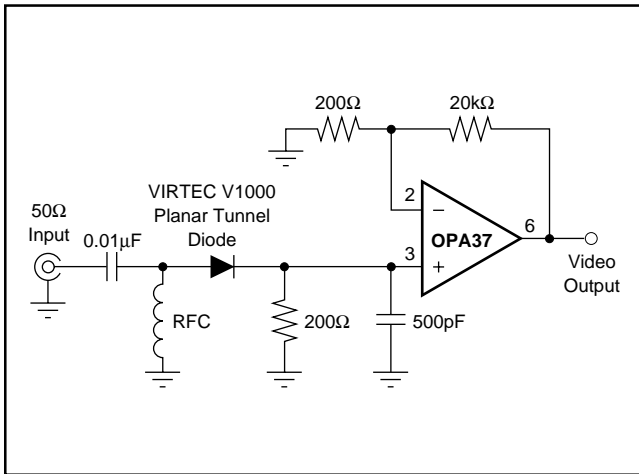


FIGURE 19. RF Detector and Video Amplifier.

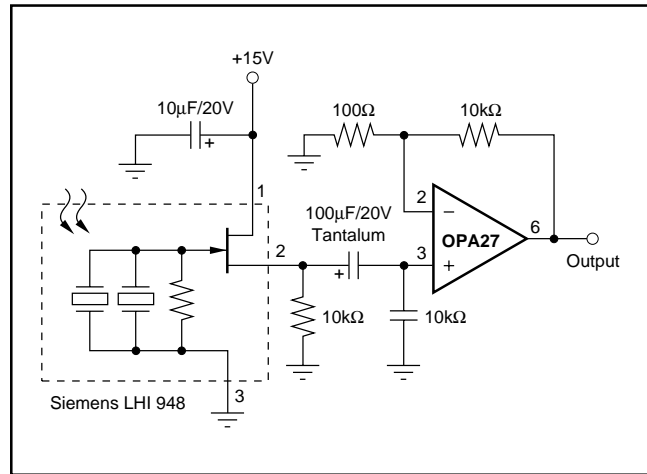


FIGURE 20. Balanced Pyroelectric Infrared Detector.

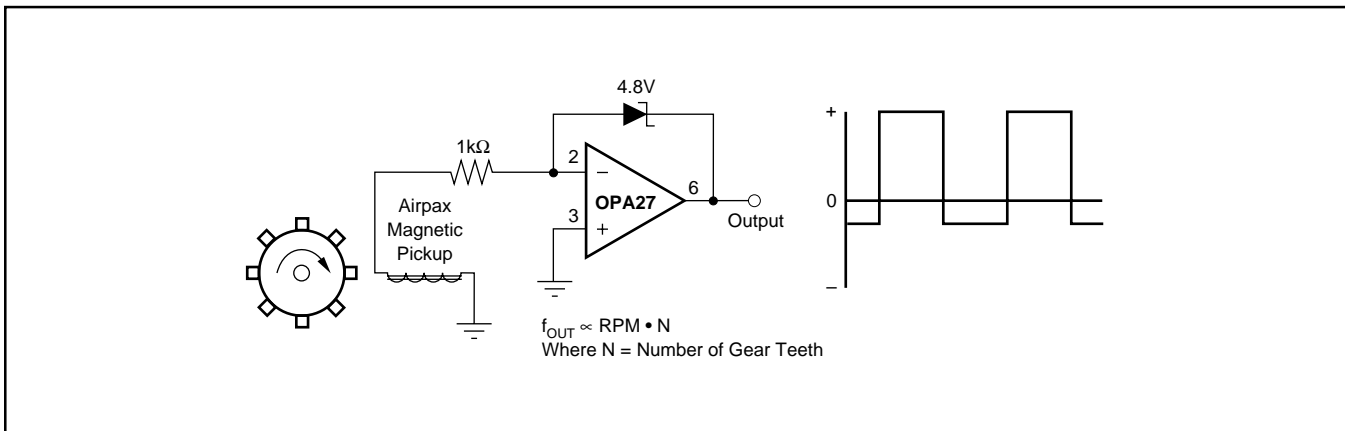


FIGURE 21. Magnetic Tachometer.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA27GP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	OPA27GP	<a href="#">Samples</a>
OPA27GPG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	OPA27GP	<a href="#">Samples</a>
OPA27GU	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA 27U	<a href="#">Samples</a>
OPA27GU/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA 27U	<a href="#">Samples</a>
OPA27GU/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA 27U	<a href="#">Samples</a>
OPA27GUE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA 27U	<a href="#">Samples</a>
OPA27GUG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA 27U	<a href="#">Samples</a>
OPA37GP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	OPA37GP	<a href="#">Samples</a>
OPA37GPG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	OPA37GP	<a href="#">Samples</a>
OPA37GU	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA 37U	<a href="#">Samples</a>
OPA37GU/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA 37U	<a href="#">Samples</a>
OPA37GUE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA 37U	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA27GU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA37GU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA27GU/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA37GU/2K5	SOIC	D	8	2500	367.0	367.0	35.0

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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