GENERAL DESCRIPTION

OB6563 is an active transition-mode (TM) power factor correction (PFC) controller for AC-DC switching mode power supply applications.

OB6563 features an internal start-up timer for stand-alone applications, a one quadrant multiplier with THD optimizer for near unity power factor, zero current detector (ZCD) to ensure TM operation, a current sensing comparator with built-in leading-edge blanking, and a totem pole output ideally suited for driving a power MOSFET.

OB6563 offers great protection coverage including system over-voltage protection (OVP) to eliminate runaway output voltage due to load removal, VCC under voltage lockout (UVLO), cycle-by-cycle current limiting, multiplier output clamping that limit maximum peak switch current, and gate drive output clamping for external power MOSFET protection.

With added system open loop protection feature, OB6563 shuts down system when the feedback loop is open.

In OB6563, the dynamic OVP sensing current is set to 10uA, which will decrease system standby power greatly. When used with On-Bright PWM controller OB2298 or Quasi-Resonant controller OB2203 in a 150W AC/DC power design, it can deliver <0.4W standby power at universal AC range input.

OB6563 is offered in SOP-8 and DIP-8 packages.
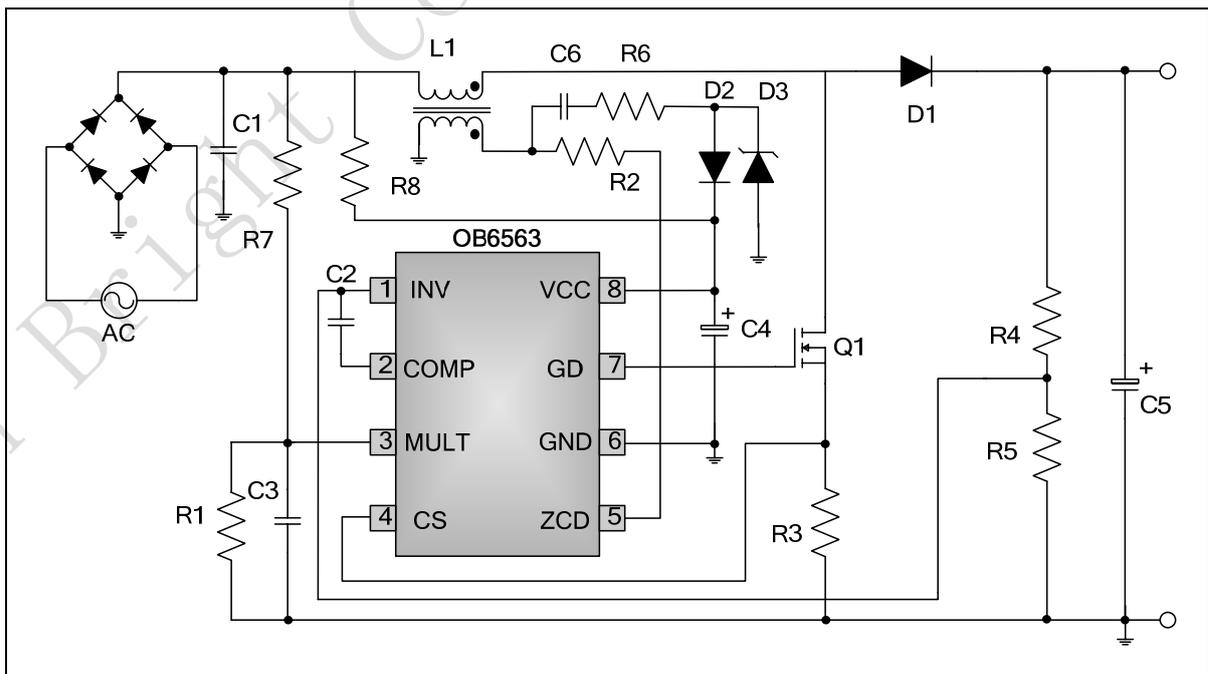
FEATURES

- Transition Mode (TM) Operation
- One quadrant multiplier with THD optimizer
- Low Dynamic OVP Sensing Current Setting
- Low Start-up Current and Operating Current
- Cycle-by-Cycle Current Limiting
- Internal RC Filter
- Trimmed 1.5% Internal Bandgap Reference
- Under Voltage Lockout with Hysteresis
- Very Precise Adjustable Output Overvoltage Protection
- Internal Start-up Timer for Stand-alone Applications
- Disable Function
- Totem Pole Output with High State Clamping
- System Open Loop Protection
- Proprietary Audio Noise Free Operation
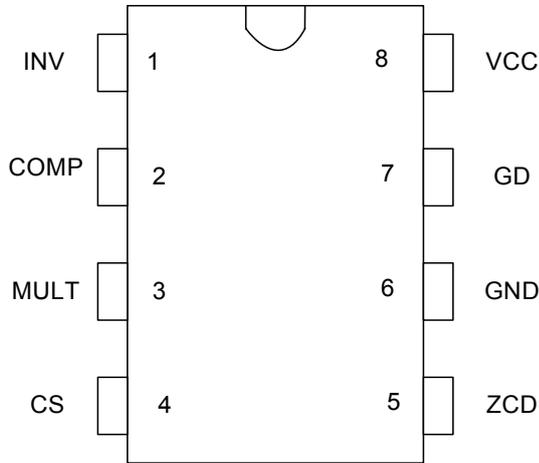- 9.5V to 28V wide range of VCC voltage

APPLICATIONS

- Electronic Ballast
- AC-DC SMPS

TYPICAL APPLICATION

GENERAL INFORMATION

Terminal Assignment
In SOP8 or DIP8 Package.

INV	1		8	VCC
COMP	2		7	GD
MULT	3		6	GND
CS	4		5	ZCD

Ordering Information

Part Number	Description
OB6563AP	8 Pin DIP, Pb free in Tube
OB6563CP	8 Pin SOP, Pb free in Tube
OB6563CPA	8 Pin SOP, Pb free in T&R

Package Dissipation Rating

Package	RθJA (℃/W)
DIP8	90
SOP8	150

Absolute Maximum Ratings

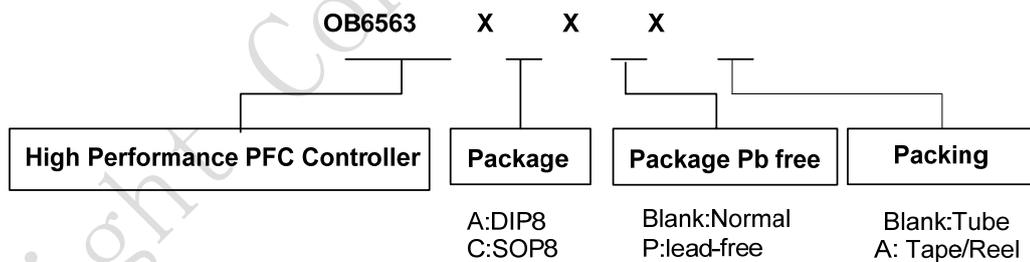| Symbol	Parameter	Value
VCC	DC Supply voltage	30 V
I_ZCD	Zero Current Detector Max. Current	50mA(source) -10mA(sink)
CS INV COMP MULT	Analog inputs & outputs	-0.3 to 7V
Tj	Maximum Operating Junction Temperature	150 ℃
Tstg	Min/Max Storage Temperature	-55 to 150 ℃
Lead Temperature	(Soldering, 10secs)	260 ℃

Note: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

OB6563   X   X   X

High Performance PFC Controller	Package	Package Pb free	Packing
	A:DIP8 C:SOP8	Blank:Normal P:lead-free	Blank:Tube A: Tape/Reel

Marking Information

LT YWW
OB6563CP

Y: Year Code(0-9)
WW: Week Code(01-52)
C: SOP8 Package
P: Pb-free Package
S: Internal Code(Optional)

LT YWW
OB6563AP

Y: Year Code(0-9)
WW: Week Code(01-52)
A: DIP8 Package
P: Pb-free Package
S: Internal Code(Optional)

TERMINAL DESCRIPTIONS

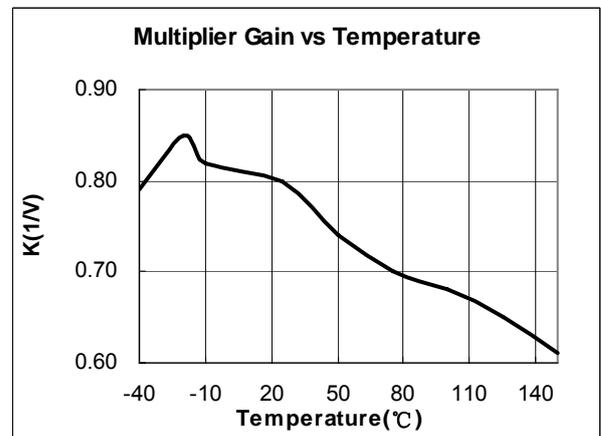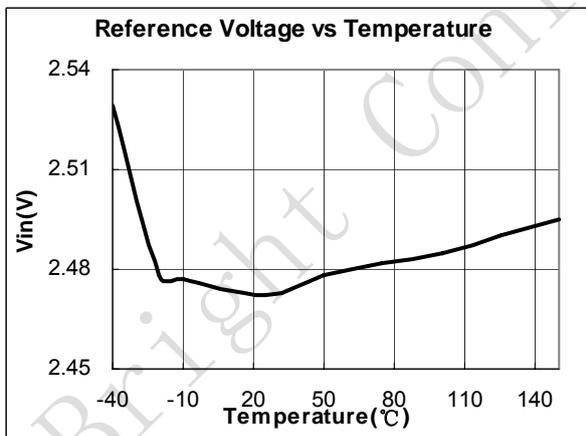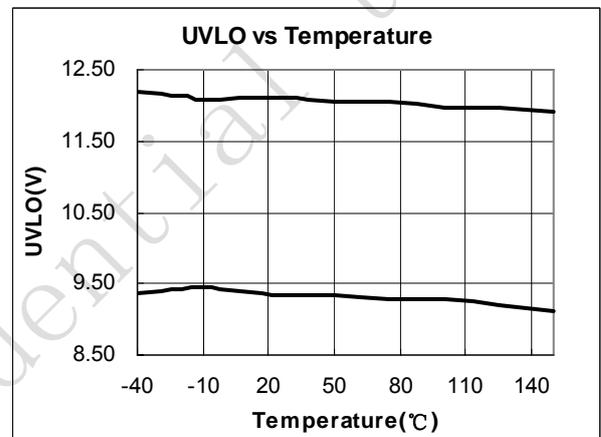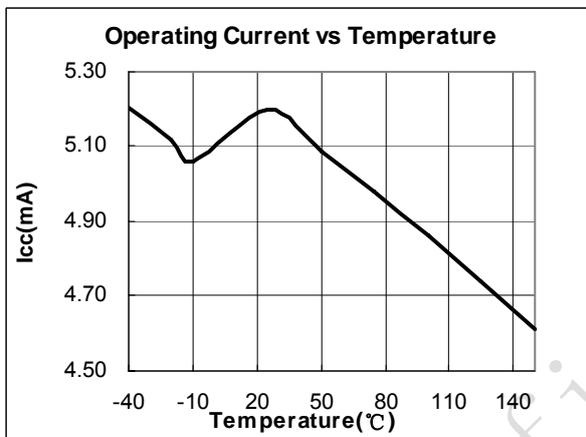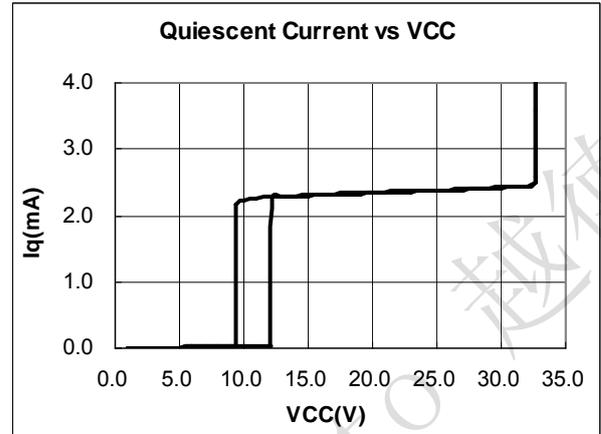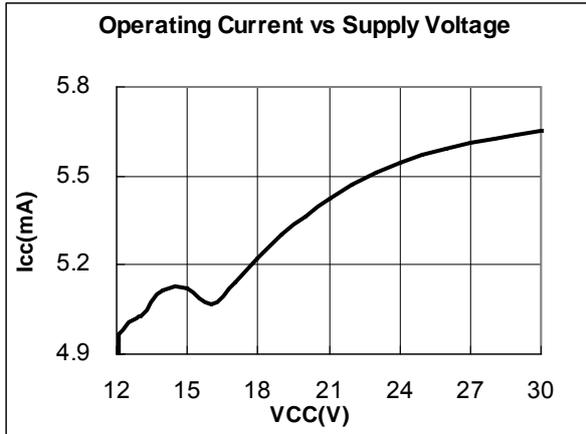| Pin Num	Pin Name	I/O	Description
1	INV	I	Inverting Input of Error Amplifier. Connected to Resistor Divider from System Output. This pin is also used for system open loop protection.
2	COMP	O	Output of Error Amplifier. A feedback compensation network is placed between COMP and the INV pin.
3	MULT	I	Input of Multiplier. Connected to Line Voltage after Bridge Diodes via A Resistor Divider to Provide Sinusoidal Reference Voltage to the Current Loop.
4	CS	I	Current Sense Input Pin. Connected to MOSFET Current Sensing Node.
5	ZCD	I	Zero Current Detection Input. When Activated, A New Switching Cycle Starts. If it is connected to GND, the device is disabled.
6	GND	P	Ground Pin
7	GD	O	Gate driver output. Drive Power MOSFET.
8	VCC	P	DC Supply Voltage.

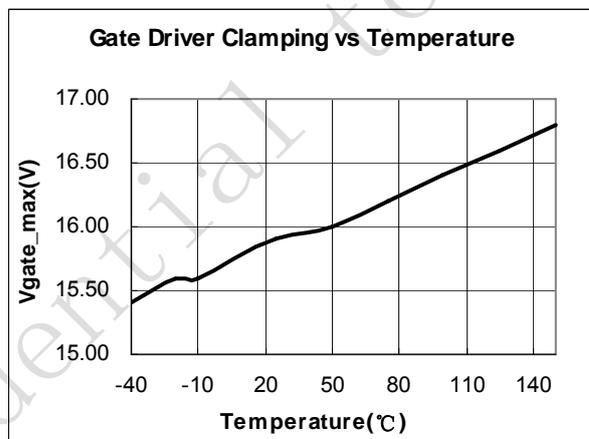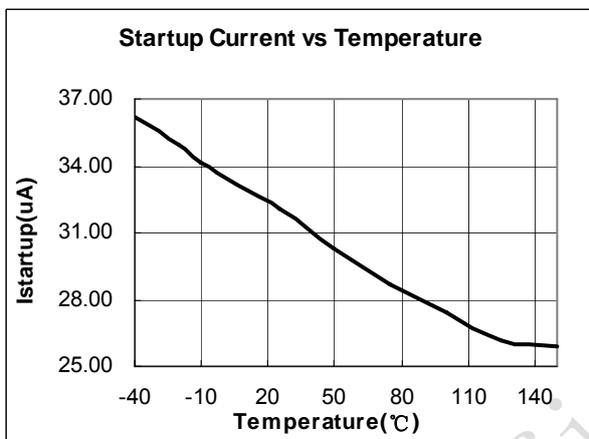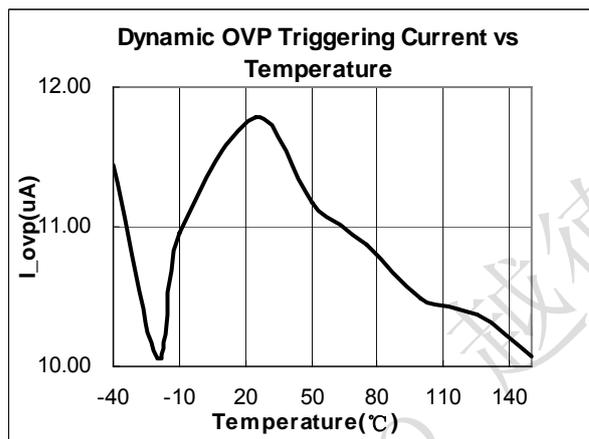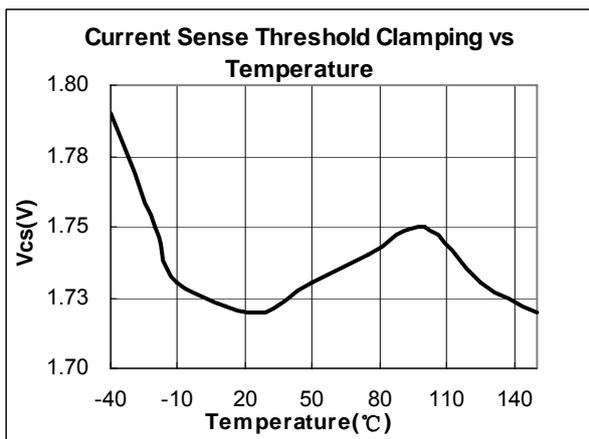## BLOCK DIAGRAM
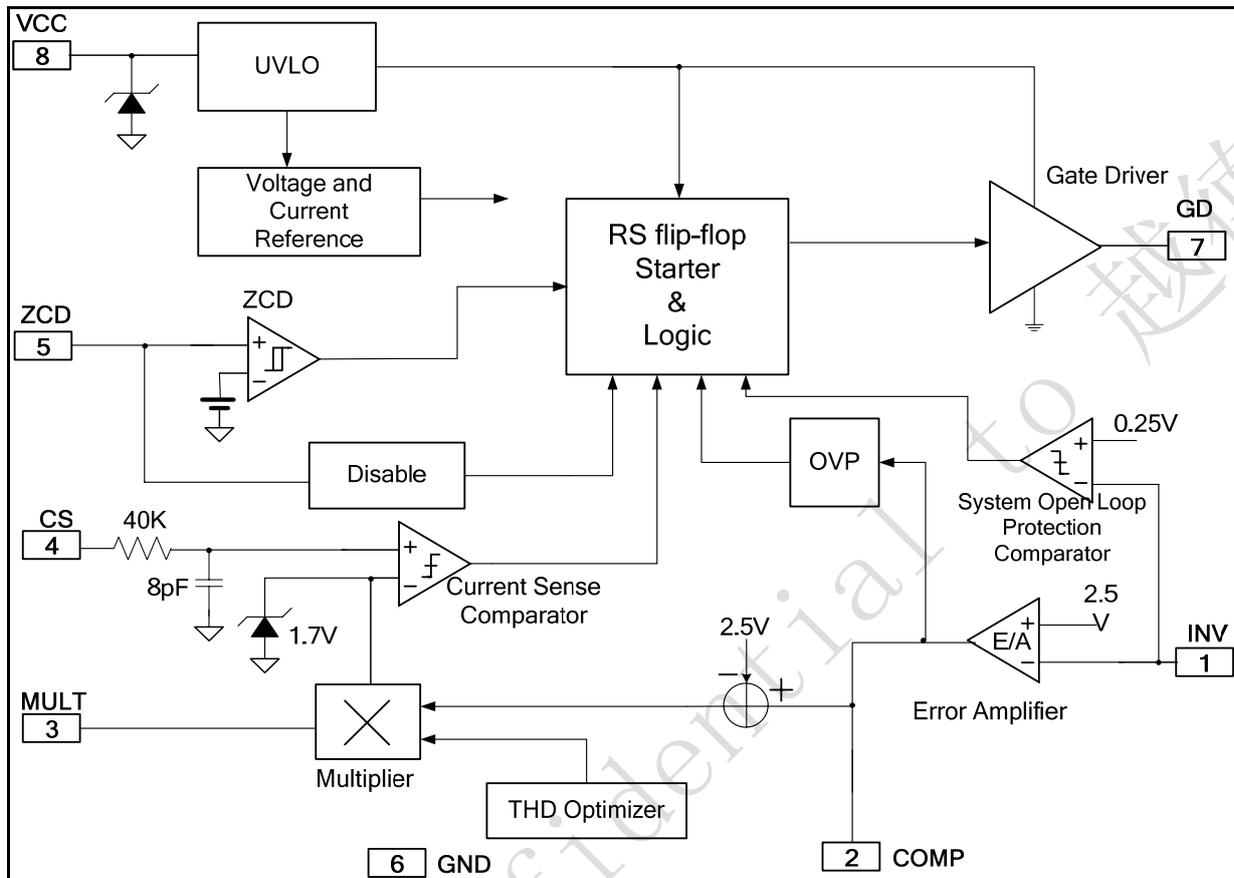
ELECTRICAL CHARACTERISTICS

(T_A = 25℃ if not otherwise noted)

Symbol	Pin	Parameter	Test Conditions	Min	Typ	Max	Unit
SUPPLY VOLTAGE SECTION							
Vcc	8	Operating Range	After Turn On	11		28	V
UVLO	8	Turn-on Threshold		11	12	13	V
	8	Turn-off Threshold		8.5	9.5	10.5	V
Hys	8	Hysteresis			2.5		V
Vz	8	Zener Voltage	Icc=5mA	30	33	36	V
SUPPLY CURRENT SECTION							
Icc-start	8	Start-up Current	Vcc=11V		35	70	uA
Iq	8	Quiescent Current, No Switching	Vcc=14.5V		2.9	4	mA
Icc	8	Operating Supply Current	CL=1nf @ 70kHz		4	5.5	mA
			In OVP condition Vpin1=2.7V		1.4	3	mA
Iq	8	Quiescent Current	Vpin5≤150mV Vcc=14.5V		1.1	3	mA
			Vpin5≤150mV, Vcc<Vcc off		35	70	uA
ERROR AMPLIFIER SECTION							
Vinv	1	Voltage Feedback Input Threshold	V_{cc}=14.5V	2.45	2.5	2.55	V
Vinv	1	Line Regulation	12V<Vcc<28V		2	5	mV
Iinv	1	Input Bias Current	I_{DD} = 10 mA		-0.1	-1	uA
Gv		Voltage Gain	Open Loop	60	80		dB
Gb		Gain Bandwidth			1.2		MHz
Icomp	2	Source Current	Vcomp=3.6V, Vinv=2.4V	-1	-3	-5	mA
		Sink Current	Vcomp=3.6V, Vinv=2.6V	1	3	5	mA
Vcomp	2	Upper Clamp Voltage	Isource=0.5mA		4.9		V
		Lower Clamp Voltage	Isink=0.2mA		2.25		V
MULTIPLIER SECTION							
Vmult	3	Linear Operating Range	Vcomp=3.0V	0 to 3.5			V
ΔVcs/ ΔVmult		Output Max. Slope	Vmult=from 0 to 0.5v Vcomp=Upper Clamp Voltage	1.65	1.9		V/V
K		Gain	Vmult=1V, Vcomp=3.5V		0.65		1/V
CURRENT SENSE COMPARATOR							
Vcs	4	Current Sense Reference Clamp	Vmult=2.5V Vcomp=Upper Clamp Voltage	1.55	1.7	1.85	V
Ics	4	Input Bias Current	Vcs=0			0.1	uA
Td(H-L)	4	Delay to Output			200	450	ns
ZERO CURRENT DETECTOR							
Vzcd	5	Input Threshold Voltage Rising Edge			1.9		V
		Hysteresis		0.3	0.5	0.7	V
Vzcd	5	Upper Clamp Voltage	Izcd=2mA	5.4	6	6.6	V
Vzcd	5	Lower Clamp Voltage	Izcd=-2mA	0.4	0.65	0.8	V
Izcd	5	Input Bias Current	1V≤Vzcd≤4.5V		2		uA

Izcd	5	Source Current Capability			-3		mA
Izcd	5	Sink Current Capability		3		10	mA
Vdis	5	Disable Threshold		150	250	350	mV
Izcd	5	Restart Current After Disable	Vzcd<Vdis Vcc>Vccoff	-100	-200	-400	uA
GATE DRIVE SECTION							
VoL	7	Low Output Voltage	Vcc=14.5V, Io=100mA			1.5	V
VoH	7	High Output Voltage	Vcc=14.5V, Io=100mA	8			V
Tr	7	Rising Time	Cl=1000pF, 10~90%		80	150	ns
Tf	7	Falling Time	Cl=1000pF, 10~90%		30	70	ns
Voclamp	7	Output ClampVoltage	Vcc=28V		16	18	V
OUTPUT OVER VOLTAGE SECTION							
Iovp	2	Dynamic OVP Triggering Current		8	10	12	uA
		Static OVP Threshold	2.1	2.25	2.4	V	
STARTUP TIMER							
Tstart		Re-Start Timer Period		70	150	300	us
SYSTEM OPEN LOOP PROTECTION COMPARATOR							
Vth_ol		System Open Loop Protection Comparator Threshold			250		mV

TYPICAL PERFOMANCE CHART

Operating Current vs Supply Voltage

Quiescent Current vs VCC

Operating Current vs Temperature

UVLO vs Temperature

Reference Voltage vs Temperature

Multiplier Gain vs Temperature

Current Sense Threshold Clamping vs Temperature

Dynamic OVP Triggering Current vs Temperature

Startup Current vs Temperature

Gate Driver Clamping vs Temperature

Restart Timer Period vs Temperature

Multiplier Characterization

OPERATIONAL DESCRIPTION

OB6563 is a highly integrated power factor correction (PFC) controller IC. The transition mode control greatly reduces the switch turn-on loss, improves the conversion efficiency and provides very good power factor correction.

- **Error Amplifier**

Connected to a resistor divider from output line, the inverting input of the Error Amplifier (E/A) is compared to an internal reference voltage(2.5V) to set the regulation on output voltage.

The E/A output is internally connected to the multiplier input and externally connected for loop compensation. It is usually realized with a capacitor which connected between the inverting input and EA output. The system loop bandwidth is set below 20 Hz to suppress the AC ripple of the line voltage.

- **Multiplier**

The one quadrant multiplier output limits the MOSFET peak current with respect of the system output voltage and the AC half wave rectified input voltage. Through controlling the CS comparator threshold as the AC line voltage traverses sinusoidally from zero to peak line voltage, the PFC preconverter's load appears to be resistive to the AC line.

In OB6563, the two inputs for the multiplier are designed to achieve good linearity over a wide dynamic range to represent an AC line free from distortion. Special efforts have been made to assure universal line applications with respect to a 90 to 264 VAC range.

The multiplier output is internally clamped to 1.7V. So the MOSFET is protected against critical operation during start up.

- **Output Overvoltage Protection**

Limited by low loop bandwidth setting, detection of output OVP could become very slow in regular approach.

OB6563 offers two level OVP protection including dynamic OVP for output fast transient protection and static OVP for output stead-state protection.

In an output transient OVP event, current in proportion to ΔV flows into Error Amplifier output COMP through compensation network. When this current reaches 8uA, the output of multiplier is forced to decrease and on-time of MOSFET is reduced. When current continues to exceed 10uA, the power MOSFET is turned off until the current falls below ~2.5uA. In this way, the system output cannot reach to a very high value.

When OVP event lasts long enough, the Error Amplifier Output, COMP, will saturate and stay low. Static OVP comparator is activated and power MOSFET Gate is off when COMP voltage is dropped below 2.25V. Normal operation is resumed when Error Amplifier goes back to its linear region after output voltage drops.

Overvoltage protection block
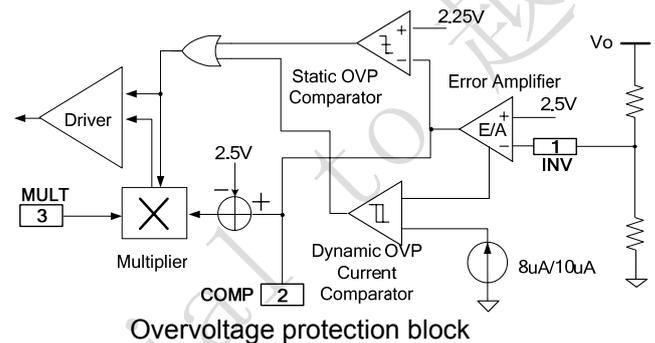
- **Startup Current and Start up Control**

The typical startup current of OB6563 is 35uA when the VCC pin is lower than the UVLO threshold so that VCC could be charged up and start up the device. A high value, low wattage startup resistor can therefore be used to minimize the power loss during the normal operation.

- **Current Sensing Comparator and Leading Edge Blanking**

Cycle-by-cycle current limiting is provided in OB6563's peak current mode control. The switch current is detected by a sense resistor into the sense pin. The multiplier output voltage is compared with this sense voltage through an internal comparator. An internal RC filter is connected at the CS pin which smoothes the switch-on current spike. The remaining switch-on spike is blanked out via an internal leading edge blanking (LEB) circuit. Another extra function of LEB is that it limits the system minimum on time, thus the THD of system at light load will be decreased.

The RS flip-flop ensures that only one single switch-on and switch-off pulse appears at the gate drive output during a given cycle.

- **Zero Current Detection**

OB6563 can perform zero current detection by using an auxiliary winding of the inductor. When the stored energy is fully released to the output, the voltage at ZCD decrease. A new switching cycle is initiated following the ZCD triggering. The turn on of power MOSFET is initiated at moment that the inductor's current reaches zero.

- **Disable Function**

When the ZCD pin is pulled low, OB6563 is disabled and some internal functional blocks are turned off. The operation current is very small under this condition until the ZCD pin is released.

- **Gate Drive Output**

The output stage is designed to ensure zero cross-conduction current. This minimizes heat dissipation, increase efficiency, and enhance reliability. The output driver is also slew rate controlled to minimize EMI. The built-in 16V clamp at the gate output protects the MOSFET gate from high voltage stress.

- **Protection Controls**

OB6563 ensures good reliability design through its good protection coverage. Output dynamic and static over-voltage protection (OVP), VCC under voltage lockout (UVLO), cycle-by-cycle current limiting and output gate clamp are standard features provided by OB6563.

- **System Open Loop Protection**

A new function of system open loop protection is provided in OB6563. The voltage at INV pin is sensed. If INV pin is below 0.25V typical, the switching will be stopped. In this way, the system output voltage cannot increase too high (only the rectified line voltage), and the pre-converter will be protected from damage.

PACKAGE MECHANICAL DATA

8-Pin Plastic DIP

DIP8 PACKAGE OUTLINE DIMENSIONS
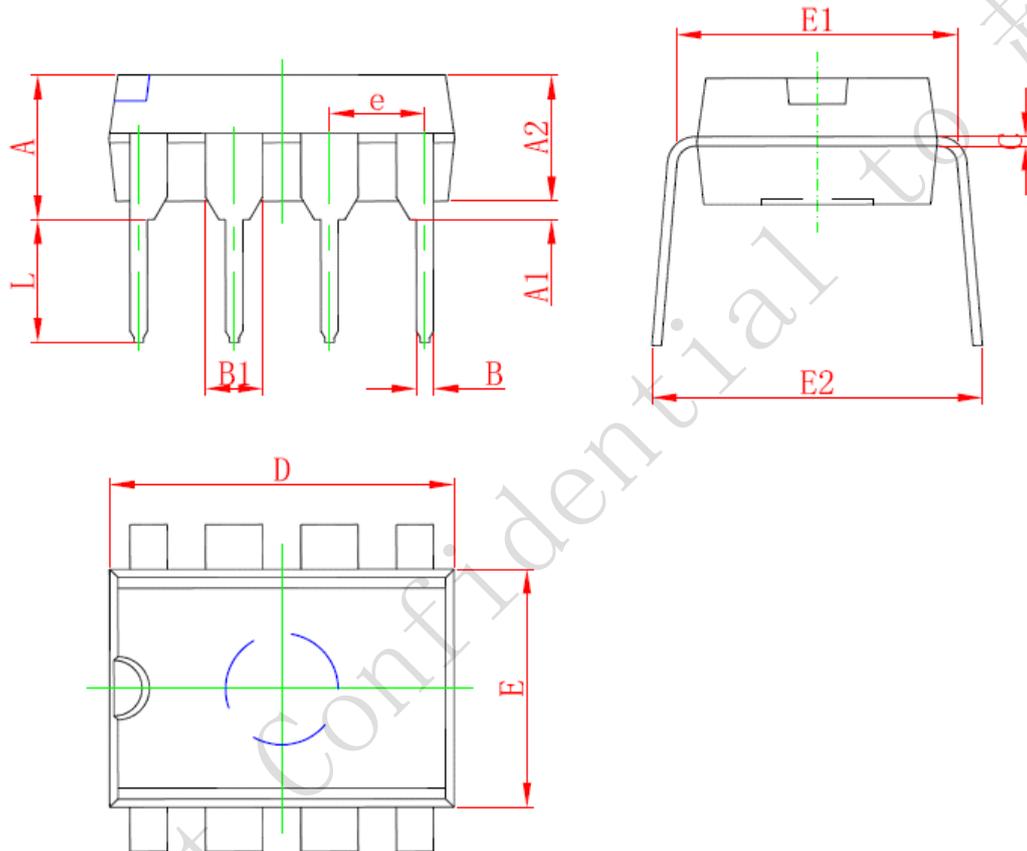
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	5.334	0.146	0.210
A1	0.381		0.015	
A2	2.921	4.953	0.115	0.195
B	0.350	0.650	0.014	0.026
B1	1.524 (BSC)		0.06 (BSC)	
C	0.200	0.360	0.008	0.014
D	9.000	10.160	0.354	0.400
E	6.096	7.112	0.240	0.280
E1	7.320	8.255	0.288	0.325
e	2.540 (BSC)		0.1 (BSC)	
L	2.921	3.810	0.115	0.150
E2	7.620	10.920	0.300	0.430

8-Pin Plastic SOP

SOP8 PACKAGE OUTLINE DIMENSIONS
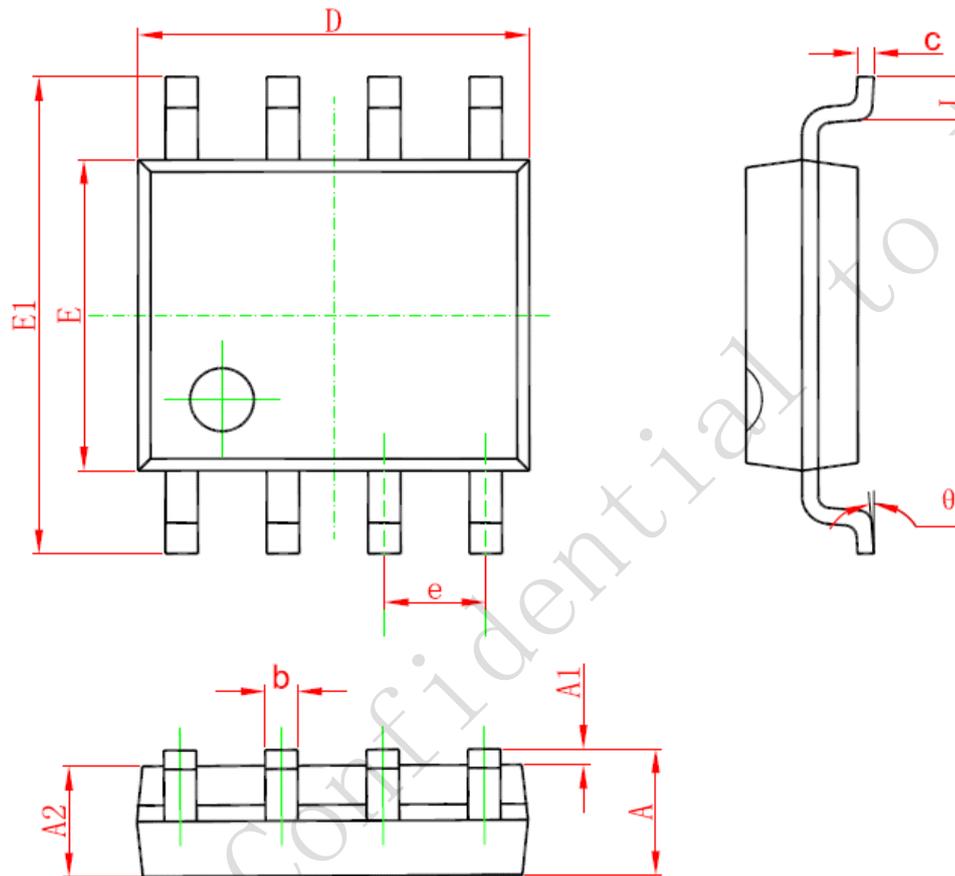
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.150	0.185	0.203
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.05 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0º	8º	0º	8º

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