XN21364S

600V Three-Phase Gate Driver Integrated Bootstrap Diode (BSD)

Features

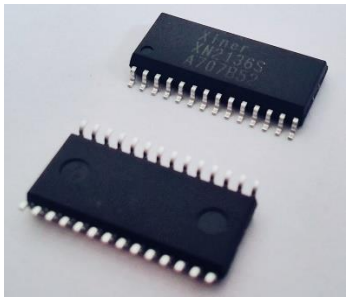
- Thick-film-SOI-technology
- Separate control circuits for all six drivers
- Designed for use with bootstrap power supplies
- Built-in BSD
- Over-current protection
- Shoot-through(cross-conduction) protection
- Undervoltage lockout for V_{CC} & V_{BS}
- Enable/disable input and fault reporting
- Adjustable fault clear timing
- Separate logic and power grounds
- 3.3V/5V/15V input logic compatible
- Output in phase with inputs
- Tolerant to negative transient voltage up to -50 V given by SOI technology
- Matched propagation delays for all channels
- SOP28 package available

Product summary

Topology	3 Phase
V_{OFFSET}	= 600 V max.
$I_{O+/-}$ (typ.)	= 0.2 A/0.35 A
V_{OUT}	= 10 V - 17.5 V
$t_{on/off}$ (typ.)	= 600 ns/600 ns

Package

SOP28



Application

- Motor drivers
- Home appliances
- IGBT and power MOS gate drivers for general purpose

Description

The XN21364 are high voltage, high speed, power IGBT gate drivers with three high-side and three low-side referenced output channels for 3-phase applications. This IC is designed to be used with low-cost bootstrap power supplies and integrated BSD.

Based on the used SOI-technology there is an excellent ruggedness on transient voltages. No parasitic thyristor structures are present in the device. Hence, no parasitic latch-up may occur at all temperatures and voltage conditions. The floating logic input is compatible with standard CMOS or LSTTL outputs (down to 3.3 V logic). A current trip function which terminates all six outputs can be derived from an external current sense resistor. Enable functionality is available to terminate all six outputs simultaneously. An open-drain FAULT signal is provided to indicate that a fault (e.g., over-current or undervoltage shutdown event) has occurred. Fault conditions are cleared automatically after a delay programmed externally via an RC network connected to the RCIN input. The output drivers feature a high-pulse current buffer stage designed for minimum driver cross-conduction. Shoot-through protection circuitry have been integrated into this IC. Propagation delays are matched to simplify the HVIC's use in high frequency applications.
The floating channels can be used to drive N-channel IGBTs/MOSFETs in the high-side configuration, which operate up to 600 V.

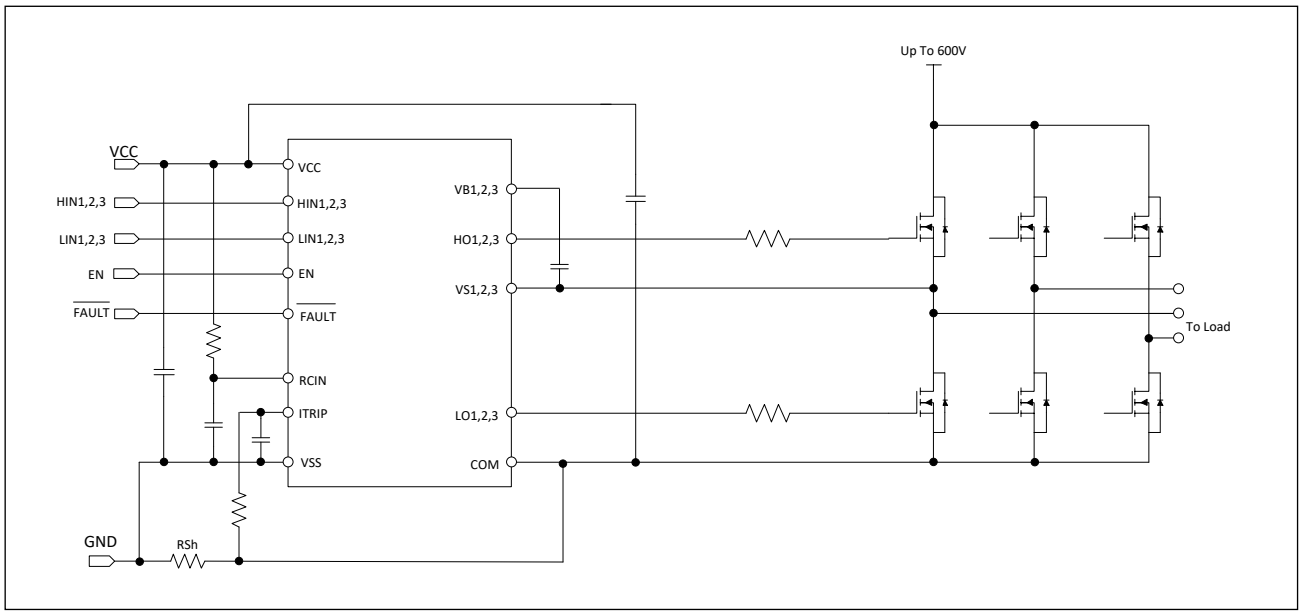


Figure 1 Typical application diagram

Ordering information

Base Part Number	Package	Standard Pack		Orderable Part Number
		Form	Quantity	
XN21364S	SOP28	Tube/Bulk	27	XN21364S
		Tape and Reel	1000	XN21364STR

1. Block diagram

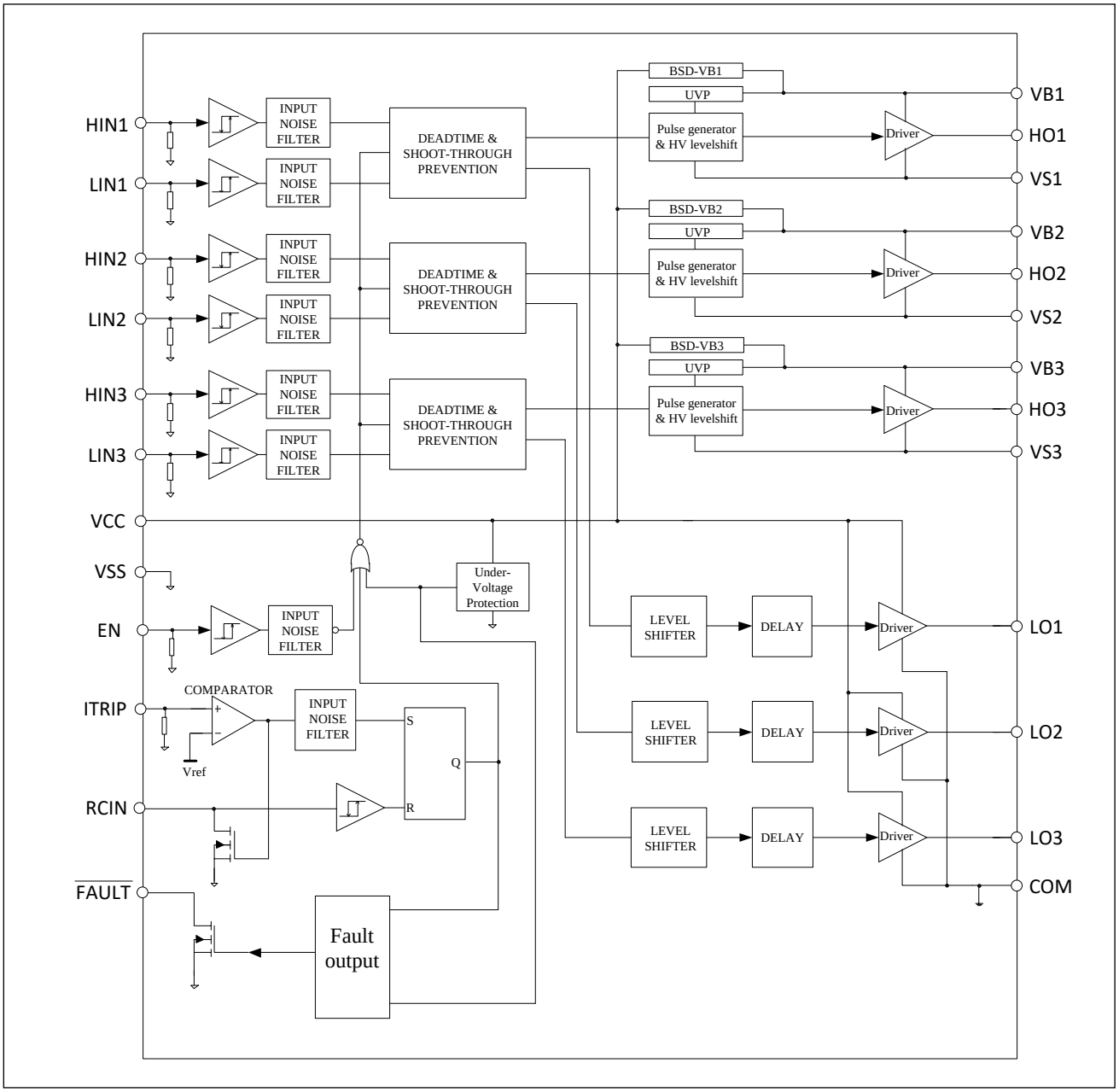


Figure 2 Function block diagram

2. Lead definitions

Table 1 XN21364S lead definitions

Name	Function
VCC	Low side and logic fixed supply
VSS	Logic Ground
HIN1,2,3	Logic inputs for high side gate driver outputs(HO1,2,3), in phase
LIN1,2,3	Logic inputs for low side gate driver outputs(LO1,2,3), in phase
FAULT/N	Indicates over-current (ITRIP) or low-side undervoltage lockout has occured. Negative logic open-drain output
ITRIP	Analog input for over current shutdown. When active, ITRIP shuts down outputs and Activates FAULT and RCIN low. When ITRIP becomes inactive, FAULT stays active low for an externally set time T_{FLTCLR}, then automatically becomes inactive (open-drain high impedance).
EN	Logic input to shutdown functionality. Logic functions when EN is high (i.e., positive logic). No effect on FAULT and not latched.
RCIN	External RC network input used to define FAULT CLEAR delay, T_{FLTCLR}, approximately equal to R*C. When RCIN>8V, the FAULT pin goes back into open-drain high-impedance
COM	Low side gate driver return
VB1,2,3	High side floating supply
HO1,2,3	High side gate driver outputs
VS1,2,3	High voltage floating supply returns
LO1,2,3	Low side gate driver output

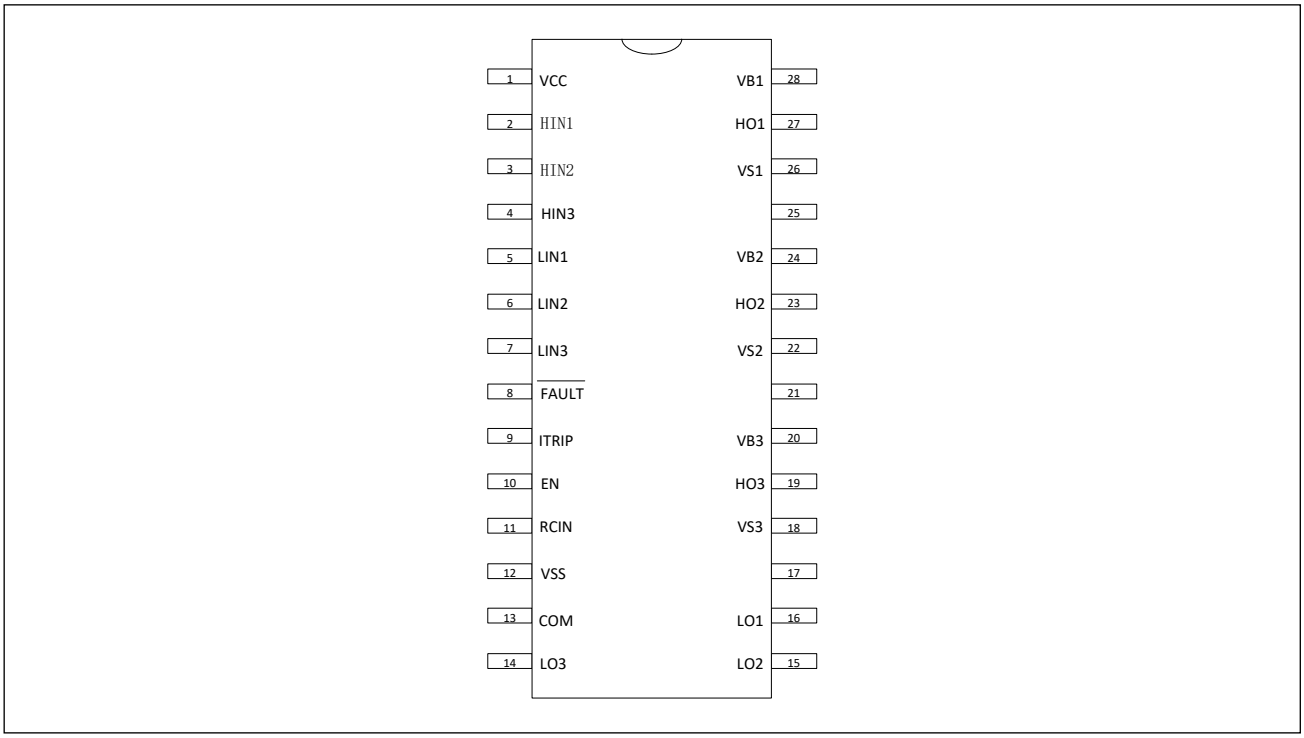


Figure 3 XN21364S lead assignments SOP28(top view)

3. Electrical parameters

3.1 Absolute maximum ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to V_{SS} unless otherwise stated in the table. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Table 2 Absolute maximum ratings

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating well supply voltage	-0.3	625	V
V_S	High-side floating well supply return voltage	V_B-25	V_B+0.3	
V_{HO}	Floating gate drive output voltage	V_S-0.3	V_B+0.3	
V_{BS}	Floating gate drive voltage supply voltage	-0.3	25	
V_{CC}	Low side supply voltage	-0.3	25	
V_{LO}	Low-side output voltage	-0.3	V_{CC}+0.3	
V_{IN}	Logic input voltage (LIN, HIN, EN)	-0.3	V_{CC}+0.3	
V_{ITRIP}	ITRIP pin voltage	-0.3	5	
COM	Power ground	-5	5	
V_{RCIN}	RCIN input voltage	-0.3	V_{CC}+0.3	
V_{FLT}	FAULT output voltage	-0.3	V_{CC}+0.3	
dV_S/dt	Allowable V_S offset supply transient relative to V_{SS}	-	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25$ ºC	-	1.6	W
Rth_{JA}	Thermal resistance, junction to ambient	-	78	℃/W
T_J	Junction temperature	-	150	℃
T_S	Storage temperature	-50	150	
T_L	Lead temperature (soldering, 10 seconds)	-	300	

3.2 Recommended operating conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to V_{SS} unless otherwise stated in the table. The offset rating is tested with supplies of (V_{CC} – V_{SS}) =(V_B – V_S) = 15 V.

Table 3 Recommended operating conditions

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating well supply voltage	V_S+10	V_S+20	V
V_S	High-side floating well supply return voltage	-5	600	
V_{HO}	Floating gate drive output voltage	V_S	V_B	
V_{BS}	Floating gate drive voltage supply voltage	10	20	
V_{CC}	Low side supply voltage	10	20	
V_{LO}	Low-side output voltage	COM	V_{CC}	

COM	Power ground	-5	5	
V_{IN}	Logic input voltage (LIN, HIN, EN)	V_{SS}	V_{CC}	
V_{ITRIP}	ITRIP pin voltage	V_{SS}	5	
V_{RCIN}	RCIN input voltage	V_{SS}	V_{CC}	
V_{FLT}	FAULT output voltage	V_{SS}	V_{CC}	
T_A	Ambient temperature	-40	125	℃
t_{IN}	Pulse width for ON and OFF	0.5	-	us

3.3 Static electrical characteristics

(V_{CC} – V_{SS}) = (V_B – V_S) = 15 V, and T_A = 25°C unless otherwise specified. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to V_{SS} and are applicable to the respective input leads: H_{IN} and L_{IN}. The V_O and I_O parameters are referenced to V_{SS} /V_S and are applicable to the respective output leads H_O or L_O. The V_{CCUV} parameters are referenced to V_{SS}. The V_{BSUV} parameters are referenced to V_S.

Table 4 Static electrical characteristics

Symbol	Definition	Min.	TYP.	Max.	Units	Test Conditions
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	9.7	10.6	12	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	9.5	10.4	11.8		
V_{BSUVHY}	V_{BS} supply undervoltage hysteresis	-	0.2	-		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	10.2	11.1	12.5		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	10	10.9	12.3		
V_{CCUVHY}	V_{CC} supply undervoltage hysteresis	-	0.2	-		
I_{LK}	High-side floating well offset supply leakage	-	1	5	uA	V_B = V_S = 600 V
I_{LK}	High-side floating well offset supply leakage	-	5	10		T_J = 125 °C, V_B = V_S = 600 V
I_{QBS}	Quiescent V_{BS} supply current	-	15	30		
I_{QCC}	Quiescent V_{CC} supply current	-	3	10	mA	
V_{OH}	High level output voltage drop, V_{BIAS}-V_O	-	0.7	1.5	V	I_O = 20mA
V_{OL}	Low level output voltage drop, V_O	-	0.3	0.5		
I_{o+}	Peak output current turn-on	120	200	-	mA	V_O = 0 V PW = 10 µs
I_{o-}	Peak output current turn-off	210	350	-		V_O = 15 V PW = 10 µs
V_{IH}	Logic “1” input voltage	2.9	-	-	V	
V_{IL}	Logic “0” input voltage	-	-	1.0		
$V_{EN,TH+}$	Enable positive going threshold	2.9	-	-		

V_{ENTH-}	Enable negative going threshold	-	-	1.0		
$V_{IT,TH+}$	ITRIP positive going threshold	0.45	0.5	0.55		
$V_{IT,HYS}$	ITRIP input hysteresis	-	0.07	-		
$V_{RCIN,\ TH+}$	RCIN positive going threshold	-	8	--		
$V_{RCIN,\ HYS}$	RCIN input hysteresis	-	3	-		
I_{IN+}	Input bias current (H_O = High)	-	100	-	uA	V_{IN} = 3.3 V
I_{IN-}	Input bias current (H_O = Low)	-	0	-		V_{IN} = 0 V
I_{EN+}	"High" enable input bias current	-	17	-		V_{IN} = 3.3 V
I_{EN-}	"Low" enable input bias current	-	0	-		V_{IN} = 0 V
I_{ITRIP+}	"High" ITRIP input bias current	-	2	-		V_{IN} = 0.45 V
I_{ITRIP-}	"Low" ITRIP input bias current	-	0	1		V_{IN} = 0 V
I_{RCIN+}	RCIN input bias current	-	0	1		V_{IN} = 15 V
I_{RCIN-}	RCIN input bias current	-	0	1		V_{IN} = 0 V
$R_{ON,RCIN}$	RCIN low on resistance	-	50	100	Ω	I=10mA
$R_{ON,FAULT}$	FAULT low on resistance	-	50	100		
V_{FDB}	Bootstrap diode forward voltage	-	1	1.5	V	I=1mA

3.3 **Dynamic electrical characteristics**

V_{CC} = V_{BS}= 15 V, V_S = V_{SS}, T_A = 25°C and C_L = 1000 pF unless otherwise specified.

Table 5 Dynamic electrical characteristics

Symbol	Definition	Min.	TYP.	Max.	Units	Test Conditions
t_{ON}	Turn-on propagation delay	-	600	1300	ns	$V_{LIN/HIN}$ = 0 or 5 V
t_{OFF}	Turn-off propagation delay	-	600	1300		
t_R	Turn-on rise time	-	50	80		$V_{LIN/HIN}$ = 0 or 5 V C_L = 1 nF
t_F	Turn-off fall time	-	25	40		
t_{ITRIP}	ITRIP to output shutdown propagation delay	-	2	-	us	$V_{LIN/HIN}$ = 0 & 5 V
t_{BL}	ITRIP blanking time	-	500	-	ns	V_{IN} = 0 V or 5 V
t_{EN}	Enable low to output shutdown propagation delay	-	0.6	1.3	us	V_{IN}, V_{EN} = 0 V or 5 V
t_{FLTCLR}	FAULT clear time RCIN: R = 2 MΩ, C = 1 nF	0.9	1.7	2.5	ms	V_{IN} = 0 V or 5 V V_{ITRIP} = 0 V
MT	Delay matching time	-	-	50	ns	
MDT	Dead time matching time	-	-	50		

4. Functions and Operations

The relationship between the input and output signals of the XN21364 are illustrated below in Figures 4 . From these figures, we can see the definitions of several timing parameters (i.e., PW_{IN}, PW_{OUT}, t_{ON}, t_{OFF}, t_R, and t_F) associated with this device.

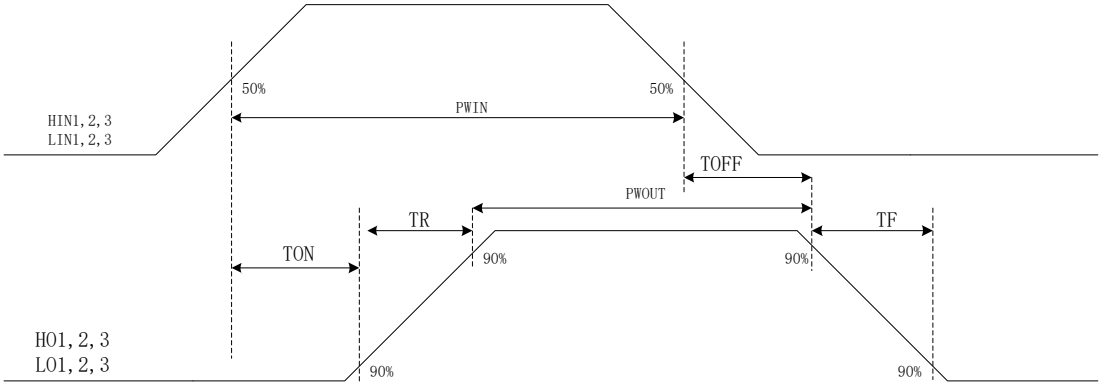


Figure4: Switching time waveforms

The following two figures illustrate the timing relationships of some of the functionality of the XN21364; this functionality is described in further detail later in this document.

During interval A of Figure 5, the HVIC has received the command to turn-on both the high- and low-side switches at the same time; as a result, the shoot-through protection of the HVIC has prevented this condition and both the highand low-side output are held in the off state.
Interval B of Figures 5 and 6 shows that the signal on the ITRIP input pin has gone from a low to a high state; as a result, all of the gate drive outputs have been disabled (i.e., see that HOx has returned to the low state; LOx is also held low), the voltage on the RCIN pin has been pulled to 0 V, and a fault is reported by the FAULT output transitioning to the low state. Once the ITRIP input has returned to the low state, the output will remain disabled and the fault condition reported until the voltage on the RCIN pin charges up to $V_{RCIN,TH}$ (see interval C in Figure 6); the charging characteristics are dictated by the RC network attached to the RCIN pin.

During intervals D and E of Figure 5, we can see that the enable (EN) pin has been pulled low (as is the case when the driver IC has received a command from the control IC to shutdown); this results in the outputs (HOx and LOx)being held in the low state until the enable pin is pulled high.

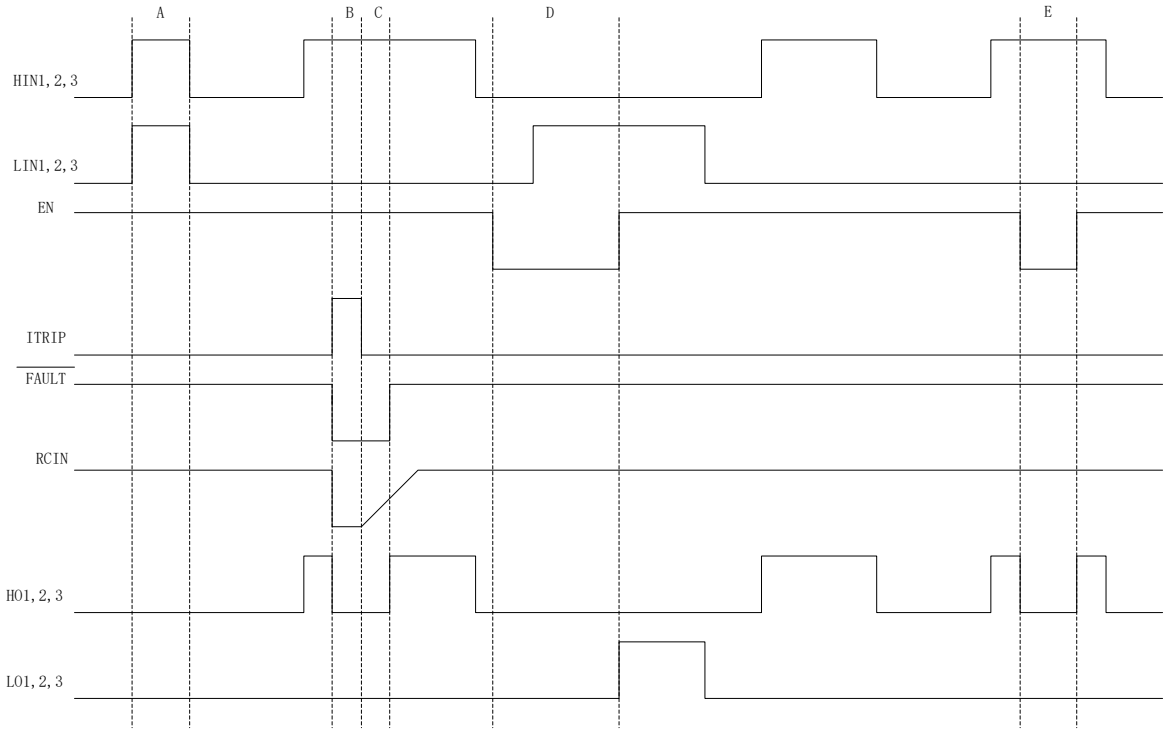


Figure5: Input/output timing diagram for the XN21364

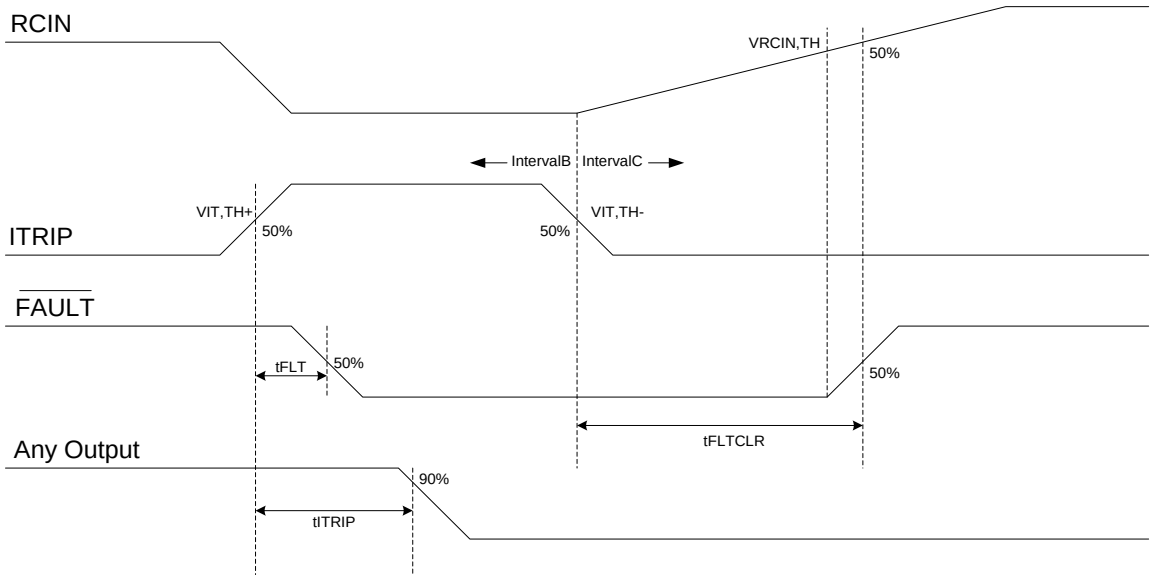


Figure6: Detailed view of B & C intervals

Undervoltage Lockout Protection

This family of ICs provides undervoltage lockout protection on both the V_{CC} (logic and low-side circuitry) power supply and the V_{BS} (high-side circuitry) power supply. Figure 7 is used to illustrate this concept; V_{CC} (or V_{BS}) is plotted over time and as the waveform crosses the UVLO threshold ($V_{CCUV+/-}$ or $V_{BSUV+/-}$) the undervoltage protection is enabled or disabled.

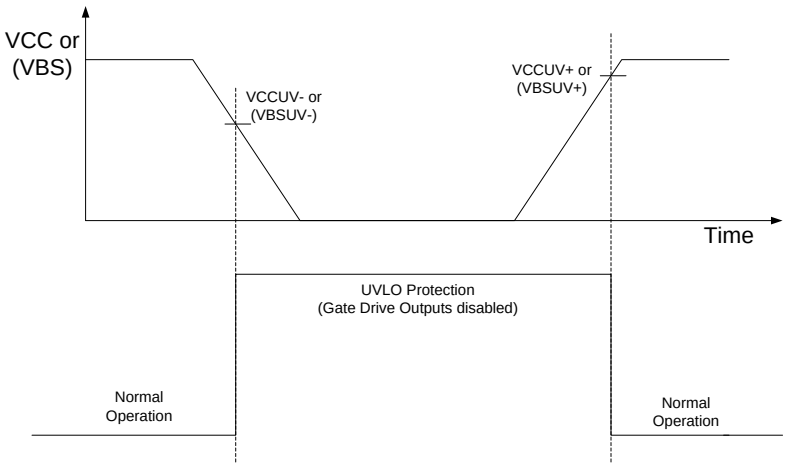


Figure 7: UVLO Protection

Enable Input

The XN21364 is equipped with an enable input pin that is used to shutdown or enable the HVIC. When the EN pin is in the high state the HVIC is able to operate normally (assuming no other fault conditions). When a condition occurs that should shutdown the HVIC, the EN pin should see a low logic state.
Table 6 gives a summary of this pin's functionality and Figure 8 illustrates the outputs' response to a shutdown command.

Enable Input	
Enable input high	Outputs enabled
Enable input low	Outputs disabled

Table 6: Enable functionality truth table

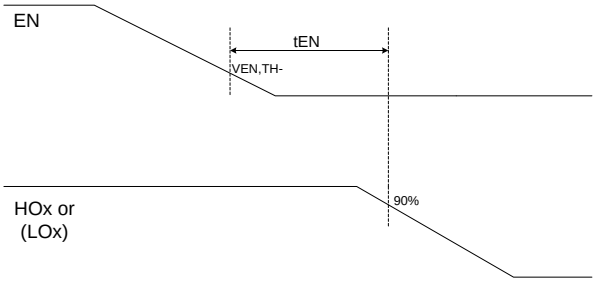


Figure 8: Output enable timing waveform

Fault Reporting and Programmable Fault Clear Timer

The XN21364 provides an integrated fault reporting output and an adjustable fault clear timer. There are two situations that would cause the HVIC to report a fault via the FAULT pin. The first is an undervoltage condition of V_{CC} and the second is if the ITRIP pin recognizes a fault. Once the fault condition occurs, the FAULT pin is internally pulled to V_{SS} and the fault clear timer is activated. The fault output stays in the low state until the fault condition has been removed and the fault clear timer expires; once the fault clear timer expires, the voltage on the FAULT pin will return to V_{CC}.

The length of the fault clear time period (t_{FLTCLR}) is determined by exponential charging characteristics of the capacitor where the time constant is set by R_{RCIN} and C_{RCIN}. In Figure 9 where we see that a fault condition has occurred (UVLO or ITRIP), RCIN and FAULT are pulled to V_{SS}, and once the fault has been removed, the fault clear timer begins. Figure 10 shows that R_{RCIN} is connected between the V_{CC} and the RCIN pin, while C_{RCIN} is placed between the RCIN and V_{SS} pins.

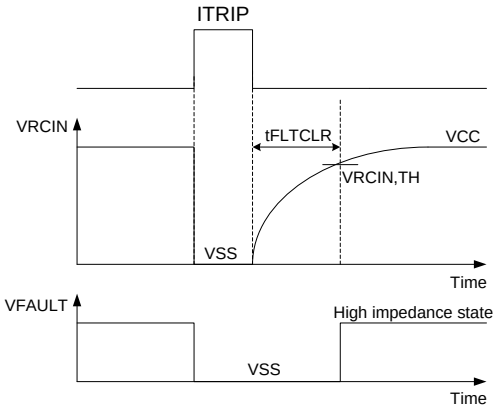


Figure 9: RCIN and FAULT pin waveforms

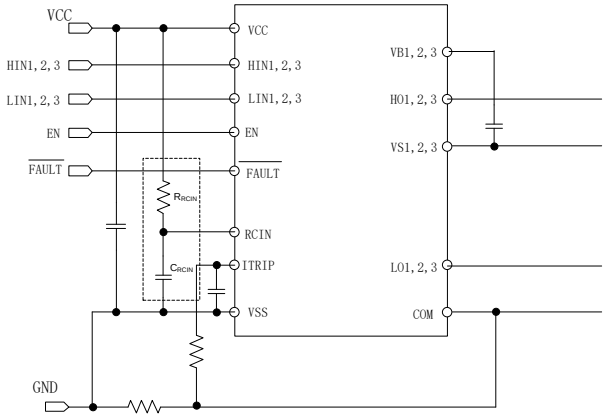


Figure 10: Programming the fault clear timer

Over-Current Protection

The XN21364 is equipped with an ITRIP input pin. This functionality can be used to detect over-current events in the DC- bus. Once the HVIC detects an over-current event through the ITRIP pin, the outputs are shutdown, a fault is reported through the FAULT pin, and RCIN is pulled to V_{SS}.

The level of current at which the over-current protection is initiated is determined by the resistor connected to ITRIP as shown in Figure 11, and the ITRIP threshold ($V_{IT,TH+}$). The circuit designer will need to determine the maximum allowable level of current in the DC- bus and select resistor.

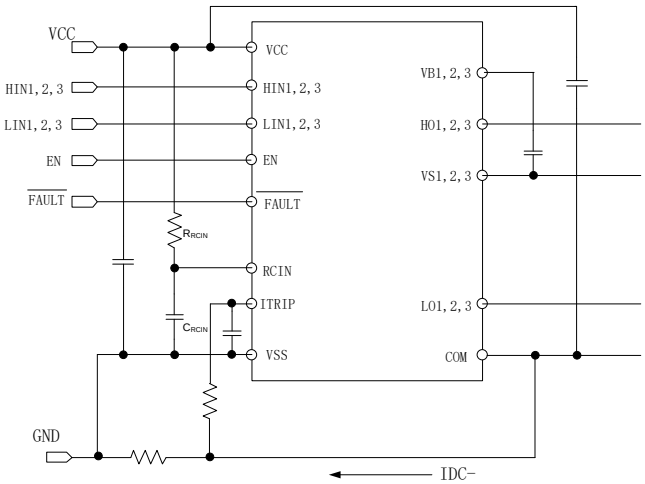


Figure 11: Programming the over-current protection

Truth Table: Undervoltage lockout, ITRIP, and ENABLE

Table 8 provides the truth table for the XN21364. The first line shows that the UVLO for V_{CC} has been tripped; the FAULT output has gone low and the gate drive outputs have been disabled. V_{CCUV} is not latched in this case and when V_{CC} is greater than V_{CCUV}, the FAULT output returns to the high impedance state.

The second case shows that the UVLO for V_{BS} has been tripped and that the high-side gate drive outputs have been disabled. After V_{BS} exceeds the V_{BSUV} threshold, HO will stay low until the HVIC input receives a new rising transition of HIN. The third case shows the normal operation of the HVIC. The fourth case illustrates that the ITRIP trip threshold has been reached and that the gate drive outputs have been disabled and a fault has been reported through the fault pin. In the last case, the HVIC has received a command through the EN input to shutdown; as a result, the gate drive outputs have been disabled.

	VCC	VBS	ITRIP	EN	RCIN	FAULT	LO	HO
UVLO V_{CC}	<V_{CCUV}	—	—	—	High	0	0	0
UVLO V_{BS}	15 V	<V_{BSUV}	0 V	5 V	High	High impedance	LIN	0
Normal operation	15 V	15 V	0 V	5 V	High	High impedance	LIN	HIN
ITRIP fault	15 V	15 V	>V_{ITRIP}	5 V	Low	0	0	0
EN command	15 V	15 V	0 V	0 V	High	High impedance	0	0

Table 8: UVLO, ITRIP, EN, RCIN, & FAULT truth table

5. Package information SOP28

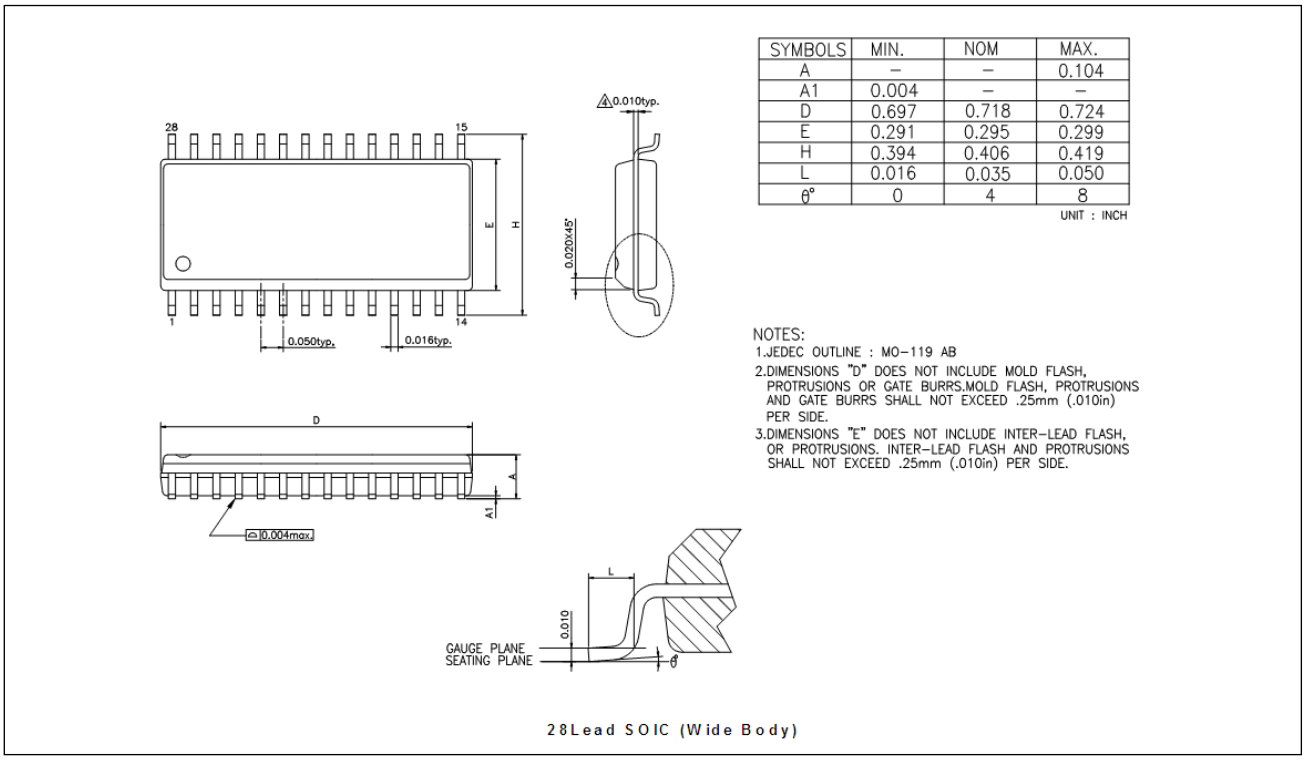


Figure 12 Package outline SOP28

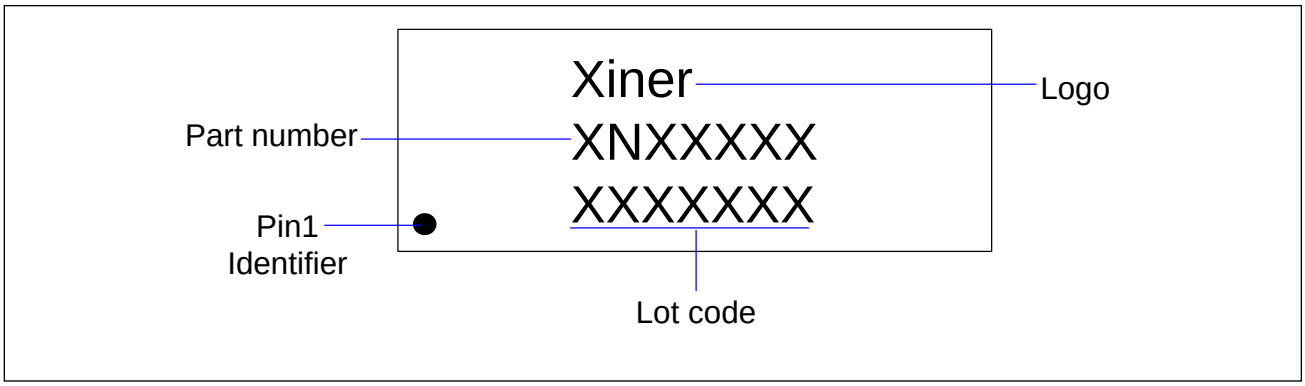
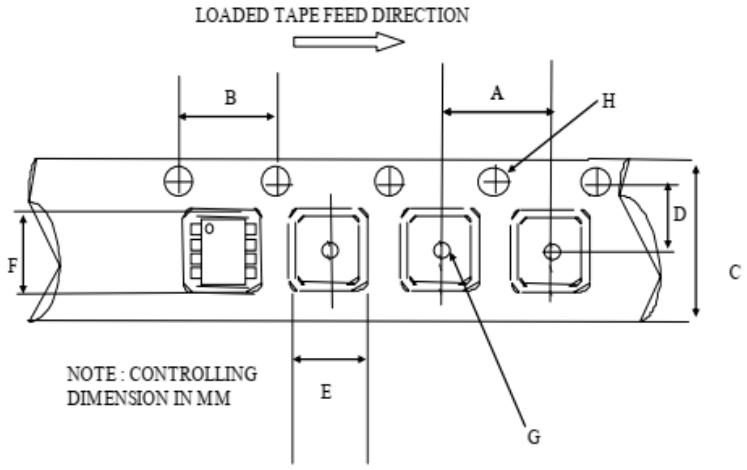
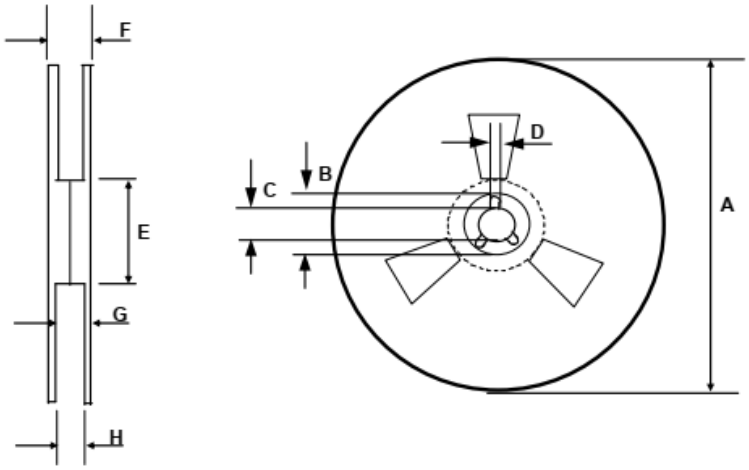


Figure 13 Marking information SOP28



CARRIER TAPE DIMENSION FOR 28SOICW

Code	Metric		Imperial	
	Min	Max	Min	Max
A	11.90	12.10	0.468	0.476
B	3.90	4.10	0.153	0.161
C	23.70	24.30	0.933	0.956
D	11.40	11.60	0.448	0.456
E	10.80	11.00	0.425	0.433
F	18.20	18.40	0.716	0.724
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 28SOICW

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	30.40	n/a	1.196
G	26.50	29.10	1.04	1.145
H	24.40	26.40	0.96	1.039

Figure 14 Tape and reel details SOP28

6. Qualification information

Table 9 Qualification information

Moisture sensitivity level		SOP28	MSL3, 260°C (per IPC/JEDEC J-STD-020)
ESD	Charged device model	Class C3 (> 1.0 kV) (per JESD22-C101)	
	Human body model	Class 2 (per JEDEC standard JESD22-A114)	
IC latch-up test		Class II Level A (per JESD78)	
RoHS compliant		Yes	

Revision history

Document version	Date of release	Description of changes
1.0	2020-12-01	Preliminary datasheet
2.0	2021-05-31	First release version