MOC3162
MOC3163

6-Pin DIP Zero-Cross Optoisolators Triac Driver Output

(600 Volts Peak)

GlobalOptoisolator™

VDE | UL | CSA | SETI | SEMKO | DEMKO | NEMKO | BABT

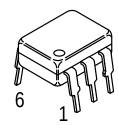
The MOC3162 and MOC3163 devices consist of gallium arsenide infrared emitting diodes optically coupled to monolithic silicon detectors performing the functions of Zero Voltage Crossing bilateral triac drivers.

They are designed for use with a triac in the interface of logic systems to equipment powered from 115/240 Vac lines, such as solid–state relays, industrial controls, motors, solenoids and consumer appliances, etc.

- Simplifies Logic Control of 115/240 Vac Power
- Zero Voltage Turn–On
- dv/dt of 1000 V/µs Guaranteed Minimum @ 600 V Peak
- I_{FT} Insensitive to Static dv/dt (Within Rated V_{DRM})
- ***To order devices that are tested and marked per VDE 0884 requirements, the suffix "V" must be included at end of part number. VDE 0884 is a test option.***

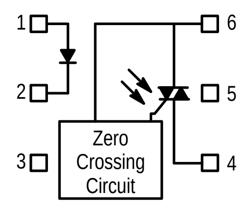
Recommended for 115/240 Vac(rms) Applications:

- Solenoid/Valve Controls
- Lighting Controls
- Static Power Switches
- AC Motor Drives
- Static AC Power Switch
- Temperature Controls
- E.M. Contactors
- AC Motor Starters
- Solid State Relays



STANDARD THRU HOLE

COUPLER SCHEMATIC



1. ANODE
2. CATHODE
3. NC
4. MAIN TERMINAL
5. SUBSTRATE DO NOT CONNECT
6. MAIN TERMINAL

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INFRARED EMITTING DIODE			
Reverse Voltage	V_R	6.0	Volts
Forward Current — Continuous	I_F	60	mA
Total Power Dissipation @ T_A = 25°C Negligible Power in Output Driver Derate above 25°C	P_D	120 1.60	mW mW/°C
OUTPUT DRIVER			
Off–State Output Terminal Voltage	V_{DRM}	600	Volts
Peak Repetitive Surge Current (PW = 100 µs, 120 pps)	I_{TSM}	1.0	A
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	150 2.0	mW mW/°C
TOTAL DEVICE			
Isolation Surge Voltage (1) (Peak ac Voltage, 60 Hz, 1 Second Duration)	V_{ISO}	7500	Vac(pk)
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	250 3.3	mW mW/°C
Junction Temperature Range	T_J	–40 to +100	°C
Ambient Operating Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–40 to +150	°C
Soldering Temperature (10 s)	T_L	260	°C

1. Isolation surge voltage, V_{ISO}, is an internal device dielectric breakdown rating. For this test, Pins 1 and 2 are common, and Pins 4, 5 and 6 are common.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT LED					
Reverse Leakage Current (V_R = 6.0 V)	I_R	—	0.05	100	μA
Forward Voltage (I_F = 30 mA)	V_F	—	1.15	1.5	Volts
OUTPUT DETECTOR (I_F = 0)					
Leakage with LED Off, Either Direction (Rated V_{DRM}, Note 1)	I_{DRM}	—	10	100	nA
Critical Rate of Rise of Off–State Voltage (Note 3) @ 600 V Peak	dv/dt	1000	—	—	V/μs
COUPLED					
LED Trigger Current, Current Required to Latch Output (Main Terminal Voltage = 3.0 V, Note 2) MOC3162	I_{FT}	—	—	10	mA
MOC3163		—	—	5.0	
Peak On–State Voltage, Either Direction (I_{TM} = 100 mA Peak, I_F = Rated I_{FT})	V_{TM}	—	1.7	3.0	Volts
Holding Current, Either Direction	I_H	—	200	—	μA
Inhibit Voltage (MT1–MT2 Voltage Above Which Device Will Not Trigger) (I_F = Rated I_{FT})	V_{INH}	—	8.0	15	Volts
Leakage in Inhibited State (I_F = 10 mA Maximum, at Rated V_{DRM}, Off State)	I_{DRM2}	—	250	500	μA

1. Test voltage must be applied within dv/dt rating.
2. All devices are guaranteed to trigger at an I_F value less than or equal to max I_{FT}. Therefore, recommended operating I_F lies between max I_{FT} (10 mA for MOC3162, 5.0 mA for MOC3163) and absolute max I_F (60 mA).
3. This is static dv/dt. See Figure 9 for test circuit. Commutating dv/dt is a function of the load–driving thyristor(s) only.

TYPICAL ELECTRICAL CHARACTERISTICS

T_A = 25°C

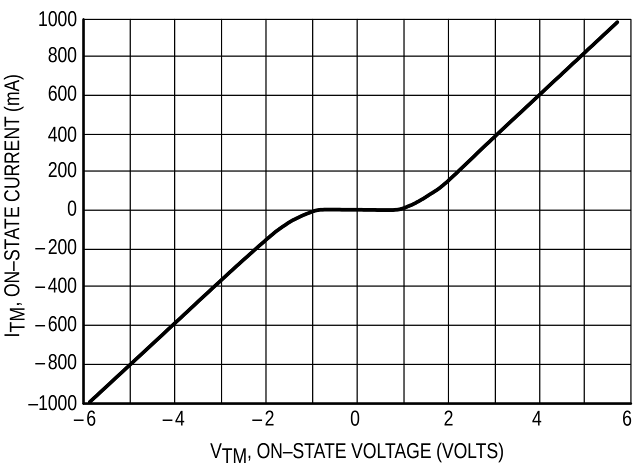


Figure 1. On–State Characteristics

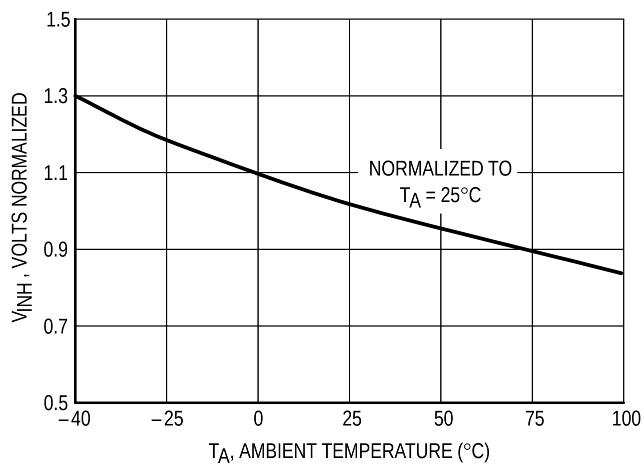


Figure 2. Inhibit Voltage versus Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

$T_A = 25°C$

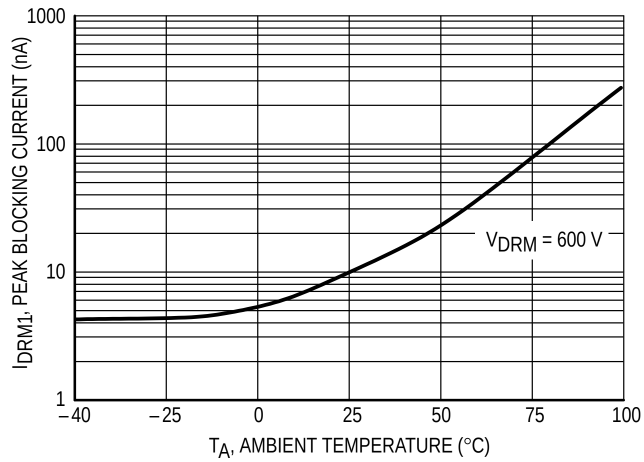


Figure 3. Leakage with LED Off versus Temperature

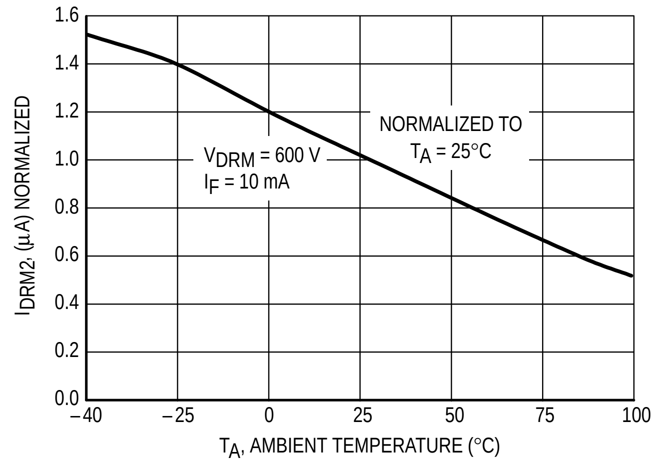


Figure 4. I_{DRM2}, Leakage in Inhibit State versus Temperature

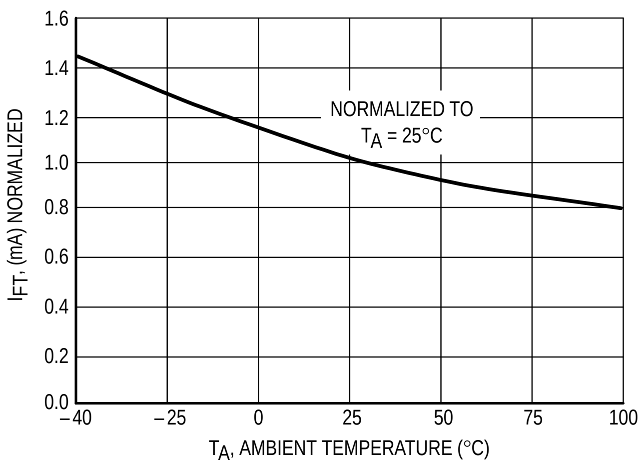


Figure 5. Trigger Current versus Temperature

I_{FT} versus Temperature (Normalized)

This graph shows the increase of the trigger current when the device is expected to operate at an ambient temperature below 25°C. Multiply the normalized I_{FT} shown on this graph with the data sheet guaranteed I_{FT}.

Example:
T_A = – 40°C, I_{FT} = 10 mA
I_{FT} @ – 40°C = 10 mA x 1.4 = 14 mA

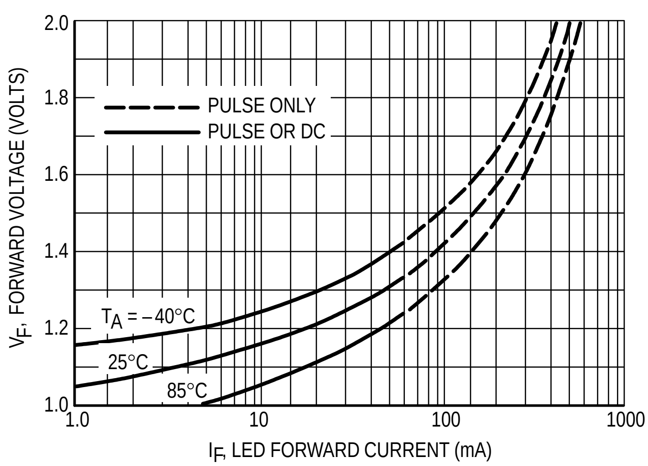


Figure 6. LED Forward Voltage versus Forward Current

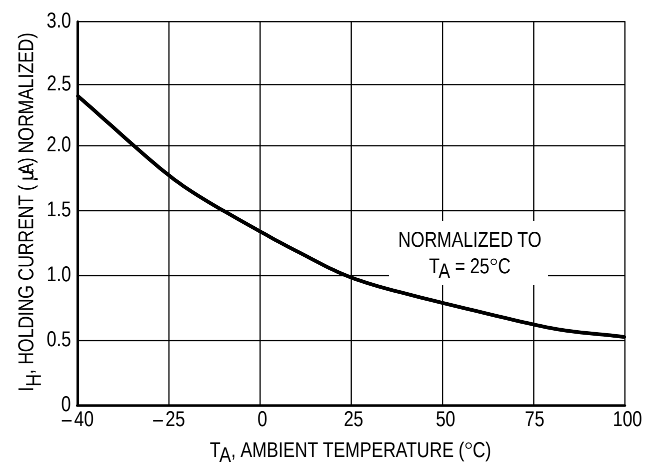


Figure 7. Holding Current, I_H versus Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

T_A = 25°C

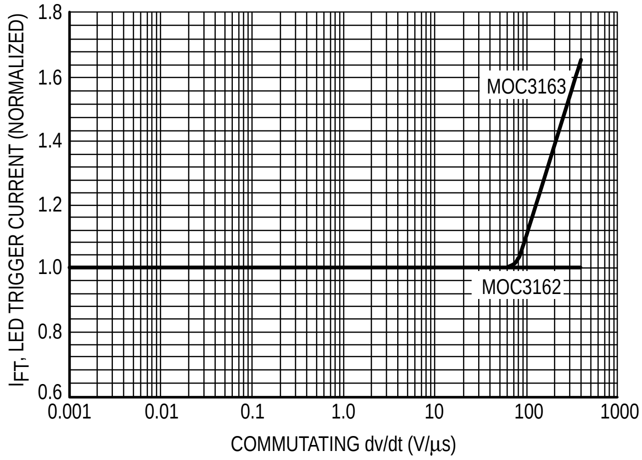


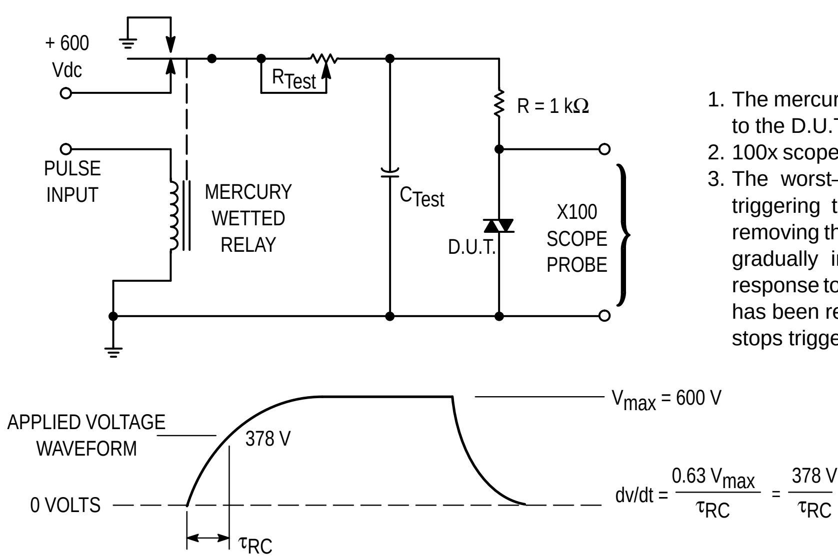
Figure 8. LED Trigger Current, I_{FT}, versus dv/dt

I_{FT} versus dv/dt

Triac drivers with good noise immunity (dv/dt stat.) have internal noise rejection circuits which prevent false triggering of the device in the event of fast raising line voltage transients. Inductive loads generate a commutating dv/dt that may activate the triac driver’s noise suppression circuits. This prevents the device from turning on at its specified trigger current. It will in this case go into the mode of “half–waving” of the load. Half–waving of the load may destroy the power triac and the load.

Figure 8 shows the dependency of the triac drivers I_{FT} versus the reapplied voltage rise with a V_p of 600 V. This dv/dt condition simulates a worst case commutating dv/dt amplitude.

It can be seen that the required trigger current I_{FT} changes with increased dv/dt. Practical loads generate a commutating dv/dt of less than 50 V/µs. The rate of rise of the commutating dv/dt is effectively slowed by the use of snubber networks across the main triac. This snubber is also needed to keep the commutating dv/dt generated by inductive loads within the commutating dv/dt ratings of the power triac.



1. The mercury wetted relay provides a high speed repeated pulse to the D.U.T.
2. 100x scope probes are used, to allow high speeds and voltages.
3. The worst–case condition for static dv/dt is established by triggering the D.U.T. with a normal LED input current, then removing the current. The variable R_{TEST} allows the dv/dt to be gradually increased until the D.U.T. continues to trigger in response to the applied voltage pulse, even after the LED current has been removed. The dv/dt is then decreased until the D.U.T. stops triggering. τ_{RC} is measured at this point and recorded.

Figure 9. Static dv/dt Test Circuit

TYPICAL ELECTRICAL CHARACTERISTICS

T_A = 25°C

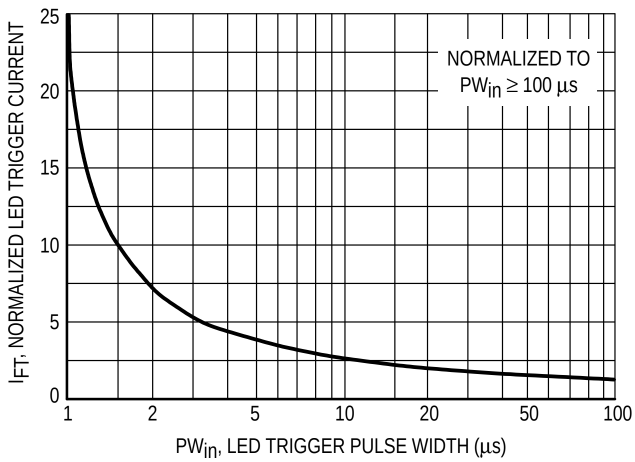


Figure 10. LED Current Required to Trigger versus LED Pulse Width

LED Trigger Current versus PW (Normalized)

For resistive loads the triac drivers may be controlled by short pulse into the input LED. This input pulse must be synchronized with the AC line voltage zero–crossing points. LED trigger pulse currents shorter than 100 μs must have an increased amplitude as shown on Figure 10. This graph shows the dependency of the trigger current I_{FT} versus the pulse width t(PW). I_{FT} in the graph, I_{FT} versus (PW), is normalized in respect to the minimum specified I_{FT} for static condition, which is specified in the device characteristic. The normalized I_{FT} has to be multiplied with the device's guaranteed static trigger current.

Example:
Guaranteed I_{FT} = 10 mA, Trigger pulse width PW = 3.0 μs
I_{FT}(pulsed) = 10 mA x 5.0 = 50 mA

APPLICATIONS GUIDE

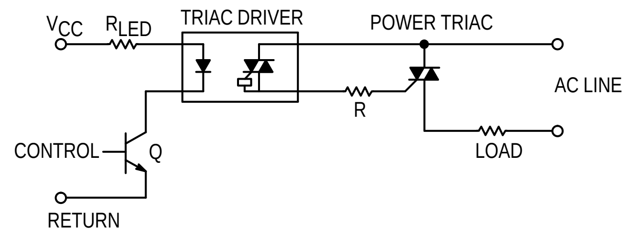
BASIC APPLICATIONS

Basic Triac Driver Circuit

Zero–cross triac drivers are very immune to static dv/dt. This allows snubberless operations in all applications where the external generated noise amplitude and rate of rise in the AC line is not exceeding the devices' guaranteed limits. For these applications a snubber circuit is not necessary when a noise insensitive power triac is used. Figure 11 shows the circuit diagram. The triac driver is directly connected to the triac main terminal 2 and a series Resistor R which limits the current to the triac driver. Current limiting resistor R could be very small for normal operation since the triac driver can be only switched on within the zero–cross window. Worst case consideration, however, considers accidental turn on at the peak of the line voltage due to a line transient exceeding the devices' maximum ratings. For this reason R should be calculated to limit the current to I_{drm} max at the peak of the line voltage.

$R = V_p$ AC/I_{TM} max rep. $= V_p$ AC/1A

The power dissipation of this current limiting resistor and the triac driver is very small because the power triac carries the load current as soon as the current through driver and current limiting resistor reaches the trigger current of the power triac. The switching transition time for the driver is only one micro second and for power triacs typical four micro seconds.

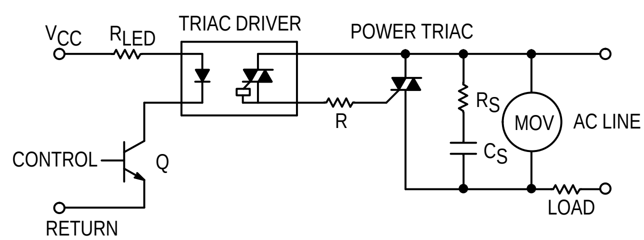


$R_{LED} = (V_{CC} - V_F$ LED $- V_{sat}$ Q$)/I_{FT}$
$R = V_p$ AC line/I_{TSM}
The load may be placed on either side of the AC line.

Figure 11. Basic Driver Circuit

Triac Driver Circuit for Noisy Environments

When the transient rate of rise and amplitude are expected to exceed the power triacs and triac drivers maximum ratings a snubber circuit as shown in Figure 12 is recommended. Fast transients are slowed by the R–C snubber and excessive amplitudes are clipped by the Metal Oxide Varistor MOV.



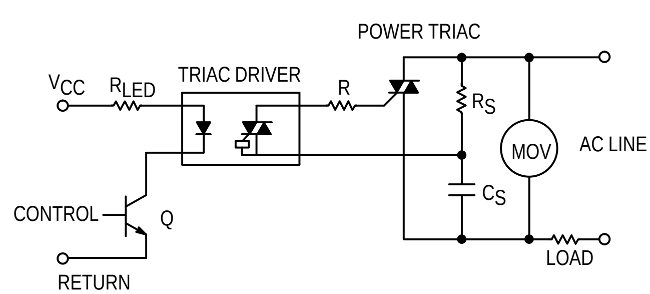
Traditional snubber configuration
Typical Snubber values R_S = 33 Ω, C_S = 0.01 µF
MOV (Metal Oxide Varistor) protects triac and driver from transient overvoltages $>V_{DRM}$ max

Figure 12. Triac Driver Circuit for Noisy Environments

Triac Driver Circuit for Extremely Noisy Environments

Noisy environments for this circuit are defined in the noise standards IEEE472, IEC255–4 and IEC801–4.

Industrial control applications, for example, do specify a maximum expected transient noise dv/dt and peak voltage which is superimposed onto the AC line voltage. Figure 13 shows a split snubber network which enhances the circuits noise immunity by protecting the triac driver with optimized efficiency.



Recommended snubber values R_S = 10 W, C_S = 0.033 mF

Figure 13. Triac Driver Circuit for Extremely Noisy Environments

APPLICATIONS GUIDE

Hot–Line Switching Application Circuit

Typical circuit for use when hot–line switching is required. In this circuit the "hot" side of the line is switched and the load connected to the cold or neutral side. The load may be connected to either the neutral or hot–line.

R_{in} is calculated so that I_F is equal to the rated I_{FT} of the part, 10 mA for the MOC3162, and 5.0 mA for the MOC3163. The 39 ohm resistor and 0.01 µF capacitor are for snubbing of the triac and may or may not be necessary depending upon the particular triac and load used.

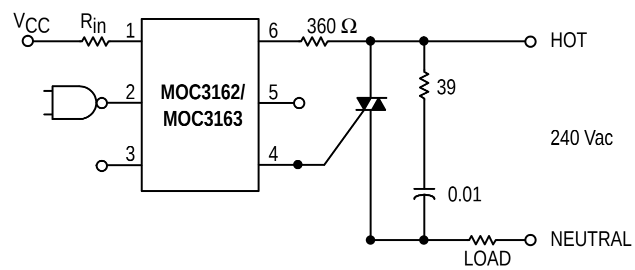


Figure 14. Hot–Line Switching Application Circuit

Inverse Parallel SCR Driver Circuit

Two inverse parallel SCR's are controlled by one triac driver with a minimum component count as shown in Figure 15. A snubber network and a MOV across the main terminals of the SCR's protects the semiconductors from transients on the AC line.

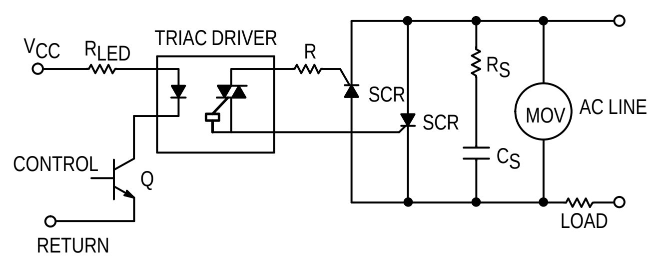
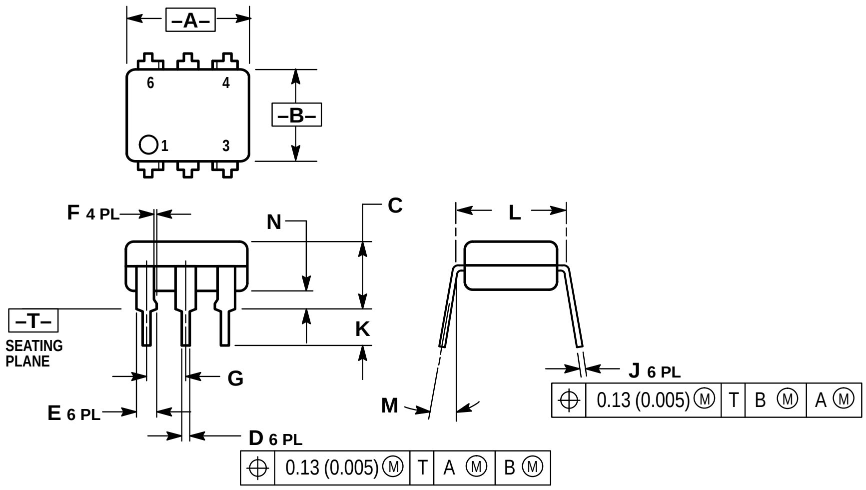


Figure 15. Inverse Parallel SCR Driver Circuit

PACKAGE DIMENSIONS

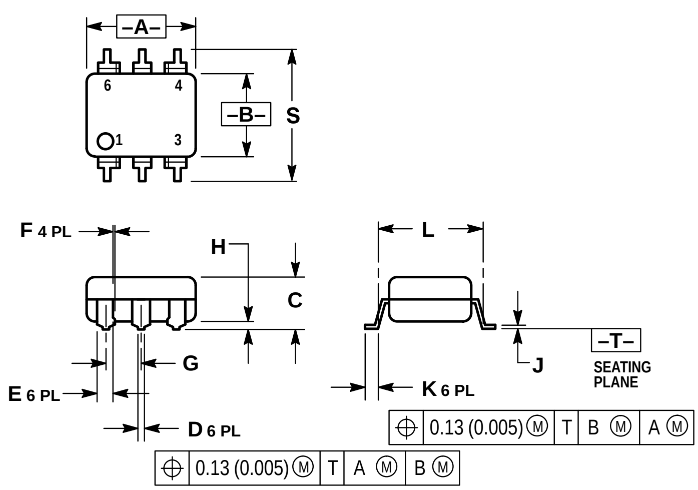


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.320	0.350	8.13	8.89
B	0.240	0.260	6.10	6.60
C	0.115	0.200	2.93	5.08
D	0.016	0.020	0.41	0.50
E	0.040	0.070	1.02	1.77
F	0.010	0.014	0.25	0.36
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.21	0.30
K	0.100	0.150	2.54	3.81
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.015	0.100	0.38	2.54

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. NC
4. MAIN TERMINAL
5. SUBSTRATE
6. MAIN TERMINAL

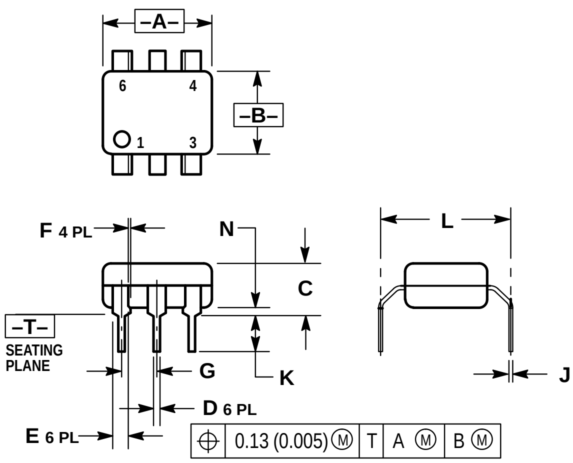
THRU HOLE



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.320	0.350	8.13	8.89
B	0.240	0.260	6.10	6.60
C	0.115	0.200	2.93	5.08
D	0.016	0.020	0.41	0.50
E	0.040	0.070	1.02	1.77
F	0.010	0.014	0.25	0.36
G	0.100 BSC		2.54 BSC	
H	0.020	0.025	0.51	0.63
J	0.008	0.012	0.20	0.30
K	0.006	0.035	0.16	0.88
L	0.320 BSC		8.13 BSC	
S	0.332	0.390	8.43	9.90

SURFACE MOUNT



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.320	0.350	8.13	8.89
B	0.240	0.260	6.10	6.60
C	0.115	0.200	2.93	5.08
D	0.016	0.020	0.41	0.50
E	0.040	0.070	1.02	1.77
F	0.010	0.014	0.25	0.36
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.21	0.30
K	0.100	0.150	2.54	3.81
L	0.400	0.425	10.16	10.80
N	0.015	0.040	0.38	1.02

0.4" LEAD SPACING

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.