PRODUCT SPECIFICATION

Model No. :	**JT60175-01**
Product Type :	**2.4" TFT+RTP 240(RGB)*320**
Customer No. :	

APPROVAL SIGNATURE

Customer : _____

Approved by :_____ (Signature)

Date :_____

Please return one copy with your official approval

JENSON SIGNATURES

Prepared by	Jin Wang
Checked by	Mayan Zhang
Approved by	Xinyong Li

Records of Revision

Rev.	Date	Page	Revise	Prepared by
00	2019.07.03	-	First issue	Jin Wang
01	2019.07.12	-	Updating viewing angle description	Jin Wang
02	2019.07.22	6~8	Updating interface definition; Add 4-line SPI application circuit.	Jin Wang

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1. Product Features

1.1 Introduction

This is a color active matrix Thin Film Transistor(TFT) Liquid Crystal Display(LCD) that uses TFT as a switching devise.This model is composed of a 2.4 inch transmissive type TFT-LCD panel and a Resistive Touch Panel(RTP) . The resolution of the panel is 240(RGB)*320 pixels and can display up to 262K color.

1.2 General Features

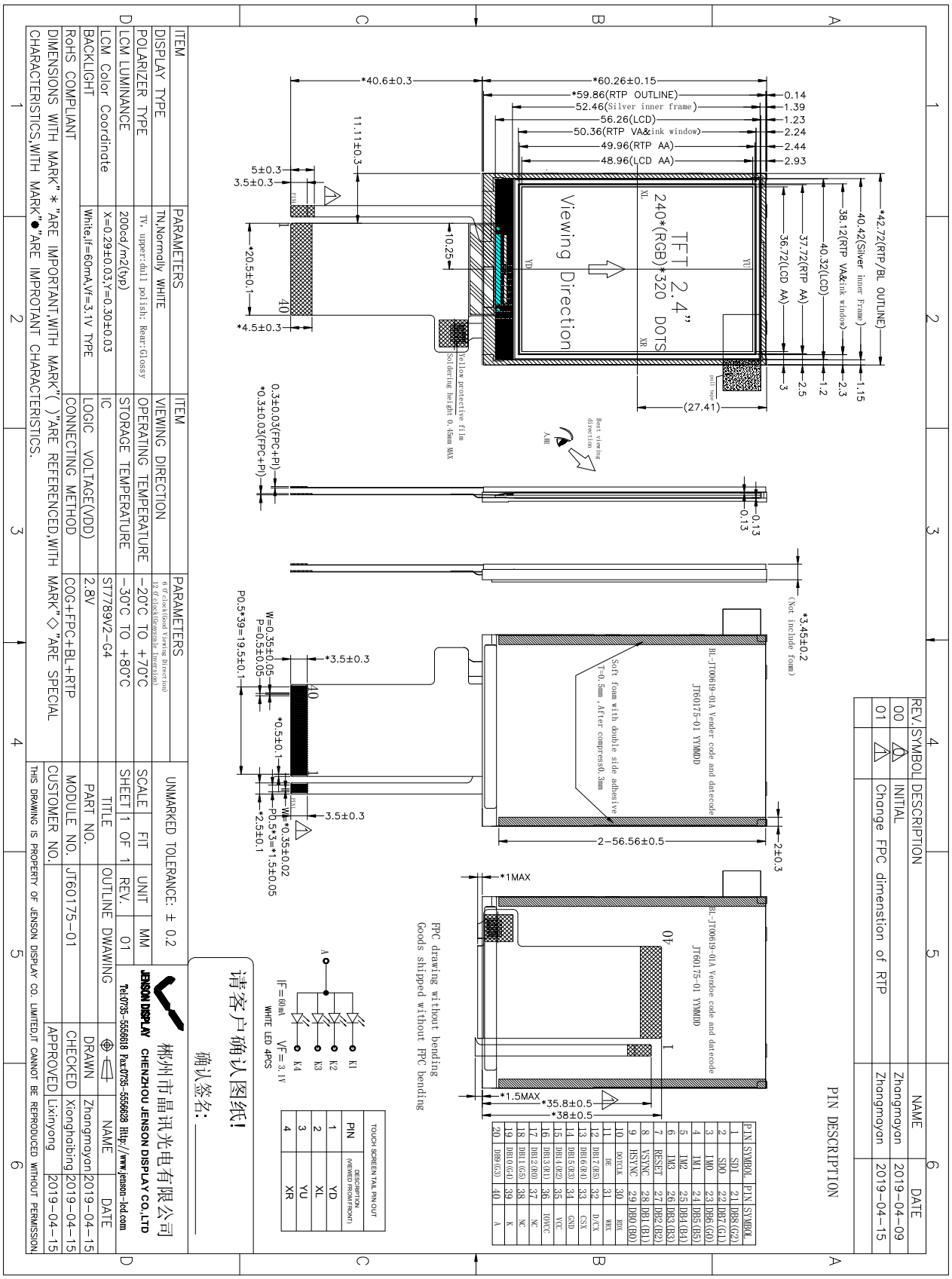
Parameter	Value	Unit
LCD Size	2.4	inch
Panel Type	TN TFT	-
Resolution	240(RGB)*320	pixel
Display Mode	Normally White, Transmissive	-
Display Colors	262K	-
Best Viewing Direction	6 O'clock	-
Contrast Ratio	250(Typ.)	-
Luminance of LCD Surface	200(Typ.)	cd/m2
Driver IC	ST7789V	-
Light sourse	4 White LEDs	-
Interface	SPI / MCU / RGB interface	-
Weight	TBD	g
Operating Temperature	-20℃~+70℃	℃
Storage Temperature	-30℃~+80℃	℃

2. Mechanical Specification

2.1 General Specification

Parameter	Value	Unit
LCM Module Size	42.72(H)×60.26(V)×3.45(T)	mm
Active Area(A.A.)	36.72(H)×48.96(V)	mm
Pixel Pitch	153(H)×153(V)	um
RTP Lens Dimension	42.72(H)×60.26(V)×1.15(T)	mm

2.2 Outline Dimension (Counter Drawing)



REV.	SYMBOL	DESCRIPTION	NAME	DATE
00	△	INITIAL	Zhangmoyan	2019-04-09
01	△	Change FPC dimenstion of RTP	Zhangmoyan	2019-04-15

PIN DESCRIPTION

PIN	SYMBOL	PIN	SYMBOL
1	SDI	21	DB8(G2)
2	SDO	22	DB7(G1)
3	IM0	23	DB6(G0)
4	IM1	24	DB5(B5)
5	IM2	25	DB4(B4)
6	IM3	26	DB3(B3)
7	RESET	27	DB2(B2)
8	VSYNC	28	DB1(B1)
9	HSYNC	29	DB0(B0)
10	DOTCLK	30	RDX
11	DE	31	WRX
12	DB17(R5)	32	D/CX
13	DB16(R4)	33	CSX
14	DB15(R3)	34	GND
15	DB14(R2)	35	VCC
16	DB13(R1)	36	IOVCC
17	DB12(R0)	37	NC
18	DB11(G5)	38	NC
19	DB10(G4)	39	K
20	DB9(G3)	40	A

TOUCH SCREEN TAIL PIN OUT

PIN	DESCRIPTION (VIEWED FROM FRONT)
1	YD
2	XL
3	YU
4	XR

ITEM	PARAMETERS	ITEM	PARAMETERS
DISPLAY TYPE	TN,Normally WHITE	VIEWING DIRECTION	6 O'clock(Good Viewing Direction) 12 O'clock(Grayscale Inversion)
POLARIZER TYPE	TN, upper:dull polish; Rear:Glossy	OPERATING TEMPERATURE	-20°C TO +70°C
LCM LUMINANCE	200cd/m2(typ)	STORAGE TEMPERATURE	-30°C TO +80°C
LCM Color Coordinate	X=0.29±0.03,Y=0.30±0.03	IC	ST7789V2-G4
BACKLIGHT	White,If=60mA,Vf=3.1V TYPE	LOGIC VOLTAGE(VDD)	2.8V
RoHS COMPLIANT		CONNECTING METHOD	COG+FPC+BL+RTP
DIMENSIONS WITH MARK"＊"ARE IMPORTANT,WITH MARK"( )"ARE REFERENCED,WITH MARK"◇"ARE SPECIAL CHARACTERISTICS,WITH MARK"●"ARE IMPROTANT CHARACTERISTICS.			

UNMARKED TOLERANCE: ± 0.2

SCALE	FIT	UNIT	MM
SHEET	1 OF 1	REV.	01
TITLE		OUTLINE DWAWING	
PART NO.		JT60175-01	
MODULE NO.			
CUSTOMER NO.			

	NAME	DATE
DRAWN	Zhangmoyan	2019-04-15
CHECKED	Xionghaibing	2019-04-15
APPROVED	Lixinyong	2019-04-15

JENSON DISPLAY CHENZHOU JENSON DISPLAY CO.,LTD
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郴州市晶讯光电有限公司

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3. Interface Assignment

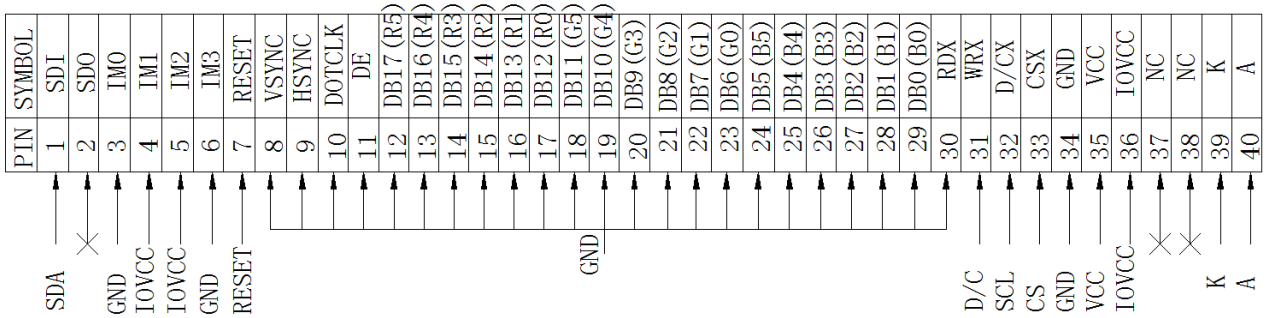
<table>
<tr><th>Pin NO.</th><th>Symbol</th><th>Description</th></tr>
<tr><td>1</td><td>SDI</td><td>-When IM3: Low, SPI interface input/output pin.
-When IM3: High, SPI interface input pin.
-The data is latched on the rising edge of the SCL signal.
-If not used, please fix this pin at VDDI or DGND level.</td></tr>
<tr><td>2</td><td>SDO</td><td>-SPI interface output pin.
-The data is output on the falling edge of the SCL signal.
-If not used, let this pin open.</td></tr>
<tr><td>3~6</td><td>IM0~IM3</td><td>
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU Interface Mode</th><th>Data pin</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>80-8bit parallel I/F</td><td>DB[7:0]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>80-16bit parallel I/F</td><td>DB[15:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>80-9bit parallel I/F</td><td>DB[8:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>80-18bit parallel I/F</td><td>DB[17:0],</td></tr>
<tr><td rowspan="2">0</td><td rowspan="2">1</td><td rowspan="2">0</td><td rowspan="2">1</td><td>3-line 9bit serial I/F</td><td>SDA: in/out</td></tr>
<tr><td>2 data lane serial I/F</td><td>SDA: in/out
WRX: in</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>4-line 8bit serial I/F</td><td>SDA: in/out</td></tr>
</table>
</td></tr>
<tr><td>7</td><td>RESET</td><td>Reset pin.</td></tr>
<tr><td>8</td><td>VSYNC</td><td>-Vertical (Frame) synchronizing input signal for RGB interface operation.
-If not used, please fix to the VDDI or DGND.</td></tr>
<tr><td>9</td><td>HSYNC</td><td>-Horizontal (Line) synchronizing input signal for RGB interface operation.
- If not used, please fix to VDDI or DGND.</td></tr>
<tr><td>10</td><td>DOTCLK</td><td>-Dot clock signal for RGB interface operation.
-If not used, please fix this pin at VDDI or DGND.</td></tr>
<tr><td>11</td><td>DE</td><td>-Data enable signal for RGB interface operation.
-If not used, please fix this pin at VDDI or DGND.</td></tr>
<tr><td>12~29</td><td>DB17~DB0</td><td>Display data bus.
-If not used, please fix this pin at VDDI or DGND.</td></tr>
<tr><td>30</td><td>RDX</td><td>-Read enable in 8080 MCU parallel interface.
-If not used, please fix this pin at VDDI or DGND.</td></tr>
<tr><td>31</td><td>WRX</td><td>-Write enable in MCU parallel interface.
- Display data/command selection pin in 4-line serial interface.
- Second Data lane in 2 data lane serial interface.
-If not used, please fix this pin at VDDI or DGND</td></tr>
<tr><td>32</td><td>D/CX</td><td>-Display data/command selection pin in parallel interface.
-This pin is used to be serial interface clock.
DCX=’1’: display data or parameter.
DCX=’0’: command data.
-If not used, please fix this pin at VDDI or DGND.</td></tr>
</table>

33	CSX	Chip select pin
34	GND	Ground
35	VCC	Analog power Supply 2.8V
36	IOVCC	Power Supply for I/O System.
37~38	NC	No connection
39	K	Backlight cathode
40	A	Backlight anode

4. Electrical Specification

4.1 Application Circuit

4.1.1 SPI-4Line Application Circuit



4.2 Absolute Maximum Ratings

Item	Symbol	Min	Max	Unit	Note
Digital Voltage	IOVCC	-0.3	+4.6	V	-
Analog Voltage	VCC	-0.3	+4.6	V	-
Gate Driver High Voltage	V_{GH}	-0.3	18	V	-
Gate Driver Low Voltage	V_{GL}	0.3	-18	V	-
Operation Temperature	T_{op}	-20	70	°C	-
Storage Temperature	T_{ST}	-30	80	°C	-

Note 1: The absolute maximum rating of this product are not allowed to be exceeded at any times. Should a module be used with any of the absolute maximum ratings exceeded, the characteristics of the module may not be recovered, or in an extreme case, the module may be permanently destroyed.

4.3 Typical Operation Conditions

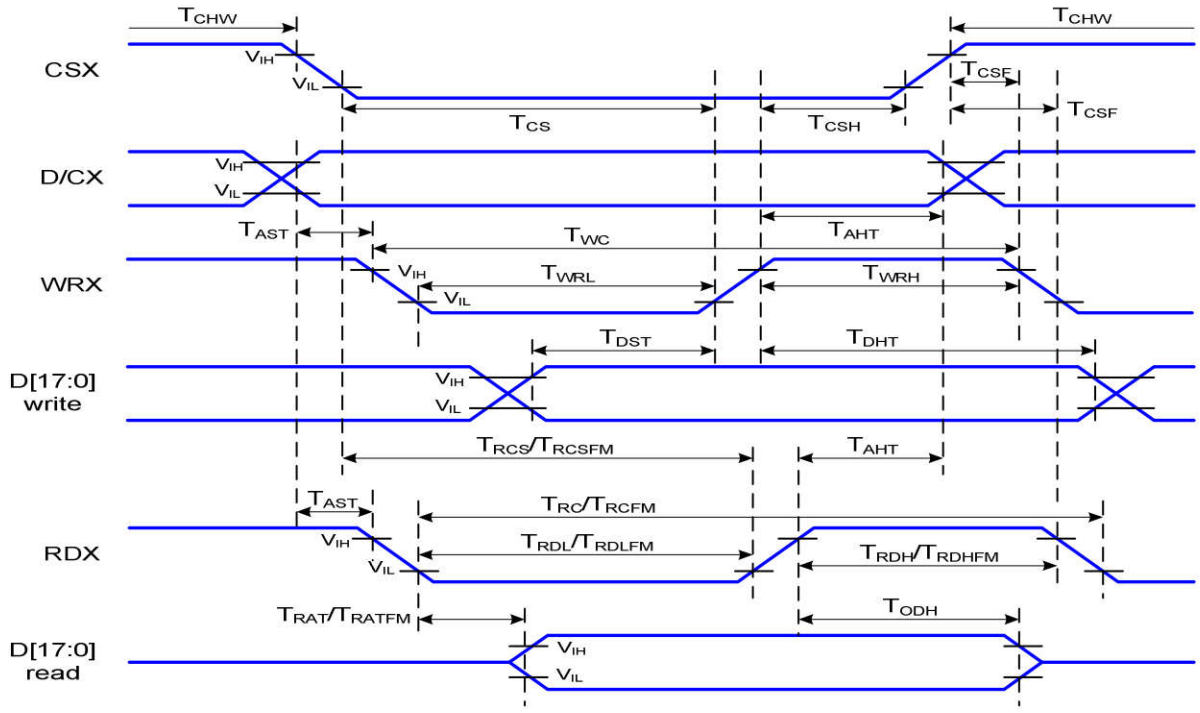
4.3.1 DC Characteristics

Item	Symbol	Min	Typ	Max	Unit	Note
Digital Voltage	IOVCC	1.65	1.8	3.3	V	-
Analog Voltage	VCC	2.4	2.75	3.3	V	-
Gate Driver High Voltage	V_{GH}	12.2	-	14.97	V	-
Gate Driver Low Voltage	V_{GL}	-12.5	-	-7.16	V	-
Input signal voltage	V_{COM}	-	vss	-	V	-
Input logic high voltage	V_{IH}	0.7IOVCC	-	IOVCC	V	-
Input logic low voltage	V_{IL}	-0.3	-	0.3IOVCC	V	-
Output logic high voltage	V_{OH}	0.8IOVCC	-	IOVCC	V	-
Output logic low voltage	V_{OL}	0	-	0.2IOVCC	V	-

Note 1: V_{GH} is TFT gate operating voltage.
Note 2: V_{GL} is FTF gate operating voltage.
The storage structure of this mode is Cst (Storage on common)

4.3.2 AC Characteristics

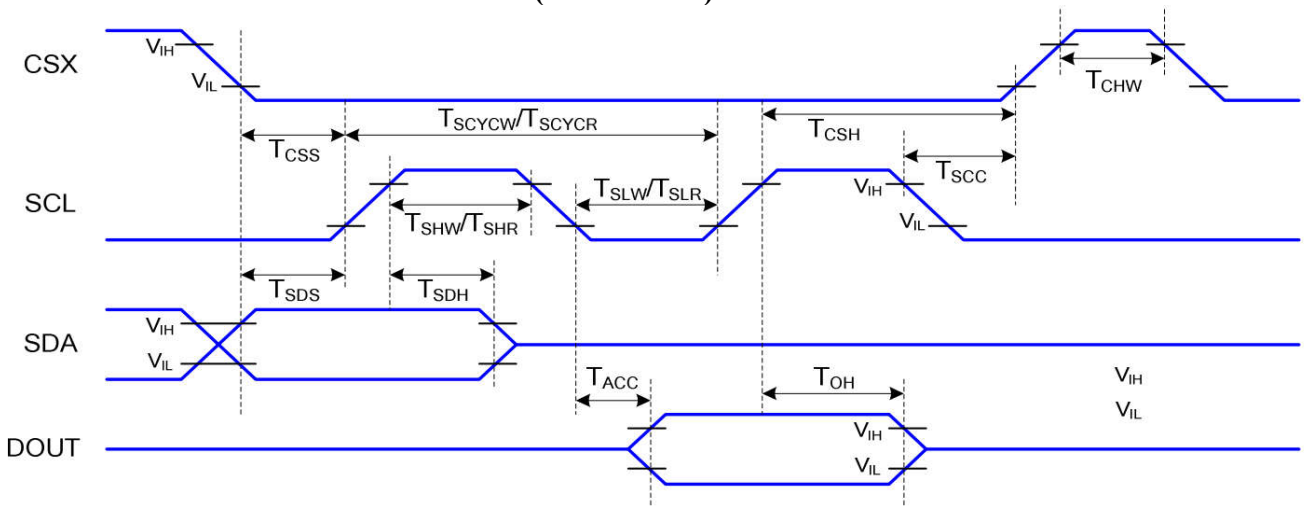
4.3.2.1 8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta= -30 to 70 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	0		ns	-
	T_{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip select "H" pulse width	0		ns	-
	T_{CS}	Chip select setup time (Write)	15		ns	
	T_{RCS}	Chip select setup time (Read ID)	45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
WRX	T_{WC}	Write cycle	66		ns	
	T_{WRH}	Control pulse "H" duration	15		ns	
	T_{WRL}	Control pulse "L" duration	15		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse "H" duration (ID)	90		ns	
	T_{RDL}	Control pulse "L" duration (ID)	45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse "H" duration (FM)	90		ns	
	T_{RDLFM}	Control pulse "L" duration (FM)	355		ns	
D[17:0]	T_{DST}	Data setup time	10		ns	For CL=30pF
	T_{DHT}	Data hold time	10		ns	
	T_{RAT}	Read access time (ID)		40	ns	
	T_{RATFM}	Read access time (FM)		340	ns	
	T_{ODH}	Output disable time	20	80	ns	

4.3.2.2 Serial Interface Characteristics (3-line serial):



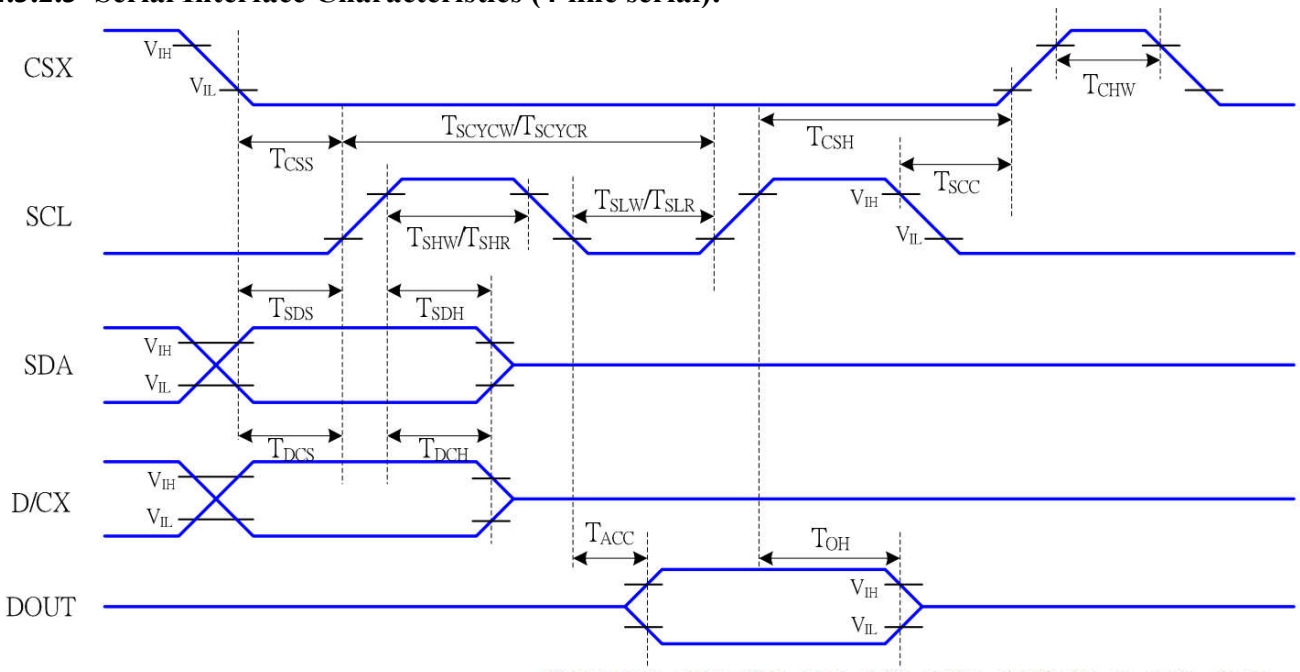
VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 ℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

Table 5 3-line serial Interface Characteristics

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

4.3.2.3 Serial Interface Characteristics (4-line serial):



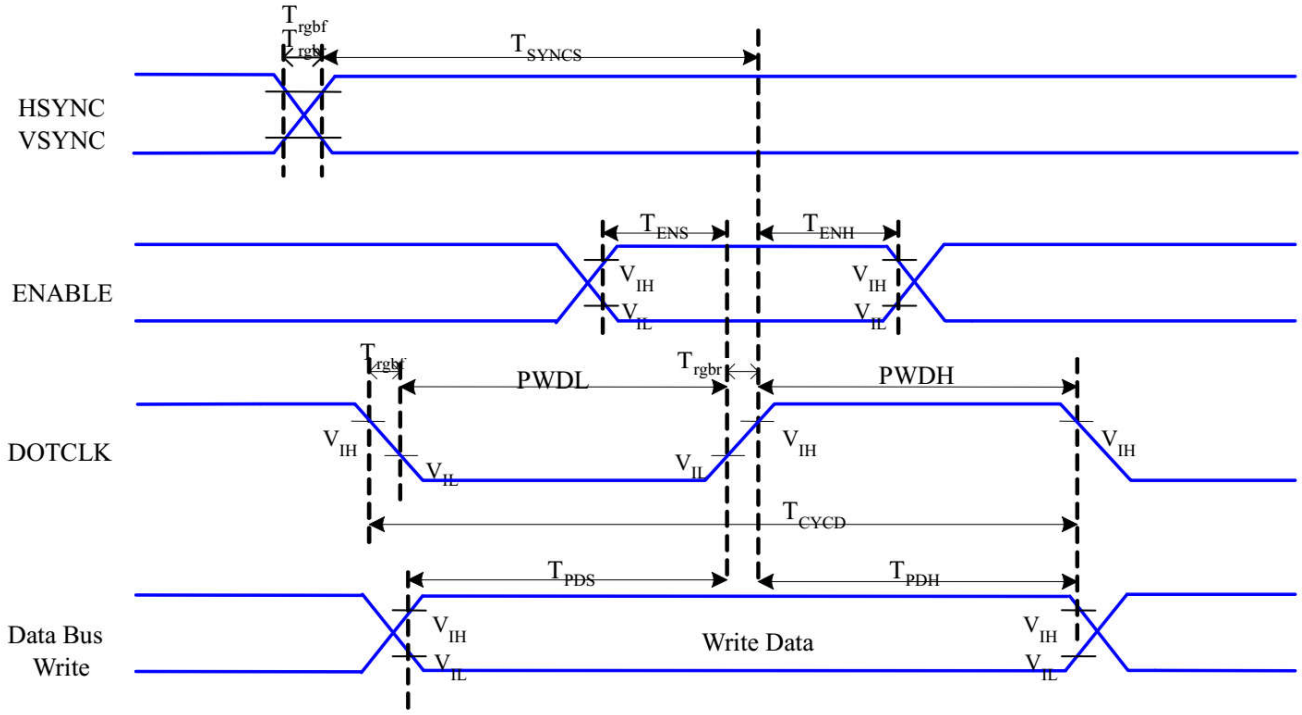
VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66		ns	-write command & data ram
	T_{SHW}	SCL "H" pulse width (Write)	15		ns	
	T_{SLW}	SCL "L" pulse width (Write)	15		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	10		ns	
	T_{DCH}	D/CX hold time	10		ns	
SDA (DIN)	T_{SDS}	Data setup time	10		ns	
	T_{SDH}	Data hold time	10		ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

Table 6 4-line serial Interface Characteristics

Note : The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

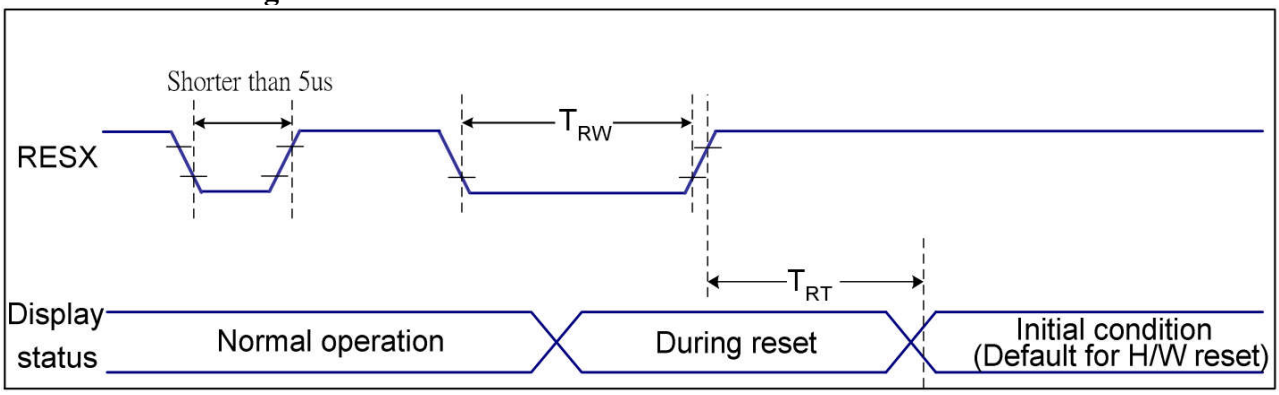
4.3.2.4 RGB Interface Characteristics:



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 ~ 70 ℃

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	T_{SYNCS}	VSYNC, HSYNC Setup Time	30	-	ns	
ENABLE	T_{ENS}	Enable Setup Time	25	-	ns	
	T_{ENH}	Enable Hold Time	25	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	60	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	60	-	ns	
	T_{CYCD}	DOTCLK Cycle Time	120	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall time	-	20	ns	
DB	T_{PDS}	PD Data Setup Time	50	-	ns	
	T_{PDH}	PD Data Hold Time	50	-	ns	

4.3.2.5 Reset Timing



VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=-30 ~ 70 ℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Notes:

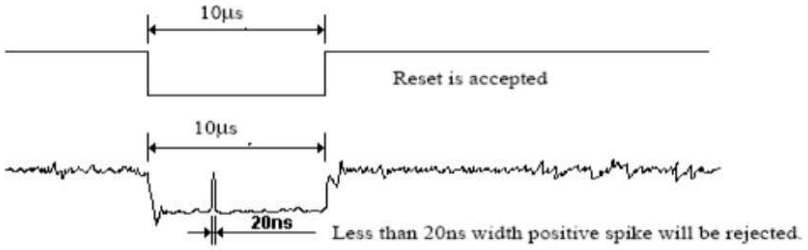
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

4.3.3 Power ON/OFF Sequence

4.3.3.1 Power ON Sequence

VDDI and VDD can be applied in any order.

VDD and VDDI can be power down in any order.

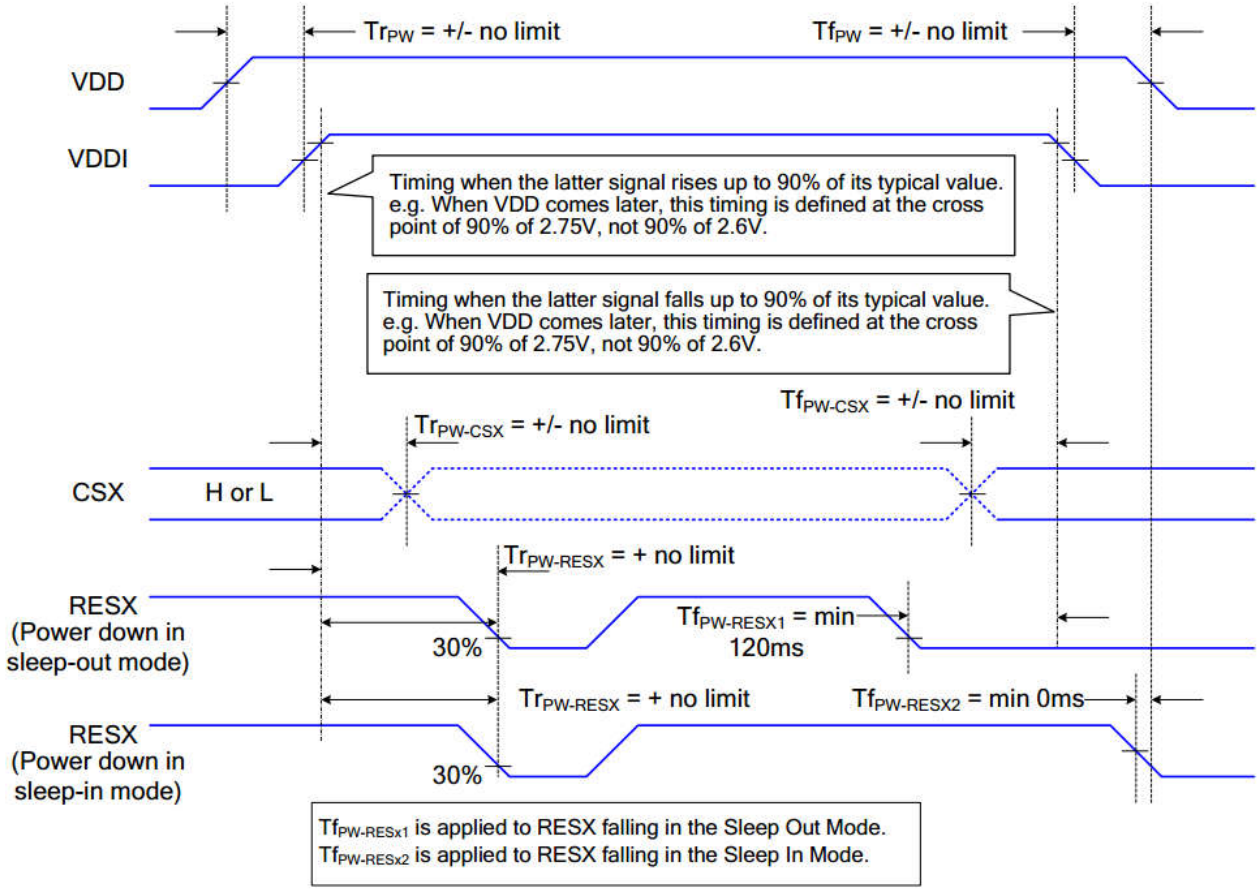
During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDD can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Note 1: There will be no damage to the display module if the power sequences are not met.
Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
Note 4: If RESX line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below



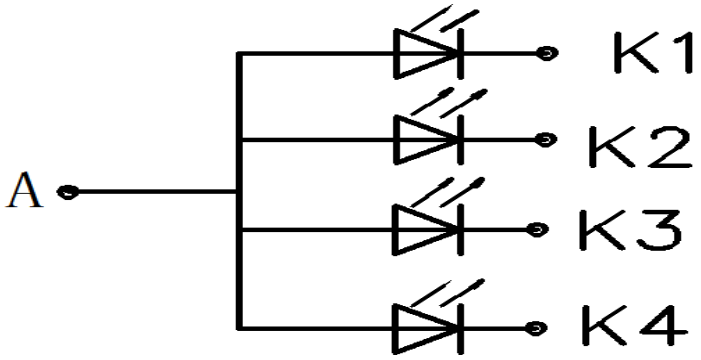
4.3.3.2 Power OFF Sequence

The uncontrolled power-off means a situation which removed a battery without the controlled power off sequence. It will neither damage the module or the host interface.

If uncontrolled power-off happened, the display will go blank and there will not any visible effect on the display (blank display) and remains blank until "Power On Sequence" powers it up.

4.3.4 Backlight Specification

4.3.4.1 Backlight Circuit



4.3.4.2 Absolute Ratings

Parameter	Symbol	Specifications	Unit
Power Dissipation	Pd	256	mW
Forward Current(Single Chip)	Ifm	20	mA
Reverse Voltage	Vr	5	V

4.3.4.3 Electrical Characteristics

Item	Symbol	Min	Typ	Max	Unit	Conditions	Note
Voltage for backlight	V_L	3.0	3.2	3.4	V	IF=80mA	Note 1
Current for backlight(Single Chip)	I_L	-	20	-	mA	Constant	-
Luminance(with LCD)	L	-	300	-	Cd/m2	I_L=80mA	-
LED life time	-	-	30000	-	Hr	-	Note 2

Note 1:The LED Supply Voltage is defined by the number of LED at Ta=25°C and I_L=20mA.
Note 2:The "LED life time" is defined as the module brightness decrease to 50% original brightness at Ta=25°C and I_L=20mA. The LED lifetime could be decreased if operating I_L is large than 20mA.

5. Touch Panel Specification

5.1 General Specification

No.	Item		Specification	Unit	Remark
1	RTP Sise		2.4	inch	-
2	Resolution		-	pixel	-
3	Outline dimension		42.72x59.86x1.15	mm	Note 1
4	Viewing Area		38.12x50.36	mm	-
5	Surface Hardness		≥3H	-	-
6	Transparency		78% ±3	-	Note 2
7	Driver IC		-	-	-
8	Interface		-	-	-
9	Support Points		single-point	-	-
10	Rate		-	Hz	-
11	Power Supply		-	V	-
12	Current Consumption	Operating	-	mA	Note 3
13		Monitor	-	mA	
14		Sleep mode	-	uA	
15	Operating Temperature		-20~70	℃	-
16	Storage Temperature		-30~80	℃	-
17	ESD	Air	±8	kV	Note 4
		Contact	±4	kV	

Note 1:The thickness Included foam.
Note 2:Test at wave length 550nm.
Note 4:Test on lens surface.

6. Optical Characteristics(T=25℃)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Contrast Ratio		CR	θ=0° , ϕ=0°	-	250	-	-	Note1
Surface Luminance		L	θ=0° , ϕ=0°	150	200	-	Cd/m2	Note2
Luminance Uniformity		U_L	θ=0° , ϕ=0°	75	80	-	%	Note3
Response Time		$T_{r+}T_f$	θ=0° , ϕ=0°	-	30	-	ms	Note4
Color Chromaticity (CIE1931)	Red	Rx	VDD=2.8V IOVCC=1.8V I_L =40mA θ=0° , ϕ=0°	-	0.612	-	-	Note5
		Ry		-	0.329	-		
	Green	Gx		-	0.299	-		
		Gy		-	0.567	-		
	Blue	Bx		-	0.144	-		
		By		-	0.110	-		
	White	Wx		-	0.308	-		
		Wy		-	0.325	-		
Color Gamut		NTSC	CIE1931	-	55	-	%	Note5
Viewing Angle	ϕ=90°	θ_T	Cr≥10	-	60	-	Degree	Note6
	ϕ=270°	θ_B		-	50	-	Degree	
	ϕ=180°	θ_L		-	60	-	Degree	
	ϕ=0°	θ_R		-	60	-	Degree	

Note1.Definition of contrast ratio
Contrast ratio(Cr) is defined mathematically by the following formula.
For more information see FIG.2.

$$\text{Contrast ratio} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Measured at the center area of the LCD

Note2.Definition of surface luminance
Surface luminance is the luminance with all pixels displaying white.
For more information see FIG.2.
Lv = Average Surface Luminance with all white pixels(P1,P2,P3, ...,Pn)

Note3.Definition of luminance uniformity
The luminance uniformity in surface luminance is determined by measuring luminance at each test position 1 through n, and then dividing the maximum luminance of n points luminance by minimum luminance of n points luminance.For more information see FIG.2.

$$Yu = \frac{\text{Minimum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}{\text{Maximum surface luminance with all white pixels (P1,P2,P3,.....,Pn)}}$$

Note4. Definition of response time
The response time is defined as the LCD optical switching time interval between "White" state and "Black"state.Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.
For additional information see FIG1.

Note5. Definition of color chromaticity (CIE1931)
CIE (x,y) chromaticity,The x,y value is determined by screen active area center position P5.For more information see FIG.2.

Note6. Definition of viewing angle
Viewing angle is the angle at which the contrast ratio is greater than 10. angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface.
For more information see FIG.3.
For viewing angle and response time testing, the testing data is base on Autronic-Melchers's ConoScope or DMS series Instruments or compatible. For contrast ratio, Surface Luminance, Luminance uniformity and CIE,the testing data is base on TOPCON's BM-5or BM-7 photo detector or compatible.
Note: For TFT module, Gray scale reverse occurs in the direction of panel viewing angle.

FIG.1. The definition of response Time

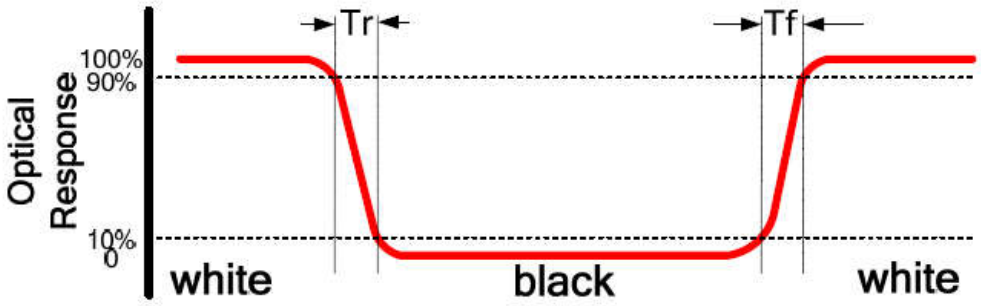


FIG.2. Measuring method for contrast ratio, surface luminance, luminance uniformity, CIE (x,y) chromaticity

Size : S≤5"(see Figure a)
A : 5 mm B : 5 mm
H,V : Active area
Light spot size ∅=5mm(BM-5) or ∅=7.7mm (BM-7)50cm distance or compatible distance from the LCD surface to detector lens.
test spot position : see Figure a.
measurement instrument : TOPCON's luminance meter BM-5 or BM-7 or compatible (see Figure c).

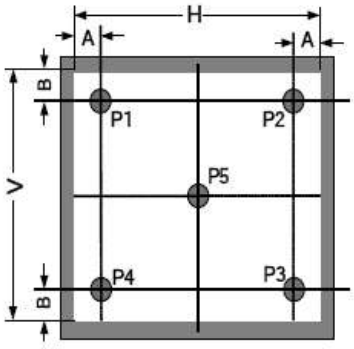


Figure a

Size : 5"<S≤12.3"(see Figure b)
H,V : Active area
Light spot size ∅=5mm(BM-5) or ∅=7.7mm (BM-7)50cm distance or compatible distance from the LCD surface to detector lens.
test spot position : see Figure b.
measurement instrument : TOPCON's luminance meter BM-5 or BM-7 or compatible (see Figure c).

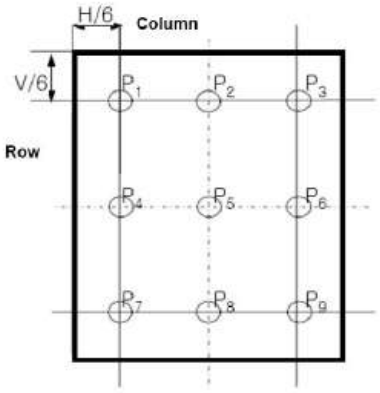


Figure b

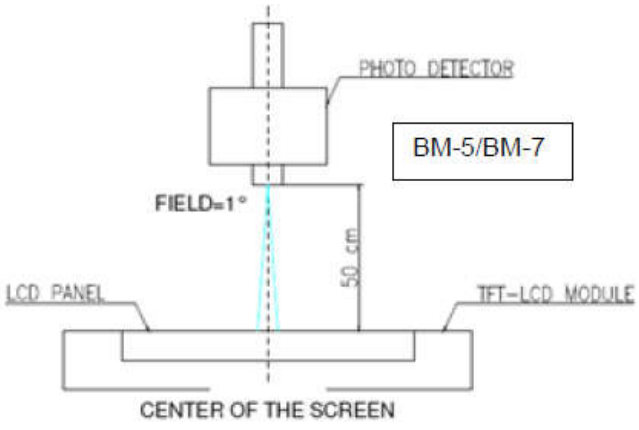
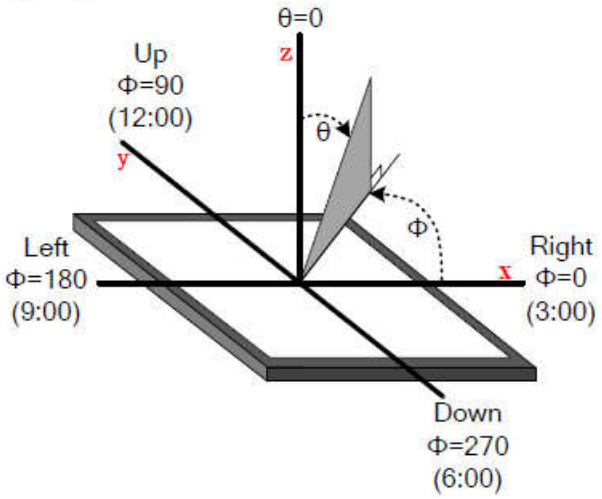


Figure c

FIG.3. The definition of viewing angle

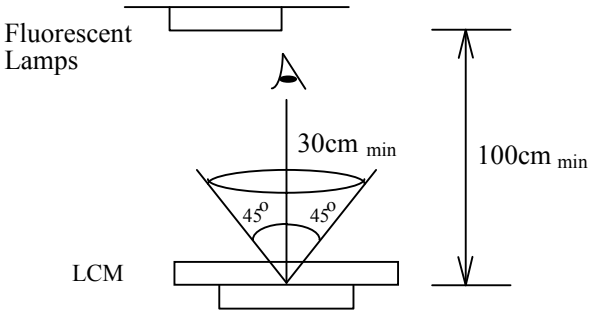


7. Quality Specifications

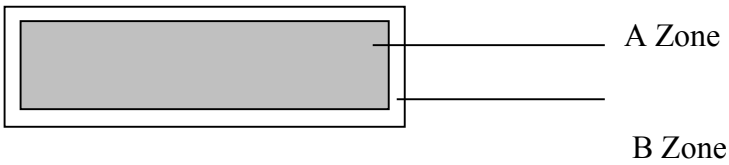
7.1 Condition for product appearance inspection

Manner of appearance test: The inspection should be performed in using 20W x 2 fluorescent lamps. Distance between LCM and fluorescent lamps should be 100 cm or more. Distance between LCM and inspector eyes should be 30 cm or more.

Viewing direction for inspection is 45° from vertical against LCM.



Definition of zone:



A Zone: Active display area (minimum viewing area).
B Zone: Non-active display area (outside viewing area).

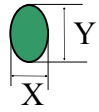
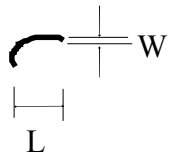
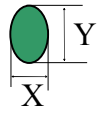
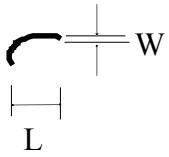
7.2 Funcation Inspection

Inspecting items	Inspecting criterion	Classifiation of defects
All functional defects	No display Display abnormally Missing vertical,horizontal segment Short circuit Back-light no lighting or abnormal lighting,and abnormally lighting. Obvious striation Current consumption exceeds limit	Major
Missing	Missing component	
Outline dimension	Referred to counter drawing	

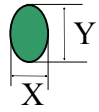
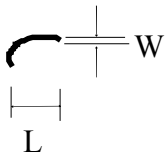
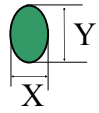
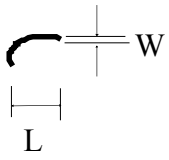
7.3 TFT - LCD Pixel Inspection

Items	Judgment striation		
	S≤5.0inch	5.0＜S≤7.0inch	7.0＜S≤12.1inch
Bad dot-bright dot(R、G、B)	1	2	3
Two adjacent bright point	0	1	2
Three or more adjacent bright point	0	0	0
Total points for bad dot-bright dot	1	3	5
Bad dot-dark dot	2	4	5
Two adjacent bright point	1	2	3
Three or more adjacent bright point	0	1	1
Total points for bad dot-dark dot	3	7	9

7.4 TFT Module Dot And Line Inspection

Item	Judgment criterion					Figure
	LCD Size		S≤5.0 inch	5.0<S≤7.0 inch	7.0<S≤12.1 inch	
Dot inspection	D≤0.1		allowed	allowed	allowed	 D=(X+Y)/2
	0.1<D≤0.2		4	allowed	allowed	
	0.3<D≤0.3		0	5	6	
	0.3<D≤0.5		0	0	6	
	D>0.5		0	0	0	
	The distance between two defect dot:DS≥5mm					
Line inspection	L(mm)	W(mm)	Judgment criterion			
	disregard	W≤0.05	allowed	allowed	allowed	
	L≤5	0.05<W≤0.1	4	5	7	
	L>5	W>0.1	0	0	0	
Concave point and air bubble for polarizer	LCD size(mm)		Judgment criterion			 D=(X+Y)/2
	D≤0.3		allowed	allowed	allowed	
	0.3<D≤1.0		3	4	5	
	01.0<D≤1.5		1	2	3	
	D>1.5		0	0	0	
Fold mark、linear scar for polarizer	L(mm)	W(mm)	Judgment criterion			
	disregard	W≤0.05	allowed	allowed	allowed	
	1<L≤5	0.05<W≤0.2	3	4	5	
	L>5	W>0.2	0	0	0	

7.5 TFT +PCAP Module Dot And Line Inspection

Item	Judgment criterion				Figure
	TFT Module Size	S≤5.0 inch	5.0<S≤7.0 inch	7.0<S≤12.1 inch	
Dot inspection	D≤0.1	allowed	allowed	allowed	 D=(X+Y)/2
	0.1<D≤0.2	6	allowed	allowed	
	0.3<D≤0.3	0	8	9	
	0.3<D≤0.5	0	0	6	
	D>0.5	0	0	0	
	The distance between two defect dot:DS≥5mm				
Line inspection	L(mm)	W(mm)	Judgment criterion		
	disregard	W≤0.05	allowed	allowed	allowed
	L≤5	0.05<W≤0.1	6	7	8
	L>5	W>0.1	0	0	0
	The distance between two defect dot:DS≥20mm				
Concave point and air bubble for polarizer	LCD size(mm)		Judgment criterion		 D=(X+Y)/2
	D≤0.3		allowed	allowed	allowed
	0.3<D≤1.0		5	6	7
	1.0<D≤1.5		3	4	5
	D>1.5		0	0	0
Fold mark、linear scar for polarize	L(mm)	W(mm)	Judgment criterion		
	disregard	W≤0.05	allowed	allowed	allowed
	1<L≤5	0.05<W≤0.2	3	4	5
	L>5	W>0.2	0	0	0

7.6 Module Cosmetic Criteria

Item	Judgment Criterion
Difference in Spec	None allowed
Pattern peeling	No substrate pattern peeling and floating
Soldering defects	No soldering missing No soldering bridge No cold soldering
Stain	No stain to spoil cosmetic badly
Plate discoloring	No plate fading, rusting and discoloring
Newton ring	Referring to limited sample
Mura	Invisible with 5%ND,allowed
Light leaks	Referring to limited sample

8. Reliability Test

Test Item	Conditions		Criteria
	Temperature	Time (hrs)	
High temp. Storage	+80°C	240	/
High temp. Operating	+70°C	240	/
Low temp. Storage	-30°C	240	/
Low temp. Operating	-20°C	240	/
High Temperature &High Humidity Operation	60°C/ 90%RH	240	/
Thermal shock , Storage	-40°C ← 25°C →+85°C (30 min ← 3 min → 30min)	20cycles	/
Package Drop Test	Heigh:60cm 1 corner,3edges,6surfaces	/	/

Note1: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.
Note2: Before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.

9. PRECAUTIONS

9.1 Handling

9.1.1 Polarizer Cleaning, Petroleum ether (or N-hexane) is recommended for cleaning the front/rear polarizers and reflectors, acetone, toluene and ethanol are not allowed to avoid damaging the surface.
9.1.2 Body grounding, must wear Anti-ESD wrist strap while pick up LCDs.
9.1.3 FPC Soldering, less than 300℃/3S, solder must be grounding on grounding bench.
9.1.4 If use electric Screwdriver to do assembly, screwdriver must be grounding.

9.2 Storage

9.2.1 Keep in a sealed polyethylene bag.
9.2.2 Keep in a dark place.
9.2.3 Keep in temperature between 0 ℃ and 35 ℃.
NOT allowed at 70 ℃ for more than 160 Hours, or at -20 ℃ for more than 48 Hrs.

9.3 Safety

If liquid crystal leak out of a damaged glass cell, **DO NOT** put it in your mouth or touch eyes, if the liquid crystal touch your skin or clothes, please wash it off immediately using soap and water.

10. Limited Warranty

Unless otherwise agreed between JENSON and customer,JENSON will replace or repair any of its LCD modules which are found to be functionally defective when inspected in accordance with JENSON LCD acceptance standards (copies available upon request) for a period of one year from date of shipments. Cosmetic/visual defects over specs must be returned to JENSON within 30 days of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of JENSON limited to repair and/or replacement on the terms set forth above.JENSON shall not be responsible for any subsequent or consequential events.

10.1 RETURNING LCM UNDER WARRANTY – TERMS AND CONDITIONS

10.1.1 No warranty can be granted if the precautions stated above have been disregarded. The typical examples of violations are :
- Broken LCD glass.
- Circuit modified in any way, including addition of components.

10.1.2 Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects. Any connectors or cable installed by the customer must be removed completely without damaging the PCB’ s eyelet, conductors and terminals.