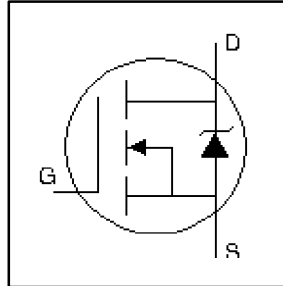


# HEXFET<sup>®</sup> Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- For Automatic Insertion
- End Stackable
- Fast Switching
- Ease of paralleling
- Simple Drive Requirements

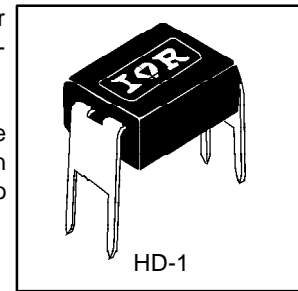


$V_{DSS} = 400V$
$R_{DS(on)} = 1.8\Omega$
$I_D = 0.49A$

## Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The 4-pin DIP package is a low-cost machine-insertable case style which can be stacked in multiple combinations on standard 0.1 inch pin centers. The dual drain serves as a thermal link to the mounting surface for power dissipation levels up to 1 watt.



## Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	0.49	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	0.31	
$I_{DM}$	Pulsed Drain Current ①	3.9	
$P_D @ T_C = 25^\circ C$	Power Dissipation	1.0	W
	Linear Derating Factor	0.0083	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy ②	48	mJ
$I_{AR}$	Avalanche Current ①	0.49	A
$E_{AR}$	Repetitive Avalanche Energy ①	0.10	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.0	V/ns
$T_J$	Operating Junction and	-55 to + 150	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

## Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient	—	—	120	°C/W

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	400	—	—	V	$V_{GS} = 0V, I_D = 250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.51	—	V/°C	Reference to $25^\circ\text{C}$ , $I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	1.8	$\Omega$	$V_{GS} = 10.0V, I_D = 0.21A$ ④
		—	—	—		$V_{GS} = V, I_D = A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
$g_{fs}$	Forward Transconductance	1.7	—	—	S	$V_{DS} = 50V, I_D = 1.2A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25	$\mu\text{A}$	$V_{DS} = 400V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 320V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
$Q_g$	Total Gate Charge	—	—	20	nC	$I_D = 2.0A$
$Q_{gs}$	Gate-to-Source Charge	—	—	3.3		$V_{DS} = 320V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	11		$V_{GS} = 10V$ , See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	10	—		$V_{DD} = 200V$
$t_r$	Rise Time	—	14	—	ns	$I_D = 3.3A$
$t_{d(off)}$	Turn-Off Delay Time	—	30	—		$R_G = 18\Omega$
$t_f$	Fall Time	—	13	—		$R_D = 56\Omega$ , See Fig. 10 ④
$L_D$	Internal Drain Inductance	—	4.0	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	6.0	—		
$C_{iss}$	Input Capacitance	—	410	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	120	—		$V_{DS} = 25V$
$C_{riss}$	Reverse Transfer Capacitance	—	47	—		$f = 1.0\text{MHz}$ , See Fig. 5



## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	0.49	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	3.9		
$V_{SD}$	Diode Forward Voltage	—	—	1.6	V	$T_J = 25^\circ\text{C}, I_S = 0.49A, V_{GS} = 0V$ ②
$t_{rr}$	Reverse Recovery Time	—	270	600	ns	$T_J = 25^\circ\text{C}, I_F = 3.3A$
$Q_{rr}$	Reverse Recovery Charge	—	1.4	3.0	$\mu\text{C}$	$di/dt = 100A/\mu\text{s}$ ②
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				

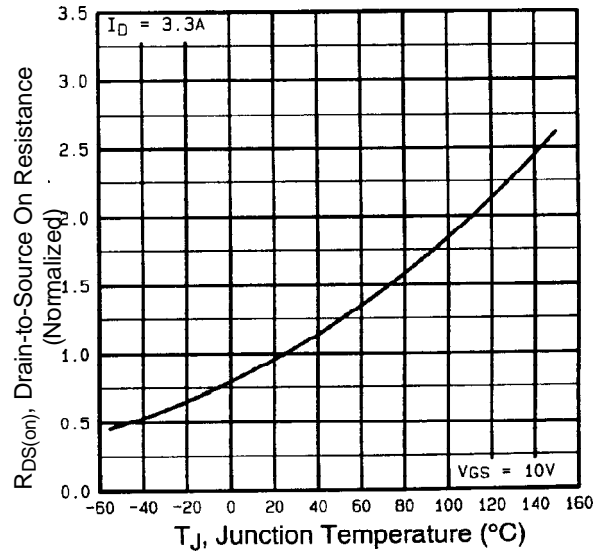
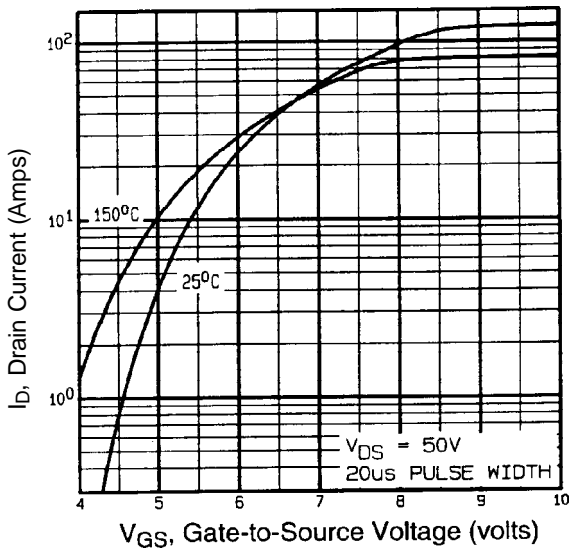
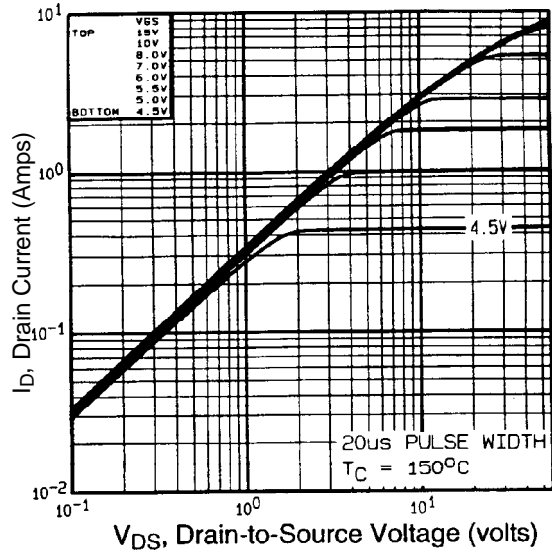
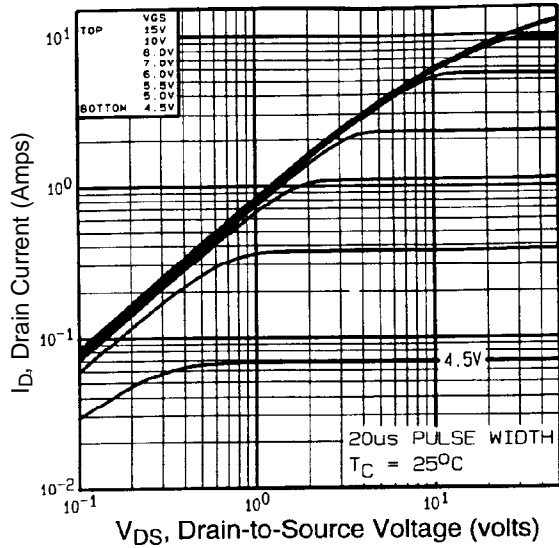
### Notes:

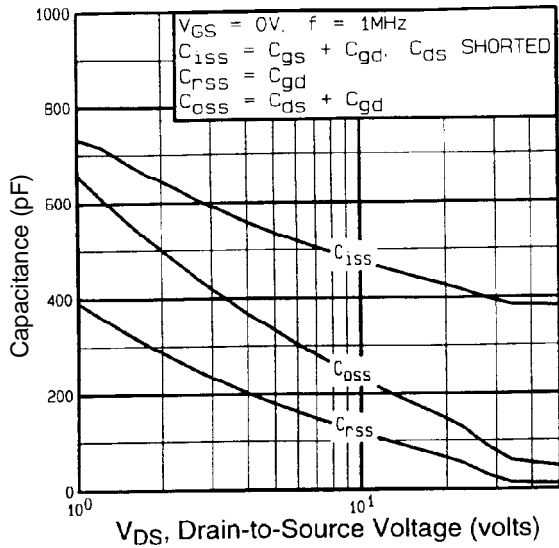
① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )

③  $I_{SD} \leq 2.0A, di/dt \leq 40A/\mu\text{s}, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$

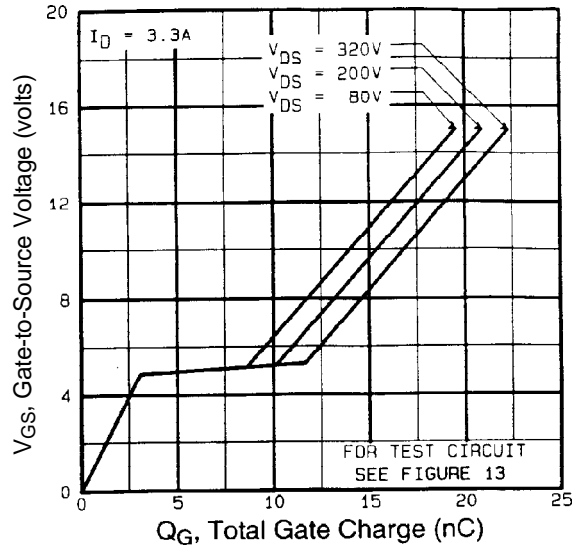
②  $V_{DD} = 50V$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 21\text{mH}$ ,  $R_G = 25\Omega, I_{AS} = 2.0A$ . (See Figure 12)

④ Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

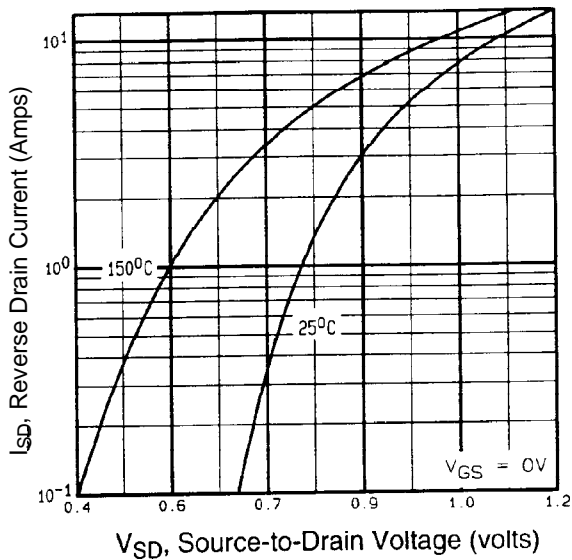




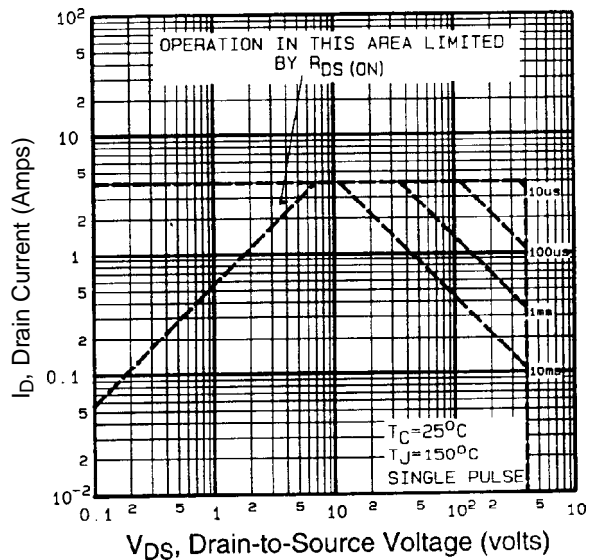
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



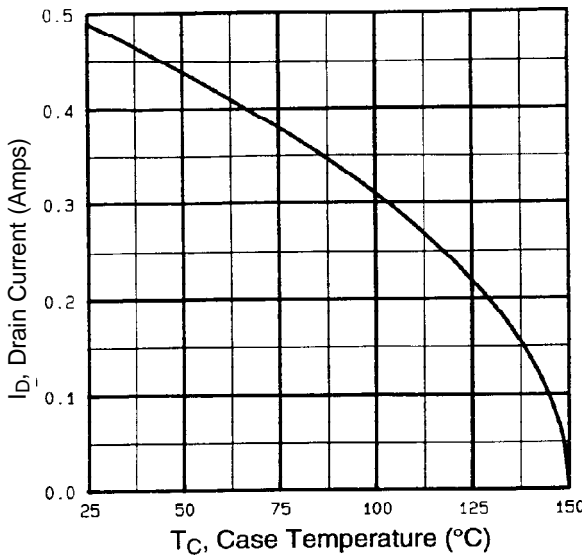
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



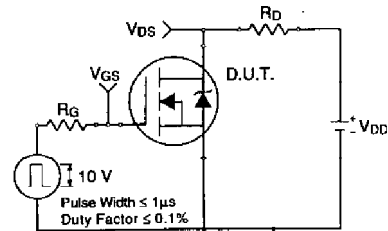
**Fig 7.** Typical Source-Drain Diode Forward Voltage



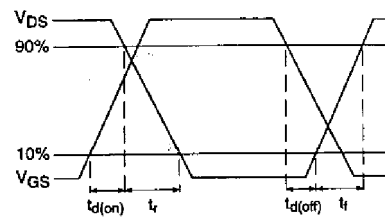
**Fig 8.** Maximum Safe Operating Area



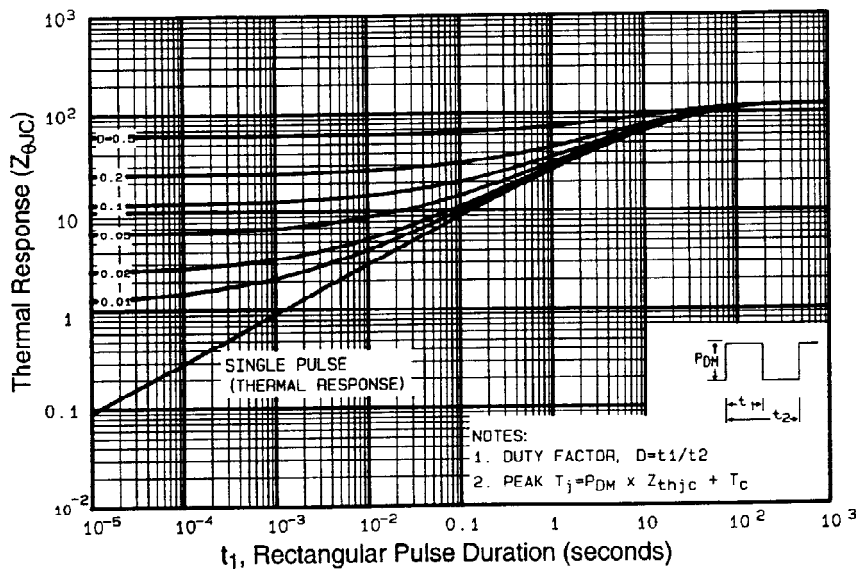
**Fig 9.** Maximum Drain Current Vs. Case Temperature



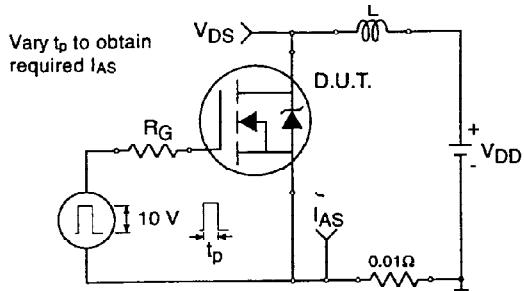
**Fig 10a.** Switching Time Test Circuit



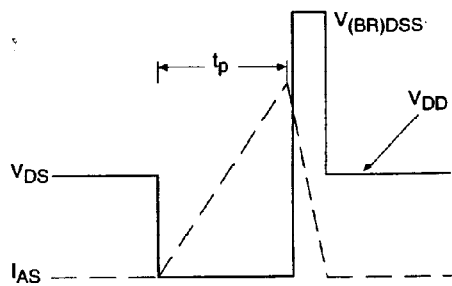
**Fig 10b.** Switching Time Waveforms



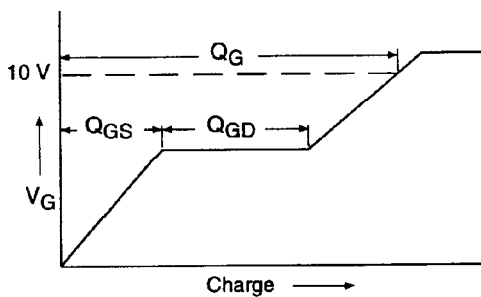
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



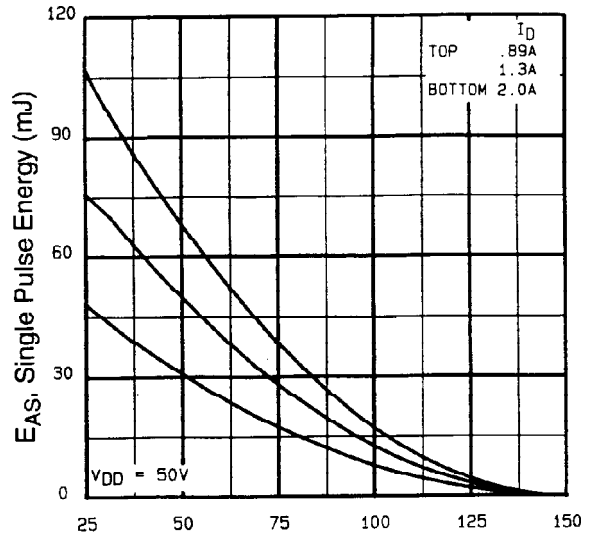
**Fig 12a.** Unclamped Inductive Test Circuit



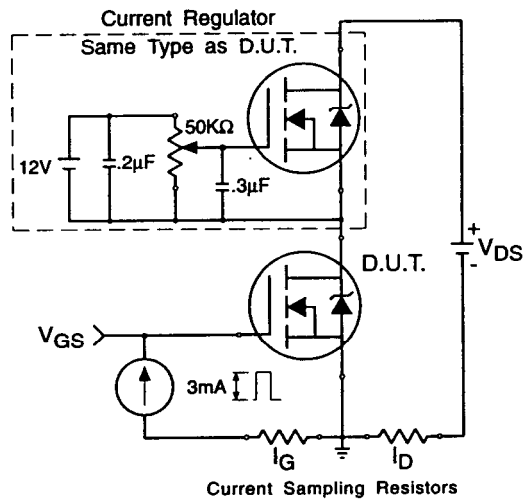
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform



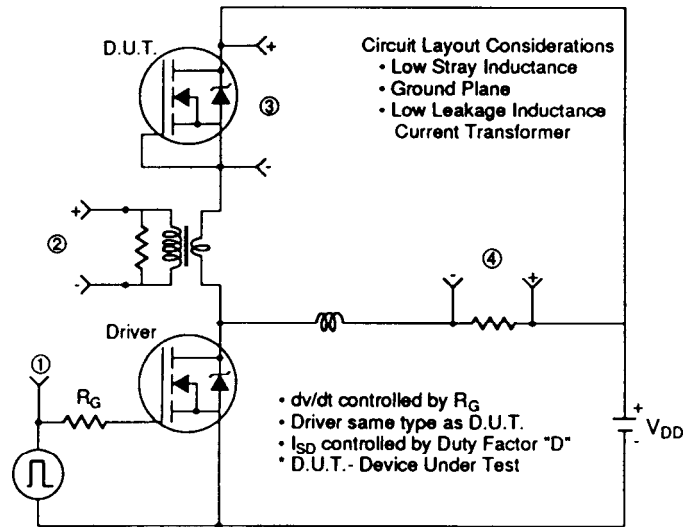
**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



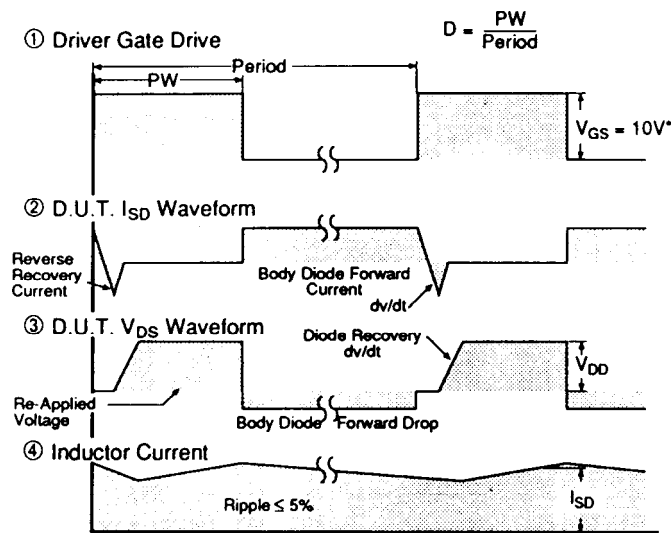
**Fig 13b.** Gate Charge Test Circuit

## dv/dt Test Circuit

Fig 14. For N-Channel HEXFETs



## Peak Diode Recovery Test Circuit

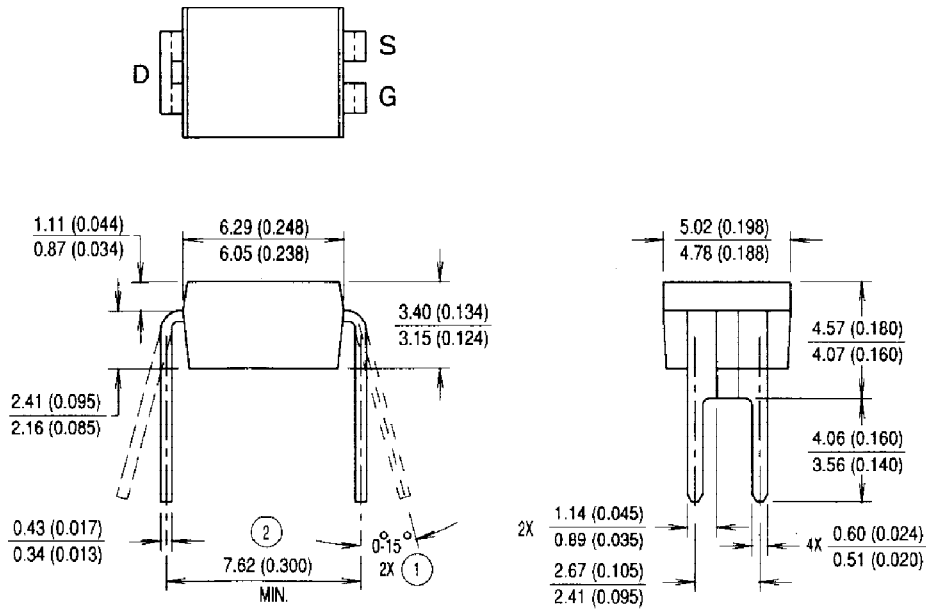


\*  $V_{GS} = 5V$  for Logic Level Devices

# IRFD320



## Package Outline



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**IOR Rectifier**

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**IR CANADA:** 7321 Victoria Park Ave., Suite 201, Markham, Ontario L3R 3L1, Tel: (905) 475 1897 **IR GERMANY:** Saalburgstrasse 157, 61350 Bad Homburg Tel: 6172 37066 **IR ITALY:** Via Liguria 49, 10071 Borgaro, Torino Tel: (39) 1145 10111 **IR FAR EAST:** K&H Bldg., 2F, 3-30-4 Nishi-Ikeburo 3-Chome, Toshima-Ki, Tokyo 171 Tel: (03)3983 0641  
**IR SOUTHEAST ASIA:** 315 Outram Road, #10-02 Tan Boon Liat Building, 0316 Tel: 65 221 8371

*Data and specifications subject to change without notice.*