High-Side & Low-Side Gate Drive IC

General description

The ID2006 is a high voltage, high speed power MOSFET driver with independent high and low side referenced output channels based on P_SUB P_EPI process. The floating channel can be used to drive an N-channel power MOSFET in the high side configuration which operates up to 200 V. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction.

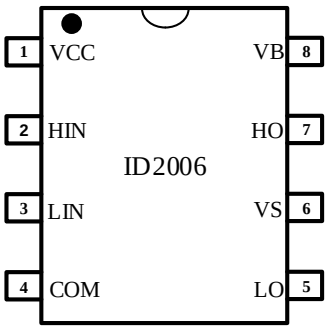
Application

- Small and medium- power motor driver
- Power MOSFETS driver
- Half−Bridge Power Converters
- Full-Bridge Power Converters
- Any Complementary Drive Converters

Features

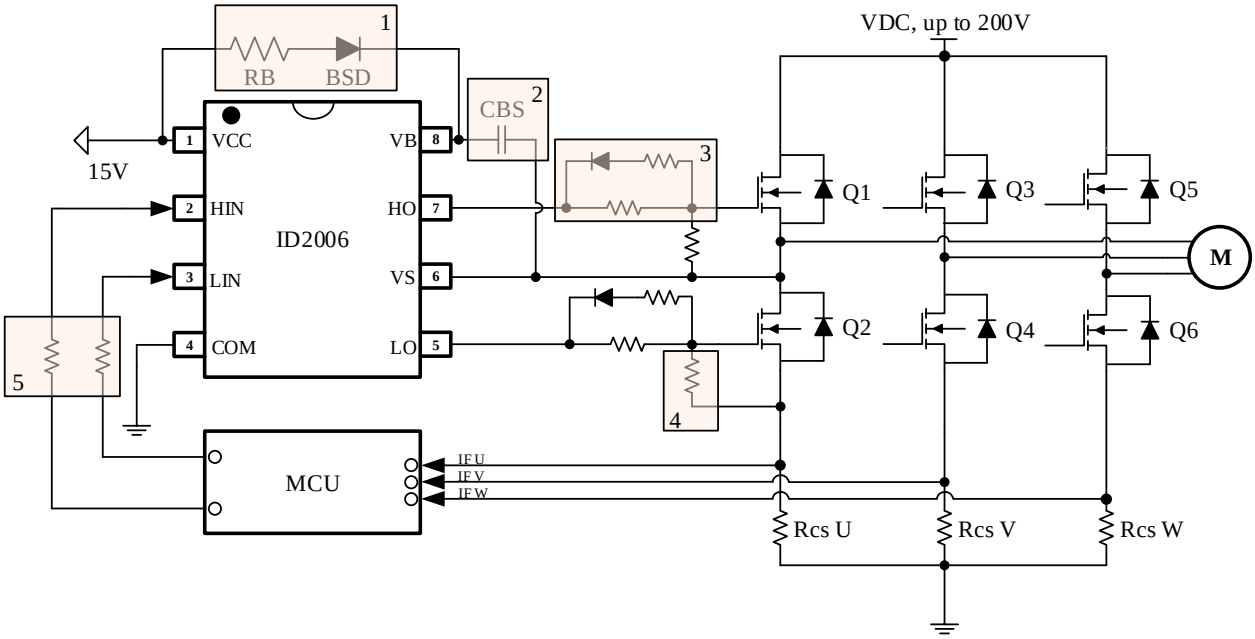
- Fully operational to+200 V
- 3.3V and 5V input logic compatible
- dV/dt Immunity ±50 V/nsec
- Gate drive supply range from 6 V to 18 V
- Typically Source / Sink current capability 1 A/1 A
- Typically -9V negative Vs bias capability

Package/Order Information



Order code	Package
ID2006SEC-R1	SOP8

Typical Circuit

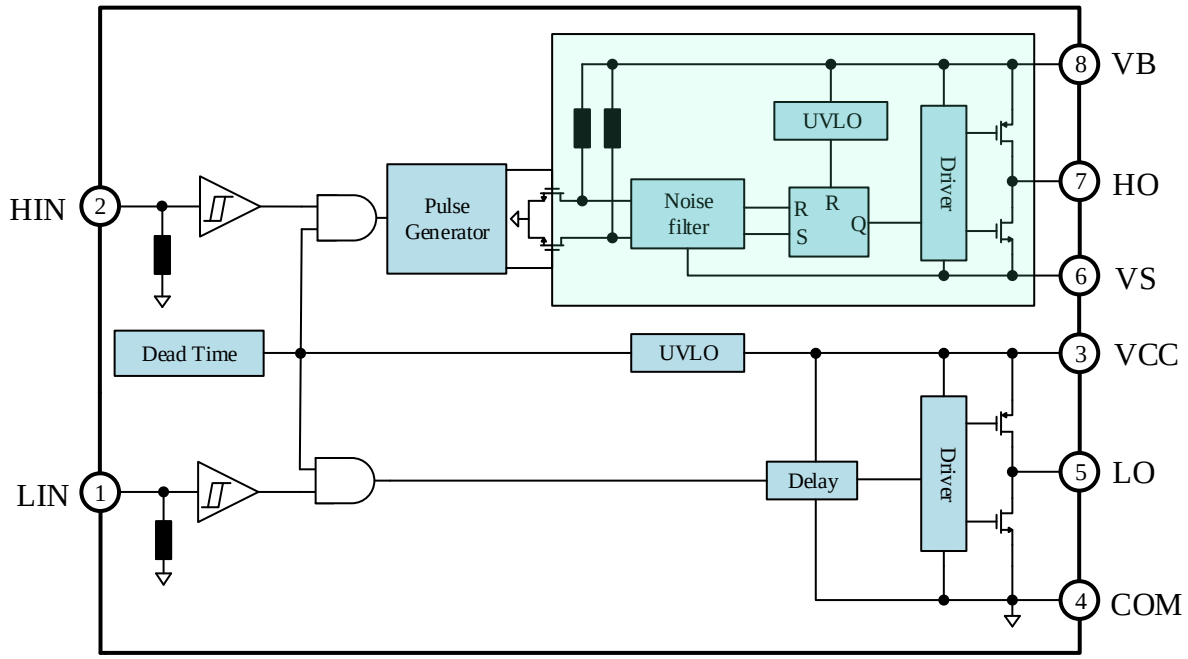


Note 1: RB value suggest 10 ohms, ultra fast recovery or schottky diode should be used as BSD
Note 2: CBS value according to PWM control condition
Note 3: Driver circuit should be adjust according to the MOSFETs be used
Note 4: Pull down resistor between Gate and Source of MOSFETs, 10k ohms is suggested
Note 5: Resistors between HIN/LIN and MCU, recommended value is 100 to 1k ohms

Pin Definitions

Pin Name	Pin Number	Pin Function Description
V_{CC}	1	Low side and main power supply
HIN	2	Logic input for high side gate driver output (HO)
LIN	3	Logic input for low side gate driver output (LO)
COM	4	Ground
LO	5	Low side gate drive output, out of phase with LIN
V_S	6	High side floating supply return or bootstrap return
HO	7	High side gate drive output, in phase with HIN
V_B	8	High side floating supply

Block Diagram



Absolute Maximum Ratings

Exceeding these ratings may damage the device.
The absolute maximum ratings are stress ratings only at T_A=25℃, unless otherwise specified.

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply	-0.3	220	V
V_S	High side floating supply return	V_B – 20	V_B + 0.3	
V_{HO}	High side gate drive output	V_S – 0.3	V_B + 0.3	
V_{CC}	Low side and main power supply	-0.3	20	
V_{LO}	Low side gate drive output	-0.3	V_{CC} + 0.3	
V_{IN}	Logic input of HIN & LIN	-0.3	V_{CC} + 0.3	
ESD	HBM Model	1.5	--	kV
	CDM Model	500	--	V
P_D	Package Power Dissipation @ $T_A \leq 25°C$	--	0.625	W
R_{thJA}	Thermal Resistance Junction to Ambient	--	200	℃ /W
T_J	Junction Temperature	--	150	℃
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	--	300	

Recommended Operating Conditions

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply	V_S + 6	V_S + 18	V
V_S	High side floating supply return	-9	200	
V_{HO}	High side gate drive output voltage	V_S	V_B	
V_{CC}	Low side supply	6	18	
V_{LO}	Low side gate drive output voltage	0	V_{CC}	
V_{IN}	logic input voltage (HIN & LIN)	0	V_{CC}	
T_A	Ambient temperature	-40	125	℃

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25 ℃ unless otherwise specified.

Symbol	Definition	MIN	TYP.	MAX.	Units
t_{ON}	High & low side turn on propagation delay	--	150	250	ns
t_{OFF}	High & low side turn off propagation delay	--	110	250	
MT	Delay matching time (t_{ON}, t_{OFF})	--	--	50	
DT	Dead time	--	300	--	
t_R	Turn on rising time	--	60	100	
t_F	Turn off falling time	--	60	100	

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25 ℃ unless otherwise specified.

Symbol	Definition	MIN.	TYP.	MAX.	Units
I_{LK}	High-side floating supply leakage current	--	--	50	μA
I_{QBS}	Quiescent V_{BS} supply current	--	70	120	
I_{QCC}	Quiescent V_{CC} supply current	--	200	280	
UV_{CCT}	V_{CC} supply under-voltage trigger voltage	4.4	5.0	5.6	V
V_{UVCCHY}	V_{CC} supply under-voltage hysteresis	--	0.3	--	
UV_{BST}	V_{BS} supply under-voltage trigger voltage	3.2	3.8	4.4	
V_{UVBSHY}	V_{BS} supply under-voltage hysteresis	--	0.3	--	
V_{OH}	High level output voltage drop, V_{BIAS} - V_O	--	--	0.2	V
V_{OL}	Low level output voltage drop, V_O	--	--	0.1	
I_{O+}	Output High short circuit pulsed current	--	1	--	A
I_{O-}	Output low short circuit pulsed current	--	1	--	
V_{IH}	High level input threshold voltage	2.5	--	--	V
V_{IL}	Low level input threshold voltage	--	--	0.8	
I_{IN+}	Logic “1” input bias current (HIN “1” & LIN “1”)	--	10	20	μA
I_{IN-}	Logic “0” input bias current (HIN “0” & LIN “0”)	--	15	30	

Function Timing Diagram

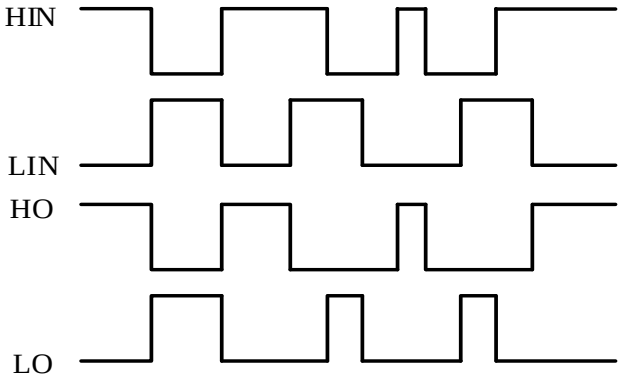


Fig.1 Input and output timing waveform

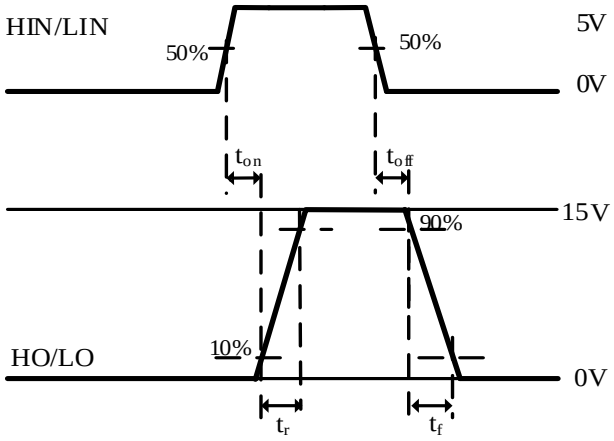


Fig.2 Propagation and Rise/Fall time definition

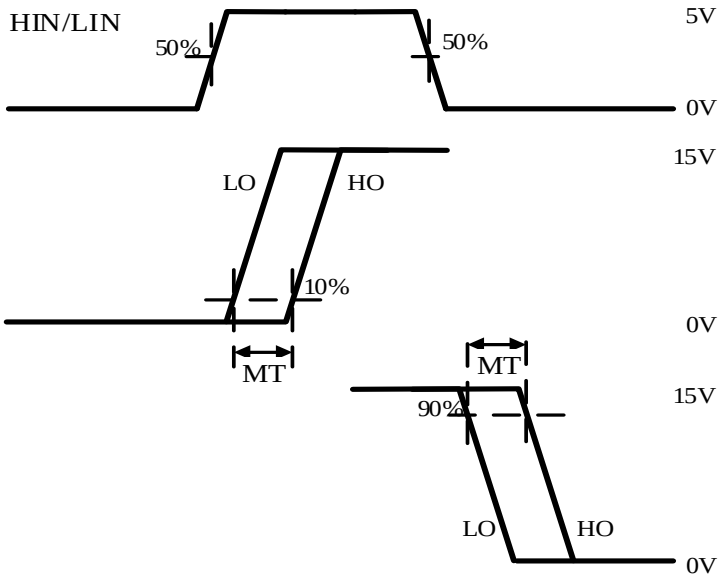
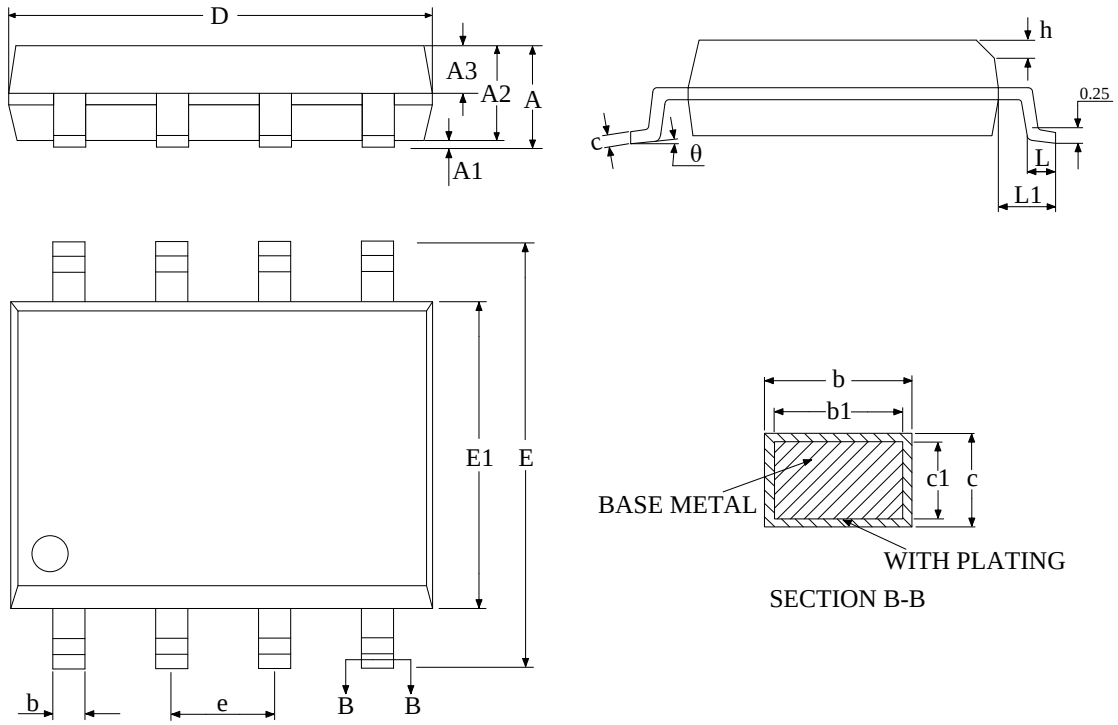


Fig.3 Delay matching definition

Package Information

SOP8 Package Outlines and Dimensions



Symbol \ Size	Min. (mm)	Typ. (mm)	Max. (mm)	Symbol \ Size	Min. (mm)	Typ. (mm)	Max. (mm)
A	-	-	1.75	D	4.70	4.90	5.10
A1	0.10	-	0.225	E	5.80	6.00	6.20
A2	1.30	1.40	1.50	E1	3.70	3.90	4.10
A3	0.60	0.65	0.70	e	1.27BSC		
b	0.39	-	0.48	h	0.25	-	0.50
b1	0.38	0.41	0.43	L	0.50	-	0.80
c	0.21	-	0.26	L1	1.05BSC		
c1	0.19	0.20	0.21	θ	0	-	8°

Top mark	Package
iDR. ID2006 YWWXXXXX	SOP8

Note：Y：Year Code；WW：Week Code；XXXXX：Internal Code

Notes:
1. This drawing is subjected to change without notice.
2. Body dimensions do not include mold flash or protrusion.

Important Notice

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