STC32G12K128-LQFP64/48/32,PDIP40 (New product notice)

1. Features and Price

➢ **Selection and price (No external crystal and external reset required with 15 channels 12-bit ADC)**

MCU	Operating voltage（V）	Flash Code Memory (100 thousand times) (Byte)	edata Internal extended DATA RAM which can be used as stack(Byte)	xdata Internal extended SRAM (Byte)	Enhanced Dual DPTR increasing or decreasing	EEPROM 100 thousand times) (Byte)	Maximum I/O Lines	Traditional I/O interrupt(INT0/INT1/INT2/INT3/INT4) (can wake-up CPU)	All I/O ports support interrupts and can wake up MCU	DMA 8080/6800 interface/ LCM driver(8-bit and 16-bit)	RTC	DMA UARTs which can wake-up CPU	DMA USARTs which can wake-up CPU	CAN	LIN	Full-spped USB	DMA SPI which can wake-up CPU	I²C which can wake-up CPU	MDU32 (Hardware 32-bit Multiplier and Divider)	Timers/Counters (T0-T4 pin Ccn wake-up CPU)	16-bit advanced PWM timer with Complementary symmetrical dead-time	Power-down Wake-up timer	DMA 15 channels high speed ADC (8 PWMs can be used as 8 DACs)	Comparator (May be used as ADC to detect external power-down)	Internal LVD interrupt (can wake-up CPU)	Watch-dog Timer	Internal high reliable reset circuit with 4 levels optional reset threshold voltage	Internal high presision Clock (adjustbal under 33MHz)	Clock output and Reset	Program encrypted transmission (Anti-blocking)	Password can be set for next update	Support RS485 download	Support hardware USB download and debug directly	Online debug itself	Price & Package				products supply information
																																			LQFP64 <12mm*12mm>	LQFP48 <9mm*9mm>	LQFP32<9mm*9mm>	PDIP40	
STC32G12K64	1.9-5.5	64K	4K	8K	2	64K	60	Y	Y	Y	Y	2	2	2	Y	Y	Y	Y	Y	5	8	Y	12bit	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y			√	√	Comc availa
STC32G12K128	1.9-5.5	128K	4K	8K	2	IAP	60	Y	Y	Y	Y	2	2	2	Y	Y	Y	Y	Y	5	8	Y	12bit	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y			√	√	

➢ **Core**
- ✓ Ultra-high speed 32-bit 8051 Core with single clock per machine cycle, which is called 1T and the speed is about 70 times faster than traditional 8051
- ✓ 49 interrupt sources and 4 interrupt priority levels
- ✓ Online debugging is supported

➢ **Operating voltage**
- ✓ 1.9V～5.5V
- ✓ Built-in LDO

➢ **Operating temperature**
- ✓ -40℃~85℃

➢ **Flash memory**
- ✓ Up to 128Kbytes of Flash memory to be used for storing user code
- ✓ Configurable EEPROM size, 512bytes single page for being erased, which can be repeatedly erased more than 100 thousand times.
- ✓ In-System-Programming, ISP in short, can be used to update the application code. No special programmer is needed.
- ✓ Online debugging with single chip is supported, and no special emulator is needed. The number of breakpoints is unlimited theoratically.
- ✓ Support hardware emulation of SWD interface (requires STC-USB Link1 tool)

➢ **SRAM**
- ✓ 4K bytes internal SRAM (EDATA)
- ✓ 8K bytes internal extended RAM (internal XDATA

Notes on using xdata:

When defining variables, single-byte variables can be defined in xdata, and multi-byte (2-byte, 4-byte) variables need to be defined in edata.

➢ **Clock**

- ✓ Internal high precise RC clock IRC(IRC for short), adjustable while ISP and can be divided to lower frequency by user software.
  - ✓ Error:±0.3% (at the temperature 25℃)
  - ✓ -1.35%～+1.30% temperature drift (at the temperature range of -40℃ to +85℃)
  - ✓ -0.76%～+0.98% temperature drift (at the temperature range of -20℃ to 65℃)
- ✓ Internal 32KHz low speed IRC with large error
- ✓ External crystal (4MHz～33MHz) and external clock
- ✓ Internal PLL output clock
  Users can freely choose the above 4 clock sources

➢ **Reset**
- ✓ Hardware reset
  - ✓ Power-on reset. Measured voltage is 1.7V~1.9V. (Effective when the chip does not enable the low voltage reset function)
  - ✓ Reset by reset pin. The default function of P5.4 is the I/O port. The P5.4 pin can be set as the reset pin while ISP download. (Note: When the P5.4 pin is set as the reset pin, the reset level is low.)
  - ✓ Watch dog timer reset
  - ✓ Low voltage detection reset. 4 low voltage detection levels are provided, 2.0V, 2.3V, 2.7V, 3.0V.
- ✓ Software reset
  - ✓ Writing the reset trigger register using software

➢ **Interrupts**
- ✓ 49 interrupt sources: INT0, INT1, INT2, INT3, INT4, timer 0, timer 1, timer 2, timer 3, timer 4, USART1, USART2, UART 3, UART 4, ADC, LVD, SPI, I^2C, comparator, PWMA, PWMB, USB, CAN, CAN2, LIN, LCMIF color screen interface, RTC, all I/O interrupts (8 groups), DMA receive and transmit interrupts of USART 1, DMA receive and transmit interrupts of USART 2, DMA receive and transmit interrupts of UART 3, DMA receive and transmit interrupts of UART 4, DMA interrupt of I2C, DMA interrupt of SPI, DMA interrupt of ADC, DMA interrupt of LCD driver and DMA interrupt of memory-to-memory.
- ✓ 4 interrupt priority levels

➢ **Digital peripherals**
- ✓ 5 16-bit timers: timer0, timer1, timer2, timer3, timer4, where the mode 3 of timer 0 has the Non-Maskable Interrupt (NMI in short) function. Mode 0 of timer 0 and timer 1 is 16-bit Auto-reload mode.
- ✓ 2 high speed USARTs: USART1, USART2, whose maximum baudrate clock may be FOSC/4. The following modes are supported, synchronous serial port mode, asynchronous serial port mode, SPI mode, LIN mode, infrared mode (IrDA), smart card mode (ISO7816)
- ✓ 2 high speed UARTs: UART3, UART4, whose maximum baudrate clock may be FOSC/4
- ✓ 2 groups of enhanced PWM, which can realize 8 channels(4 groups complementary symmetry) control signals with dead time, and support external fault detection function.
- ✓ SPI: Master mode, slave mode or master/slave automatic switch mode are supported.
- ✓ I^2C: Master mode or slave mode are supported.
- ✓ ICE: Hardware support emulation.
- ✓ RTC: Support year, month, day, hour, minute, second, sub-second (1/128 second). And supports clock interrupt and a set of alarm clocks.
- ✓ USB: USB2.0/USB1.1 compatible with full-speed USB, 6 bidirectional endpoints, support 4 endpoint transfer modes (control transfer, interrupt transfer, bulk transfer and isochronous transfer), each endpoint has a 64-byte buffer.
- ✓ CAN: Two independent CAN 2.0 control units.
- ✓ LIN: An independent LIN control unit (supports versions 1.3 and 2.1), USART1 and USART2 can support two sets of LIN.
- ✓ MDU32: Hardware 32-bit Multiplier and Divider which supports 32-bit divided by 32-bit, 32-bit multiplied by 32-bit operations.
- ✓ I/O port interrupt: All I/Os support interrupts, each group of I/O interrupts has an independent interrupt entry address, all I/O interrupts can support 4 types interrupt mode: high level interrupt, low level interrupt, rising edge interrupt, falling edge interrupt. Provides 4 levels of interrupt priority and supports power-down wake-up function.
- ✓ LCD dirver: support 8080 and 6800 interface, and support 8-bit and 16-bit data width.
- ✓ DMA: Support SPI shift to receive data to memory, SPI shift to send data from memory, I2C send data from memory, I2C receive data to memory, USART 1/2 and UART 3/4 receive data to memory, USART 1/2 and UART 3/4 send data from memory, ADC automatically sample data to memory (calculate average value at the same time), LCD driver send data from memory, and copy data from memory to memory
- ✓ Hardware digital ID: support 32 bytes

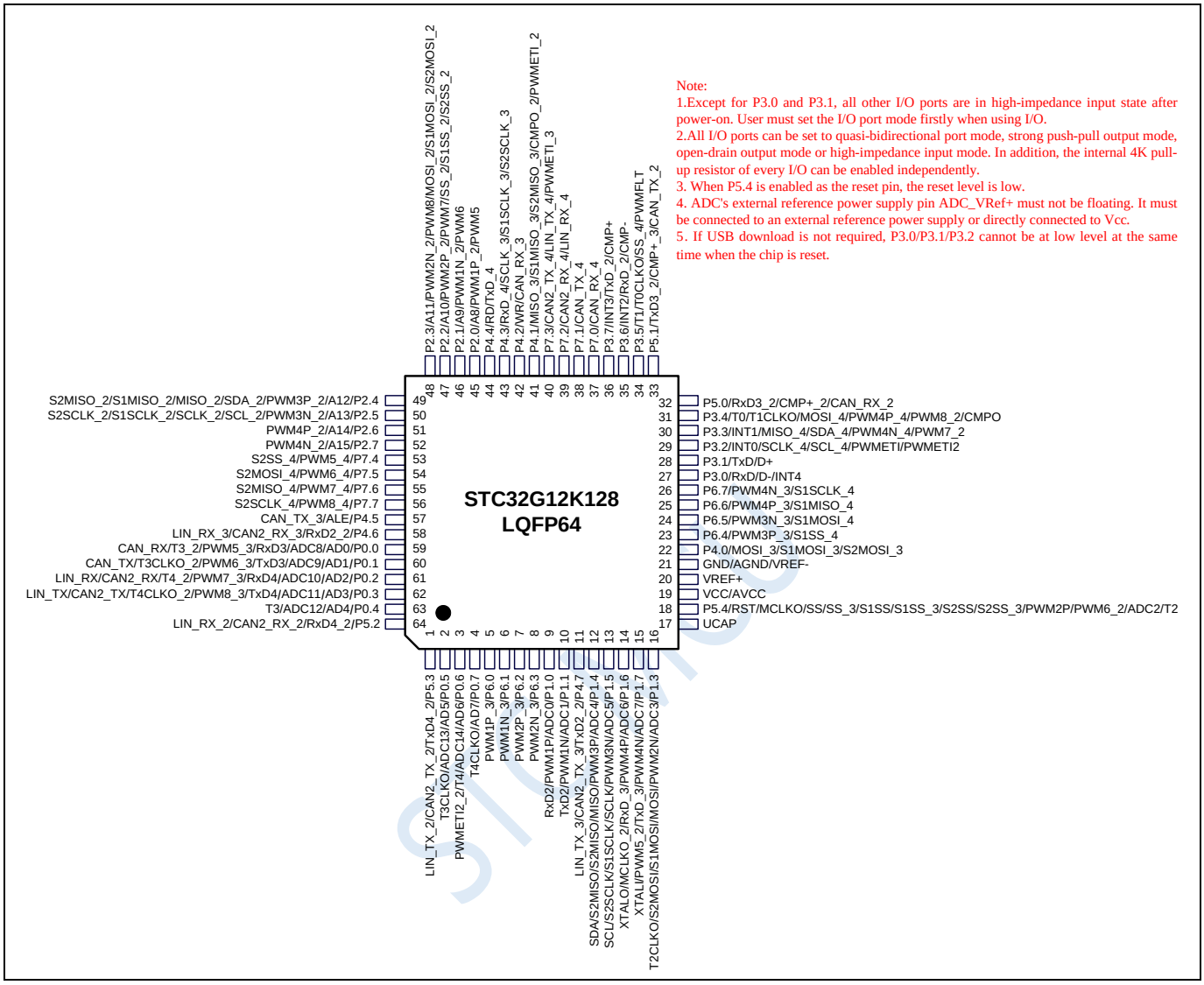
➢ **Analog peripherals**
- ✓ Ultra high speed ADC which supports 12-bit precision 15 channels (channel 0 to channel 14) analog-to-digital conversion. ADC channel 15 is used to test the internal reference voltage. (The default internal reference voltage is 1.19V when the chip is shipped, the error is ±1%)
- ✓ Comparator. A set of comparator

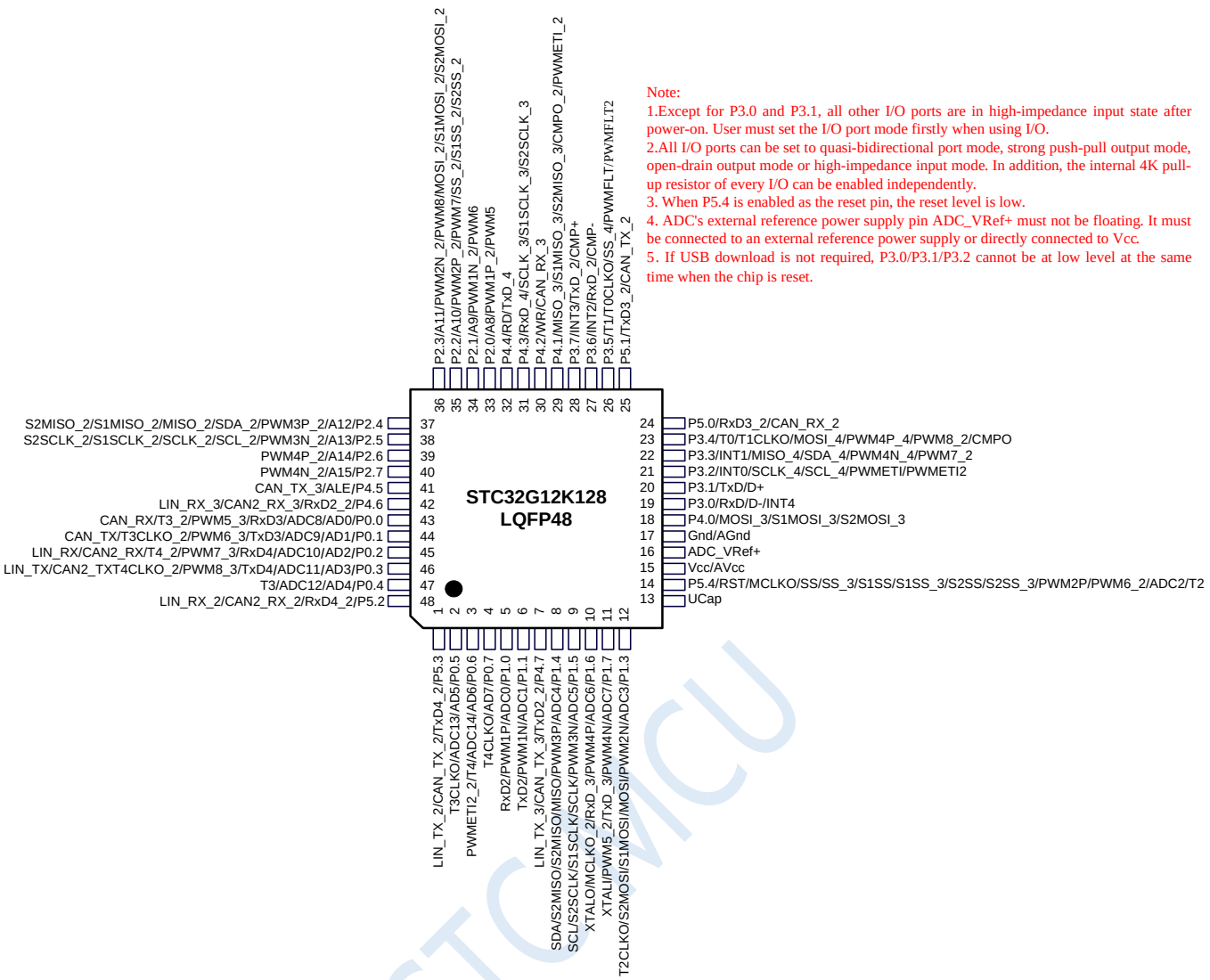
➢ **GPIO**
- ✓ Up to 60 GPIOs: P0.0~P0.7, P1.0~P1.7(No P1.2), P2.0~P2.7, P3.0~P3.7, P4.0~P4.7, P5.0~P5.4, P6.0~P6.7, P7.0~P7.7
- ✓ 4 modes for all GPIOs: quasi_bidirectional mode, push-pull outputmode, open drain mode, high-impedance input mode
- ✓ Except for P3.0 and P3.1, all other I/O ports are in a high-impedance state after power-on. User must set the I/O ports mode before using them. In addition, the internal 4K pull-up resistor of every I/O can be enabled independently.

➢ **Package**

- ✓ LQFP64, LQFP48, LQFP32, PDIP40

2. Pinouts


Note:
1.Except for P3.0 and P3.1, all other I/O ports are in high-impedance input state after power-on. User must set the I/O port mode firstly when using I/O.
2.All I/O ports can be set to quasi-bidirectional port mode, strong push-pull output mode, open-drain output mode or high-impedance input mode. In addition, the internal 4K pull-up resistor of every I/O can be enabled independently.
3. When P5.4 is enabled as the reset pin, the reset level is low.
4. ADC's external reference power supply pin ADC_VRef+ must not be floating. It must be connected to an external reference power supply or directly connected to Vcc.
5. If USB download is not required, P3.0/P3.1/P3.2 cannot be at low level at the same time when the chip is reset.
STC32G12K128
LQFP64
1 LIN_TX_2/CAN2_TX_2/TxD4_2/P5.3
2 T3CLKO/ADC13/AD5/P0.5
3 PWMETI2_2/T4/ADC14/AD6/P0.6
4 T4CLKO/AD7/P0.7
5 PWM1P_3/P6.0
6 PWM1N_3/P6.1
7 PWM2P_3/P6.2
8 PWM2N_3/P6.3
9 RxD2/PWM1P/ADC0/P1.0
10 TxD2/PWM1N/ADC1/P1.1
11 LIN_TX_3/CAN2_TX_3/TxD2_2/P4.7
12 SDA/S2MISO/S2MISO/PWM3P/ADC4/P1.4
13 SCL/S2SCLK/S1SCLK/SCLK/PWM3N/ADC5/P1.5
14 XTALO/MCLKO_2/RxD_3/PWM4P/ADC6/P1.6
15 XTALI/PWM5_2/TxD_3/PWM4N/ADC7/P1.7
16 T2CLKO/S2MOSI/S1MOSI/MOSI/PWM2N/ADC3/P1.3
17 UCAP
18 P5.4/RST/MCLKO/SS/SS_3/S1SS/S1SS_3/S2SS/S2SS_3/PWM2P/PWM6_2/ADC2/T2
19 VCC/AVCC
20 VREF+
21 GND/AGND/VREF-
22 P4.0/MOSI_3/S1MOSI_3/S2MOSI_3
23 P6.4/PWM3P_3/S1SS_4
24 P6.5/PWM3N_3/S1MOSI_4
25 P6.6/PWM4P_3/S1MISO_4
26 P6.7/PWM4N_3/S1SCLK_4
27 P3.0/RxD/D-/INT4
28 P3.1/TxD/D+
29 P3.2/INT0/SCLK_4/SCL_4/PWMETI/PWMETI2
30 P3.3/INT1/MISO_4/SDA_4/PWM4N_4/PWM7_2
31 P3.4/T0/T1CLKO/MOSI_4/PWM4P_4/PWM8_2/CMPO
32 P5.0/RxD3_2/CMP+_2/CAN_RX_2
33 P5.1/TxD3_2/CMP+_3/CAN_TX_2
34 P3.5/T1/T0CLKO/SS_4/PWMFLT
35 P3.6/INT2/RxD_2/CMP-
36 P3.7/INT3/TxD_2/CMP+
37 P7.0/CAN_RX_4
38 P7.1/CAN_TX_4
39 P7.2/CAN2_RX_4/LIN_RX_4
40 P7.3/CAN2_TX_4/LIN_TX_4/PWMETI_3
41 P4.1/MISO_3/S1MISO_3/S2MISO_3/CMPO_2/PWMETI_2
42 P4.2/WR/CAN_RX_3
43 P4.3/RxD_4/SCLK_3/S1SCLK_3/S2SCLK_3
44 P4.4/RD/TxD_4
45 P2.0/A8/PWM1P_2/PWM5
46 P2.1/A9/PWM1N_2/PWM6
47 P2.2/A10/PWM2P_2/PWM7/SS_2/S1SS_2/S2SS_2
48 P2.3/A11/PWM2N_2/PWM8/MOSI_2/S1MOSI_2/S2MOSI_2
49 S2MISO_2/S1MISO_2/MISO_2/SDA_2/PWM3P_2/A12/P2.4
50 S2SCLK_2/S1SCLK_2/SCLK_2/SCL_2/PWM3N_2/A13/P2.5
51 PWM4P_2/A14/P2.6
52 PWM4N_2/A15/P2.7
53 S2SS_4/PWM5_4/P7.4
54 S2MOSI_4/PWM6_4/P7.5
55 S2MISO_4/PWM7_4/P7.6
56 S2SCLK_4/PWM8_4/P7.7
57 CAN_TX_3/ALE/P4.5
58 LIN_RX_3/CAN2_RX_3/RxD2_2/P4.6
59 CAN_RX/T3_2/PWM5_3/RxD3/ADC8/AD0/P0.0
60 CAN_TX/T3CLKO_2/PWM6_3/TxD3/ADC9/AD1/P0.1
61 LIN_RX/CAN2_RX/T4_2/PWM7_3/RxD4/ADC10/AD2/P0.2
62 LIN_TX/CAN2_TX/T4CLKO_2/PWM8_3/TxD4/ADC11/AD3/P0.3
63 T3/ADC12/AD4/P0.4
64 LIN_RX_2/CAN2_RX_2/RxD4_2/P5.2



Note:

1.Except for P3.0 and P3.1, all other I/O ports are in high-impedance input state after power-on. User must set the I/O port mode firstly when using I/O.

2.All I/O ports can be set to quasi-bidirectional port mode, strong push-pull output mode, open-drain output mode or high-impedance input mode. In addition, the internal 4K pull-up resistor of every I/O can be enabled independently.

3. When P5.4 is enabled as the reset pin, the reset level is low.

4. ADC's external reference power supply pin ADC_VRef+ must not be floating. It must be connected to an external reference power supply or directly connected to Vcc.

5. If USB download is not required, P3.0/P3.1/P3.2 cannot be at low level at the same time when the chip is reset.

3. Pin descriptions

Pin number		name	type	description
LQFP64	LQFP48			
1	2	P5.3	I/O	Standard IO port
		TxD4_2	O	Transmit pin of UART 4
		CAN2_TX_2	O	Transmit pin of CAN2
		LIN_TX_2	O	Transmit pin of LIN
2	2	P0.5	I/O	Standard IO port
		AD5	I	Address/data bus
		ADC13	I	ADC analog input 13
		T3CLKO	O	Clock out of timer 3
3	3	P0.6	I/O	Standard IO port
		AD6	I	Address/data bus
		ADC14	I	ADC analog input 14
		T4	I	Timer4 external input
		PWMFLT2_2	I	Enhance PWM external anomaly detection pin 2
4	4	P0.7	I/O	Standard IO port
		AD7	I	Address/data bus
		T4CLKO	O	Clock out of timer 4
5		P6.0	I/O	Standard IO port
		PWM1P_3	I/O	Capture of external signal/ Positive of PWM1 pulse output
6		P6.1	I/O	Standard IO port
		PWM1N_3	I/O	Capture of external signal/ Negative of PWM1 pulse output
7		P6.2	I/O	Standard IO port
		PWM2P_3	I/O	Capture of external signal/ Positive of PWM2 pulse output
8		P6.3	I/O	Standard IO port
		PWM2N_3	I/O	Capture of external signal/ Negative of PWM2 pulse output
9	5	P1.0	I/O	Standard IO port
		ADC0	I	ADC analog input 0
		PWM1P	I/O	Capture of external signal/ Positive of PWMA pulse output
		RxD2	I	Input of USART2
10	6	P1.1	I/O	Standard IO port
		ADC1	I	ADC analog input 1
		PWM1N	I/O	Capture of external signal/Negative of PWMA pulse output
		TxD2	I	Transmit pin of USART 2
11	7	P4.7	I/O	Standard IO port
		TxD2_2	I	Transmit pin of USART 2
		CAN2_TX_3	O	Transmit pin of CAN2
		LIN_TX_3	O	Transmit pin of LIN
12	8	P1.4	I/O	Standard IO port
		ADC4	I	ADC analog input 4
		PWM3P	I/O	Capture of external signal/Positive of PWM3 pulse output
		MISO	I/O	Master Iutput/Slave Onput of SPI
		S1MISO	I/O	Master Iutput/Slave Onput of USART1-SPI
		S2MISO	I/O	Master Iutput/Slave Onput of USART2-SPI
		SDA	I/O	Serial data line of I2C
13	9	P1.5	I/O	Standard IO port
		ADC5	I	ADC analog input 5
		PWM3N	I/O	Capture of external signal/Negative of PWM3 pulse output
		SCLK	I/O	Serial Clock of SPI
		S1SCLK	I/O	Serial Clock of USART1-SPI
		S2SCLK	I/O	Serial Clock of USART2-SPI
		SCL	I/O	Serial Clock line of I2C

Pin number		name	type	description
LQFP64	LQFP48			
14	10	P1.6	I/O	Standard IO port
		ADC6	I	ADC analog input 6
		RxD_3	I	Input of USART 1
		PWM4P	I/O	Capture of external signal/Positive of PWM4 pulse output
		MCLKO_2	O	Main clock output
		XTALO	O	Connect to external oscillator
15	11	P1.7	I/O	Standard IO port
		ADC7	I	ADC analog input 7
		TxD_3	O	Transmit pin of USART 1
		PWM4N	I/O	Capture of external signal/Negative of PWM4 pulse output
		PWM5_2	I/O	Capture of external signal/Pulse output of PWM5
		XTALI	I	Connect to external oscillator
16	12	P1.3	I/O	Standard IO port
		ADC3	I	ADC analog input 3
		MOSI	I/O	Master Output/Slave Input of SPI
		S1MOSI	I/O	Master Output/Slave Input of USART1-SPI
		S2MOSI	I/O	Master Output/Slave Input of USART2-SPI
		PWM2N	I/O	Capture of external signal/Negative of PWM2 pulse output
		T2CLKO	O	Clock out of timer 2
17	13	UCAP	I	USB core power regulator pin
18	14	P5.4	I/O	Standard IO port
		NRST	I	Reset pin (low level reset)
		MCLKO	O	Main clock output
		SS_3	I	Slave selection of SPI (it is output with regard to master)
		SS	I	Slave selection of SPI (it is output with regard to master)
		S1SS_3	I	Slave selection of USART1-SPI (it is output with regard to master)
		S1SS	I	Slave selection of USART1-SPI (it is output with regard to master)
		S2SS_3	I	Slave selection of USART2-SPI (it is output with regard to master)
		S2SS	I	Slave selection of USART2-SPI (it is output with regard to master)
		PWM2P	I/O	Capture of external signal/Positive of PWM2 pulse output
		PWM6_2	I/O	Capture of external signal/Pulse output of PWM6
		T2	I	Timer2 external input
		ADC2	I	ADC analog input 2
19	15	Vcc	Vcc	Power Supply
		AVcc	Vcc	ADC Power Supply
20	16	VRef+	I	Reference voltage pin of ADC
21	17	Gnd	Gnd	Ground
		AGnd	Gnd	ADC Ground
		VRef-	I	Reference voltage ground pin of ADC
22	18	P4.0	I/O	Standard IO port
		MOSI_3	I/O	Master Output/Slave Input of SPI
		S1MOSI_3	I/O	Master Output/Slave Input of USART1-SPI
		S2MOSI_3	I/O	Master Output/Slave Input of USART2-SPI
23		P6.4	I/O	Standard IO port
		PWM3P_3	I/O	Capture of external signal/Positive of PWM3 pulse output
		S1SS_4	I	Slave selection of USART1-SPI (it is output with regard to master)
24		P6.5	I/O	Standard IO port
		PWM3N_3	I/O	Capture of external signal/Negative of PWM3 pulse output
		S1MOSI_4	I/O	Master Output/Slave Input of USART1-SPI
25		P6.6	I/O	Standard IO port
		PWM4P_3	I/O	Capture of external signal/Positive of PWM4 pulse output
		S1MISO_4	I/O	Master Output/Slave Input of USART1-SPI

Pin number		name	type	description
LQFP64	LQFP48			
26		P6.7	I/O	Standard IO port
		PWM4N_3	I/O	Capture of external signal/Negative of PWM4 pulse output
		S1SCLK_4	I/O	Serial Clock of USART1-SPI
27	19	P3.0	I/O	Standard IO port
		D-	I/O	USB data line
		RxD	I	Input of USART1
		INT4	I	External interrupt4
28	20	P3.1	I/O	Standard IO port
		D+	I/O	USB data line
		TxD	O	Transmit pin of USART1
29	21	P3.2	I/O	Standard IO port
		INT0	I	External interrupt0
		SCLK_4	I/O	Serial Clock of SPI
		SCL_4	I/O	Serial Clock line of I2C
		PWMETI	I	PWM external trigger input pin
		PWMET2	I	PWM external trigger input pin 2
30	22	P3.3	I/O	Standard IO port
		INT1	I	External interrupt1
		MISO_4	I/O	Master Iutput/Slave Onput of SPI
		SDA_4	I/O	Serial data line of I2C
		PWM4N_4	I/O	Capture of external signal/Negative of PWM4 pulse output
		PWM7_2	I/O	Capture of external signal/Pulse output of PWM7
31	23	P3.4	I/O	Standard IO port
		T0	I	Timer0 external input
		T1CLKO	O	Clock out of timer 1
		MOSI_4	I/O	Master Output/Slave Input of SPI
		PWM4P_4	I/O	Capture of external signal/Positive of PWM4 pulse output
		PWM8_2	I/O	Capture of external signal/Pulse output of PWM8
		CMPO	O	Output of comparator
32	24	P5.0	I/O	Standard IO port
		RxD3_2	I	Input of UART3
		CMP+_2	I	Positive input of comparator
		CAN_RX_2	I	Receive pin of CAN
33	25	P5.1	I/O	Standard IO port
		TxD3_2	O	Transmit pin of UART 3
		CMP+_3	I	Positive input of comparator
		CAN_TX_2	I	Transmit pin of CAN
34	26	P3.5	I/O	Standard IO port
		T1	I	Timer1 external input
		T0CLKO	O	Clock out of timer 0
		SS_4	I	Slave selection of SPI (it is output with regard to master)
		PWMFLT	I	Enhance PWMA external anomaly detection pin
35	27	P3.6	I/O	Standard IO port
		INT2	I	External interrupt2
		RxD_2	I	Input of USART1
		CMP-	I	Negative input of comparator
36	28	P3.7	I/O	Standard IO port
		INT3	I	External interrupt3
		TxD_2	O	Transmit pin of USART 1
		CMP+	I	Positive input of comparator
37		P7.0	I/O	Standard IO port
		CAN_RX_4	I	Receive pin of CAN

Pin number		name	type	description
LQFP64	LQFP48			
38		P7.1	I/O	Standard IO port
		CAN_TX_4	O	Transmit pin of CAN
40		P7.3	I/O	Standard IO port
		CAN2_TX_4	O	Transmit pin of CAN2
		LIN_TX_4	O	Transmit pin of LIN
		PWMETI_3	I	PWM external trigger input pin
41	29	P4.1	I/O	Standard IO port
		MISO_3	I/O	Master Iutput/Slave Onput of SPI
		S1MISO_3	I/O	Master Iutput/Slave Onput of USART1-SPI
		S2MISO_3	I/O	Master Iutput/Slave Onput of USART2-SPI
		CMPO_2	O	Output of comparator
		PWMETI_3	I	PWM external trigger input pin
42	30	P4.2	I/O	Standard IO port
		WR	O	WRITE signal of external bus
		CAN_RX_3	I	Receive pin of CAN
43	31	P4.3	I/O	Standard IO port
		RxD_4	I	Input of USART1
		SCLK_3	I/O	Serial Clock of SPI
		S1SCLK_3	I/O	Serial Clock of USART1-SPI
		S2SCLK_3	I/O	Serial Clock of USART2-SPI
44	32	P4.4	I/O	Standard IO port
		RD	O	READ signal of external bus
		TxD_4	O	Transmit pin of USART 1
45	33	P2.0	I/O	Standard IO port
		A8	I	Address bus
		PWM1P_2	I/O	Capture of external signal/Positive of PWMA pulse output
		PWM5	I/O	Capture of external signal/Pulse output of PWM5
46	34	P2.1	I/O	Standard IO port
		A9	I	Address bus
		PWM1N_2	I/O	Capture of external signal/Negative of PWMA pulse output
		PWM6	I/O	Capture of external signal/Pulse output of PWM6
47	35	P2.2	I/O	Standard IO port
		A10	I	Address bus
		SS_2	I	Slave selection of SPI (it is output with regard to master)
		S1SS_2	I	Slave selection of USART1-SPI (it is output with regard to master)
		S2SS_2	I	Slave selection of USART2-SPI (it is output with regard to master)
		PWM2P_2	I/O	Capture of external signal/Positive of PWMB pulse output
		PWM7	I/O	Capture of external signal/Pulse output of PWM7
48	36	P2.3	I/O	Standard IO port
		A11	I	Address bus
		MOSI_2	I/O	Master Output/Slave Input of SPI
		S1MOSI_2	I/O	Master Output/Slave Input of USART1-SPI
		S2MOSI_2	I/O	Master Output/Slave Input of USART2-SPI
		PWM2N_2	I/O	Capture of external signal/Negative of PWMB pulse output
		PWM8	I/O	Capture of external signal/Pulse output of PWM8

Pin number		name	type	description
LQFP64	LQFP48			
49	37	P2.4	I/O	Standard IO port
		A12	I	Address bus
		MISO_2	I/O	Master Iutput/Slave Onput of SPI
		S1MISO_2	I/O	Master Iutput/Slave Onput of USART1-SPI
		S2MISO_2	I/O	Master Iutput/Slave Onput of USART2-SPI
		SDA_2	I/O	Serial data line of I2C
		PWM3P_2	I/O	Capture of external signal/Positive of PWM3 pulse output
50	38	P2.5	I/O	Standard IO port
		A13	I	Address bus
		SCLK_2	I/O	Serial Clock of SPI
		S1SCLK_2	I/O	Serial Clock of USART1-SPI
		S2SCLK_2	I/O	Serial Clock of USART2-SPI
		SCL_2	I/O	Serial Clock line of I2C
		PWM3N_2	I/O	Capture of external signal/Negative of PWM3 pulse output
51	39	P2.6	I/O	Standard IO port
		A14	I	Address bus
		PWM4P_2	I/O	Capture of external signal/Positive of PWM4 pulse output
52	40	P2.7	I/O	Standard IO port
		A15	I	Address bus
		PWM4N_2	I/O	Capture of external signal/Negative of PWM4 pulse output
53		P7.4	I/O	Standard IO port
		PWM5_4	I/O	Capture of external signal/Pulse output of PWM5
		S2SS_4	I	Slave selection of USART2-SPI (it is output with regard to master)
54		P7.5	I/O	Standard IO port
		PWM6_4	I/O	Capture of external signal/Pulse output of PWM6
		S2MOSI_4	I/O	Master Iutput/Slave Onput of USART2-SPI
55		P7.6	I/O	Standard IO port
		PWM7_4	I/O	Capture of external signal/Pulse output of PWM7
		S2MISO_4	I/O	Master Iutput/Slave Onput of USART2-SPI
56		P7.7	I/O	Standard IO port
		PWM8_4	I/O	Capture of external signal/Pulse output of PWM8
		S2SCLK_4	I/O	Serial Clock of USART2-SPI
57	41	P4.5	I/O	Standard IO port
		ALE	O	Address Latch Enable signal
		CAN_TX_3	O	Transmit pin of CAN
58	42	P4.6	I/O	Standard IO port
		RxD2_2	I	Input of USART2
		CAN2_RX_3	I	Receive pin of CAN2
		LIN_RX_3	I	Receive pin of LIN
59	43	P0.0	I/O	Standard IO port
		AD0	I	Address/data bus
		ADC8	I	ADC analog input 8
		RxD3	I	Input of UART3
		PWM5_3	I/O	Capture of external signal/Pulse output of PWM5
		CAN_RX	I	Receive pin of CAN

Pin number		name	type	description
LQFP64	LQFP48			
60	44	P0.1	I/O	Standard IO port
		AD1	I	Address/data bus
		ADC9	I	ADC analog input 9
		TxD3	O	Transmit pin of UART 3
		PWM6_3	I/O	Capture of external signal/Pulse output of PWM6
		CAN_TX	O	Transmit pin of CAN
61	45	P0.2	I/O	Standard IO port
		AD2	I	Address/data bus
		ADC10	I	ADC analog input 10
		RxD4	I	Input of UART4
		PWM7_3	I/O	Capture of external signal/Pulse output of PWM7
		CAN2_RX	I	Receive pin of CAN2
		LIN_RX	I	Receive pin of LIN
62	46	P0.3	I/O	Standard IO port
		AD3	I	Address/data bus
		ADC11	I	ADC analog input 11
		TxD4	O	Transmit pin of UART 4
		PWM8_3	I/O	Capture o f external signal/Pulse output of PWM8
		CAN2_TX	O	Transmit pin of CAN2
		LIN_TX	O	Transmit pin of LIN
63	47	P0.4	I/O	Standard IO port
		AD4	I	Address/data bus
		ADC12	I	ADC analog input 12
		T3	I	Timer3 external input
64	48	P5.2	I/O	Standard IO port
		RxD4_2	I	Input of UART4
		CAN2_RX_2	I	Receive pin of CAN2
		LIN_RX_2	I	Receive pin of LIN