SD6500

8 Bits DAC and 2 Diff High Precision ADC

Features

- High precision ADC, 19.3bits ENOB at 8sps. It can be set to 2 differential or 4 single-ended inputs
- Low noise, high input impedance preamplifier with selectable gain options:1, 4, 8, 16, 32, 64, 128, or 256
- Internal 8MHz and 32kHz RC oscillator
- Two-wire communication interface, maximum speed at 1.1MHz
- Built-in 8 bits DAC, supports one output
- Built-in temperature sensor, support single point calibration
- Hardware timing comparison measurement function
- Built-in sensor excitation output, output voltage options: 2.4V, 2.7V, 3.0V and 3.3V
- Low voltage detection and power on reset circuit
- Operating voltage range: 2.4~3.6V
- Operating temperature range: -40~85℃

Description

The SD6500 has built-in 24 bits ADC and two-wire communication circuits.

A host computer can read and edit all the registers in the IC through the two-wire communication circuit.

The IC supports the timed measurement comparison mode. After entering this mode, the IC will turn on the host after successful data comparison. The host can also independently turn on the IC.

The IC has built-in temperature sensor, and 8 bits DAC to meet the requirements of various applications.

Application

High-precision electronic scale, blood glucose meter, and infrared temperature measurement

Ordering Information

MSOP10 package

Pin Diagram and Descriptions

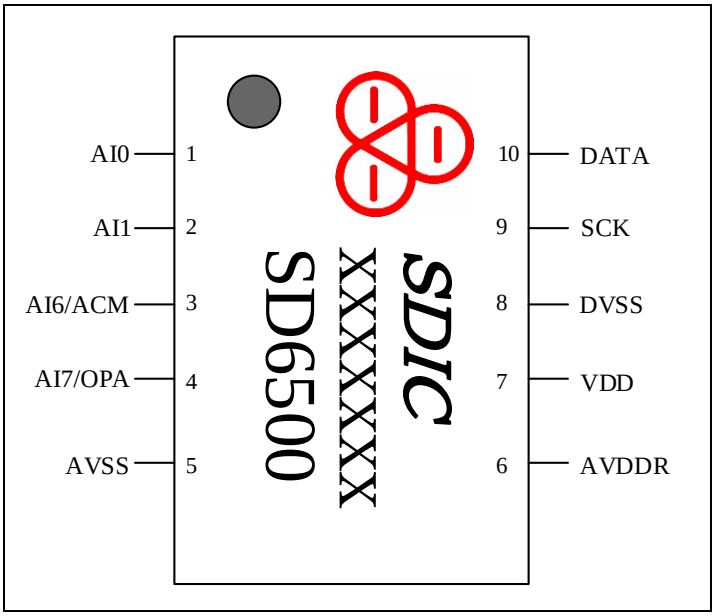


Figure 1. MSOP10 Pin diagram

Table 1. Pin Descriptions

Pin No.	Pin Name	Attribute	Description
1	AI0	Analog	Analog signal differential or 2 single-ended inputs.
2	AI1	Analog	
3	AI6/ACM	Analog	Analog signal input ports can be used as 1 differential or 2 single-ended inputs. AI6 can be used as ACM voltage output and AI7 as the amplifier OPA output
4	AI7/OPA	Analog	
5	AVSS	Ground	Analog ground
6	AVDDR	Analog	Internal LDO output for IC's analog module can provide excitation to the external transducer. The IC connects 0.1uF filter capacitor to AVSS.
7	VDD	Power	Power supply for the IC connects 10uF capacitor to AVSS
8	DVSS	Ground	Digital ground
9	SCK	I	Two-wire communication system clock input
10	DATA	I/O	Two-wire communication system data I/O port

Functional Block

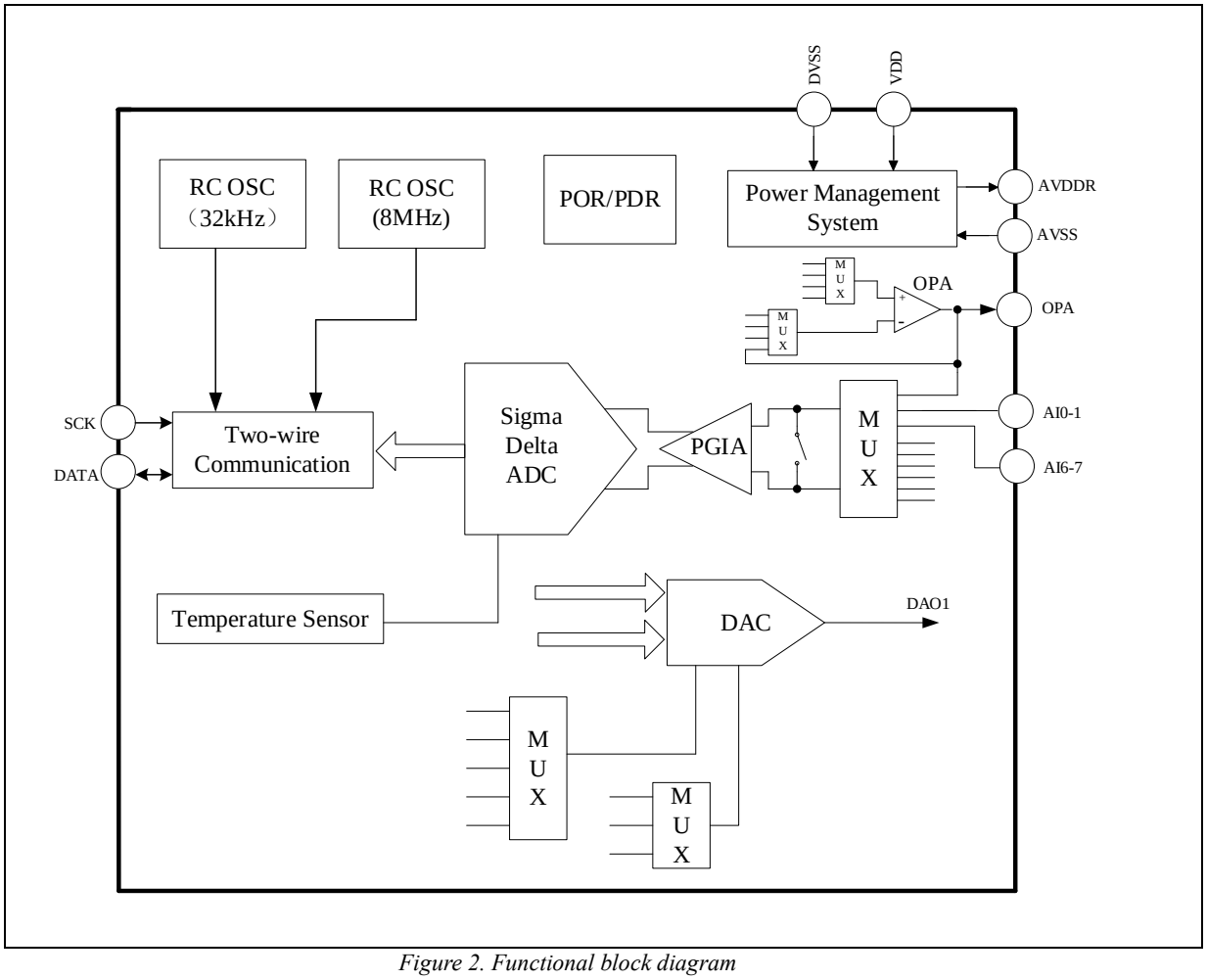


Figure 2. Functional block diagram

Functional Block

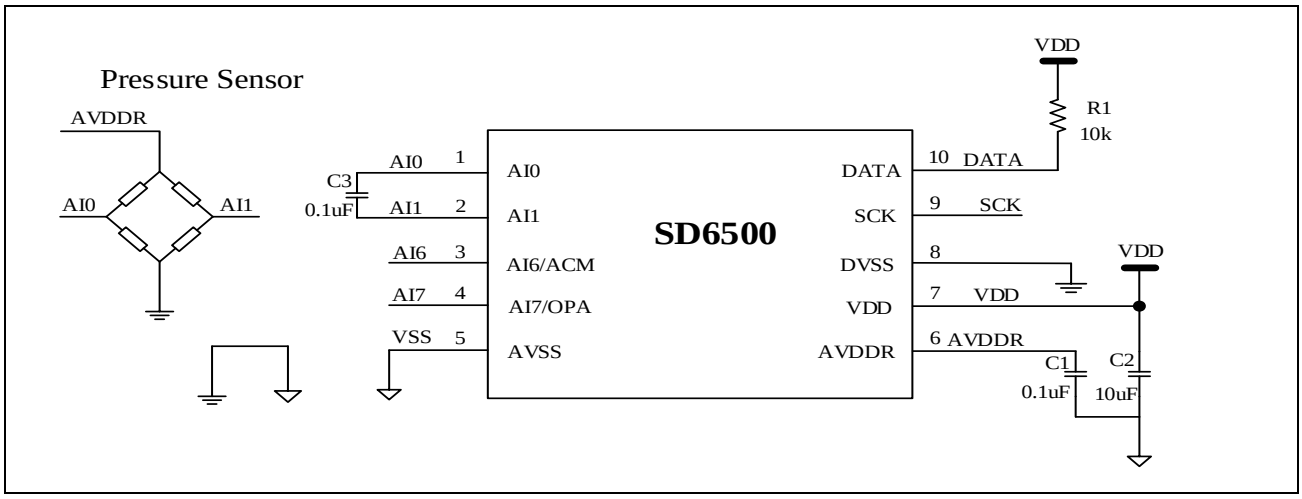


Figure 3. High-precision electronic scale typical application diagram

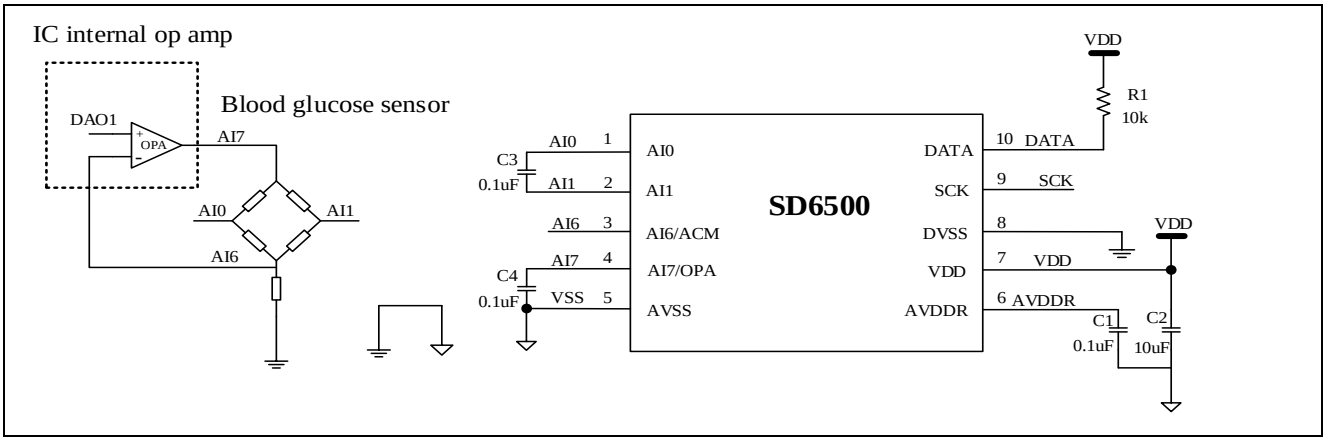


Figure 4. Blood glucose meter typical application diagram

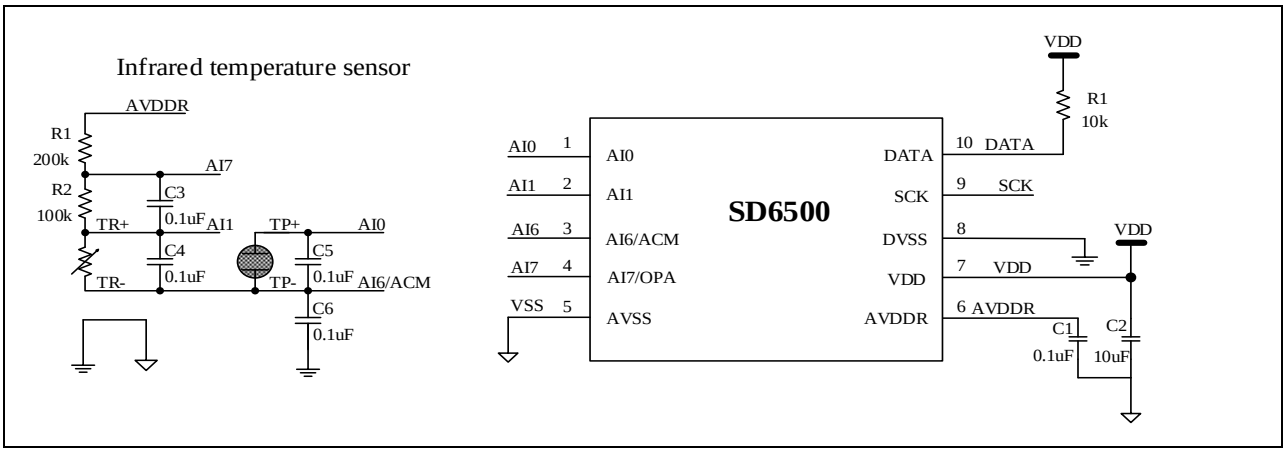


Figure 5. Infrared temperature measurement typical application diagram

ADC Characteristics

Table 2. ENOB and voltage noise Vn_{rms} (AVDDR = 2.4V, VREF = 0.6V, SINC3, Buffer on)

ADC sampling rate = 128kHz									
OSR			128	256	512	1024	2048	4096	8192	16384
Gain	256	ENOB	14.9	15.4	16.0	16.5	16.9	17.4	17.9	18.4
		Vnrms (nV)	298.9	210.5	144.1	102.5	73.7	52.0	36.9	27.5
	128	ENOB	15.8	16.3	16.8	17.3	17.8	18.4	18.9	19.3
		Vnrms (nV)	322.2	219.8	153.9	109.5	76.3	53.6	38.5	28.7
	1	ENOB	16.9	17.9	18.4	19.0	19.5	20.0	20.4	20.9
		Vnrms (nV)	19231.3	9837.5	6324.5	4560.1	3238.6	2305.6	1638.4	1222.0

ADC sampling rate = 512kHz									
OSR			128	256	512	1024	2048	4096	8192	16384
Gain	256	ENOB	14.2	14.7	15.2	15.7	16.2	16.7	17.2	17.7
		Vnrms(nV)	490.9	346.8	247.5	176.1	123.3	86.7	63.7	45.3
	128	ENOB	15.1	15.6	16.0	16.6	17.1	17.5	18.0	18.5
		Vnrms(nV)	539.2	380.0	277.8	190.5	134.9	97.9	70.9	50.7
	1	ENOB	16.8	17.8	18.3	18.8	19.3	19.8	20.3	20.8
		Vnrms(nV)	20484.9	9957.8	6888.3	5001.9	3492.0	2538.9	1802.8	1253.2

Remarks:

1. The above data are averages based on multiple ICs' measured results. Each IC contributes 1024 data points.
2. ENOB = $\log_2\left(\frac{FSR}{Vn_{rms}}\right)$, FSR is the Full-Scale Voltage Range (2 * Vref / Gain), Vn_{rms} is the rms Noise.

Electrical Specifications

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
T_A	Operating temperature	-40	+85	°C
T_S	Storage temperature	-55	+150	°C
V_{DD}	Supply voltage	-0.2	+4.0	V
V_{IN}, V_{OUT}	Digital input/output voltage	-0.2	V_{DD}+0.3	V
T_L	Reflow temperature profile	Per IPC/JEDECJ-STD-020C		°C

Remarks:

1. CMOS device can easily be damaged by electrostatics. It must be stored in conductive foam, and must not exceed the operating voltage range.
2. Turn off power before inserting or removing the device.

Table 4. Electrical Specifications (VDD = 3V, T A = 25°C)

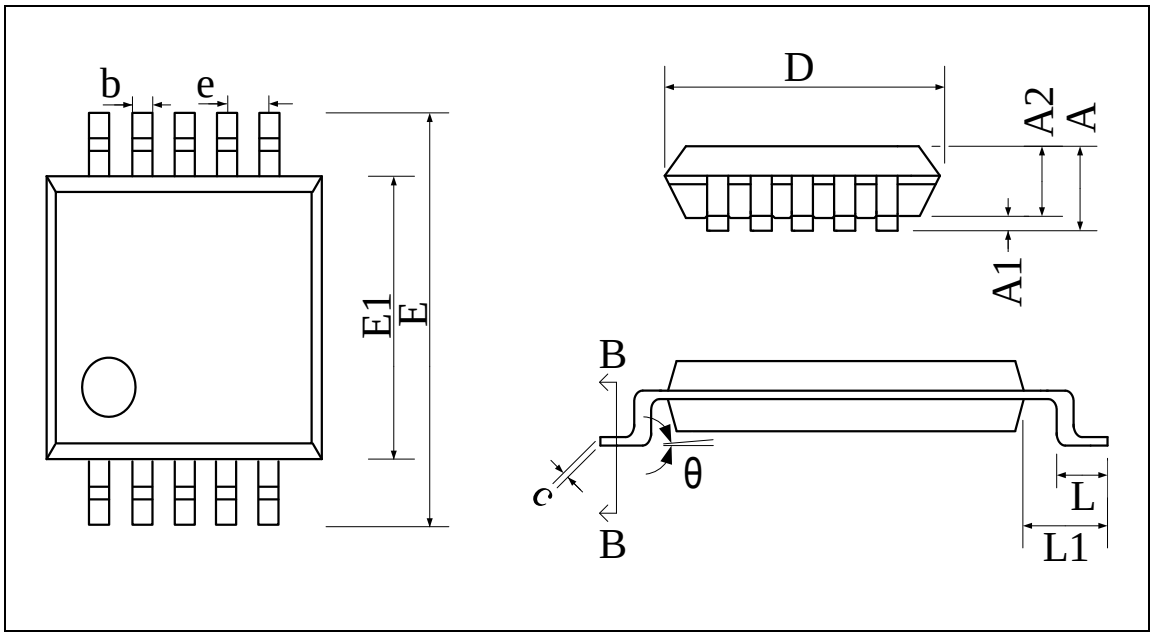
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Remarks
VDD	Supply voltage	2.4	3.3	3.6	V	--
FOSC	Operating frequency	--	8	--	MHz	--
IHRC	Internal high frequency RC oscillator	--	8	--	MHz	--
ILRC	Internal low frequency RC oscillator	--	32	--	kHz	--
IDD1	Operating current 1	--	1.6	--	mA	All analog circuits are active
IDD2	Operating current 2	--	1	--	uA	IC at sleep mode
Fsam	ADC sampling rate	--	--	512	kHz	--
OSR	Over sampling rate	128	--	16384	--	--
NFbit	Noise free bits[1]	--	16	--	bits	Gain = 128， input FSR = ±4mV
NMbit	No missing code output	--	--	24	bits	--
INL	INL	--	0.002	--	%FSR	--
VINdif	PGIA differential input range	-Vref [2]	--	Vref	mV	1X gain
		-Vref/4	--	Vref/4		4X gain
		-Vref/8	--	Vref/8		8X gain
		-Vref/16	--	Vref/16		16X gain
		-Vref/32	--	Vref/32		32X gain
		-Vref/64	--	Vref/64		64X gain
		-Vref/128	--	Vref/128		128X gain
		-Vref/256	--	Vref/256		256X gain
VIN	PGIA voltage input Range [3]	-0.3	--	AVDDR		Gain = 1 and input buffer = off
		0.3	--	AVDDR-0.7		Gain = 1 and input buffer = on, or Gain ≠ 1
Vacm	ACM output voltage	--	1.2	--	V	--
IacmSour	ACM source current	--	1	--	mA	--
IacmSink	ACM sink current	--	1	--	mA	--

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Remarks
PSRacm	ACM PSR	--	100	--	uV/V	--
Vavddr	AVDDR Voltage output	--	2.4	--	V	AVDDRX[1:0] = 00
		--	2.7	--		AVDDRX [1:0] = 01
		--	3.0	--		AVDDRX [1:0] = 10
		--	3.3	--		AVDDRX [1:0] = 11
Iavddr	AVDDR current	--	10	--	mA	--
POR	POR voltage	--	2.0	--	V	--
LVD	LVD voltage	--	1.9	--	V	--
THlbt	LVD hysteresis	--	200	--	mV	--
Communication port I/O Parameter						
VIH	Input high voltage	0.7VDD	--	--	V	--
VIL	Input low voltage	--	--	0.3VDD	V	--
VOH	Output high voltage	VDD-0.3	--	--	V	--
VOL	Output low voltage	--	--	VSS+0.3	V	--

Notes:

1. Noise free bits and effective resolution are both related to the signal's full scale range. Its peak to peak or rms noise plays the decisive role.
2. VREF is the reference voltage signal for the ADC. Its original source is user selectable. The choices are AVDDR, ACM.
3. There are two components that determine the ADC or PGIA input range: differential and absolute. The differential value is determined by PGIA gain and ADC voltage reference choice. The absolute value is limited by the circuit architecture.

Packaging Information



Dimension: mm

Symbol	Min.	Nom.	Max.
A	——	——	1.10
A1	0.05	0.10	0.15
A2	0.75	0.85	0.95
b	0.18	——	0.26
c	0.15	——	0.19
D	2.90	3.00	3.10
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
L	0.40	——	0.70
L1	0.95 REF		
e	0.50 BSC		
θ	0°	——	8°

Figure 6. MSOP10 Mechanical specification