PCM1803A Single-Ended, Analog-Input 24-Bit, 96-kHz Stereo A/D Converter

1 Features

- 24-Bit Delta-Sigma Stereo A/D Converter
- Single-Ended Voltage Input: 3 V_{p-p}
- Oversampling Decimation Filter:
  - Oversampling Frequency: ×64, ×128
  - Pass-Band Ripple: ±0.05 dB
  - Stop-Band Attenuation: –65 dB
  - On-Chip High-Pass Filter: 0.84 Hz (44.1 kHz)
- High-Performance:
  - THD+N: –95 dB (Typically)
  - SNR: 103 dB (Typically)
  - Dynamic Range: 103 dB (Typically)
- PCM Audio Interface:
  - Master or Slave Mode Selectable
  - Data Formats:
    - 24-Bit Left-Justified
    - 24-Bit I^2S
    - 20-, 24-Bit Right-Justified
- Sampling Rate: 16 kHz to 96 kHz
- System Clock: 256 f_S, 384 f_S, 512 f_S, 768 f_S
- Dual Power Supplies: 5 V for Analog, 3.3 V for Digital
- Package: 20-Pin SSOP

2 Applications

- AV Amplifier Receivers
- MD Players
- CD Recorders
- Multitrack Receivers
- Electric Musical Instruments

3 Description

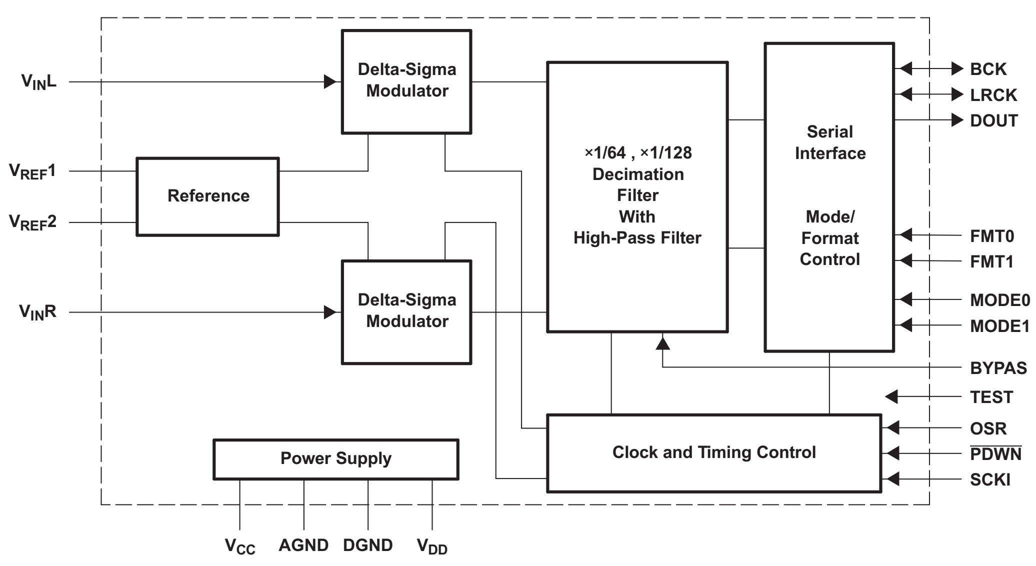
The PCM1803A device is high-performance, low-cost, single-chip stereo analog-to-digital converter with single-ended analog voltage input. The PCM1803A uses a delta-sigma modulator with 64- and 128-times oversampling, and includes a digital decimation filter and high-pass filter, which removes the DC component of the input signal. For various applications, the PCM1803A supports master and slave modes and four data formats in serial interface. The PCM1803A is suitable for a wide variety of cost-sensitive consumer applications where good performance and operation from a 5-V analog supply and 3.3-V digital supply are required. The PCM1803A is fabricated using a highly-advanced CMOS process and is available in a small 20-pin SSOP package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
PCM1803A	SSOP (20)	7.20 mm × 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



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4 Revision History

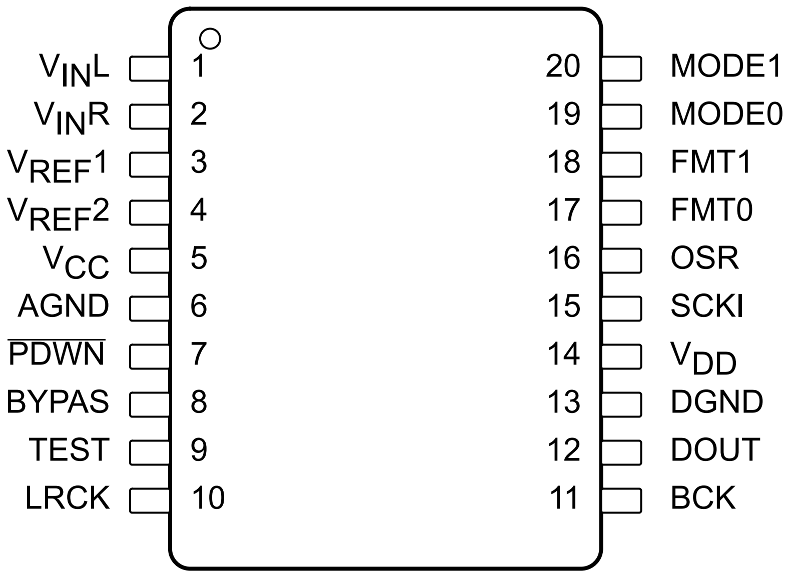
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (August 2006) to Revision B **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1
- Changed $R_{\theta JA}$ value from 115 °C/W to 84.4 °C/W in *Thermal Information* 5
- Changed the *Thermal Information* table 5

5 Pin Configuration and Functions

DB Package
20-Pin SSOP
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	6	–	Analog GND
BCK	11	I/O	Audio data bit clock input/output(1)
BYPAS	8	I	HPF bypass control. LOW: Normal mode (DC reject); HIGH: Bypass mode (through)(2)
DGND	13	–	Digital GND
DOUT	12	O	Audio data digital output
FMT0	17	I	Audio data format select input 0. See *Data Format*.(2)
FMT1	18	I	Audio data format select input 1. See *Data Format*.(2)
LRCK	10	I/O	Audio data latch enable input/output(1)
MODE0	19	I	Mode select input 0. See *Data Format*.(2)
MODE1	20	I	Mode select input 1. See *Data Format*.(2)
OSR	16	I	Oversampling ratio select input. LOW: ×64 f_S, HIGH: ×128 f_S(2)
$\overline{PDWN}$	7	I	Power-down control, active-low (2)
SCKI	15	I	System clock input: 256 f_S, 384 f_S, 512 f_S, or 768 f_S(3)
TEST	9	I	Test, must be connected to DGND(2)
V_{CC}	5	–	Analog power supply, 5-V
V_{DD}	14	–	Digital power supply, 3.3-V
$V_{IN}L$	1	I	Analog input, L-channel
$V_{IN}R$	2	I	Analog input, R-channel
$V_{REF}1$	3	–	Reference-voltage-1 decoupling capacitor
$V_{REF}2$	4	–	Reference-voltage-2 decoupling capacitor

(1) Schmitt-trigger input
(2) Schmitt-trigger input with internal pulldown (50 kΩ, typically), 5-V tolerant
(3) Schmitt-trigger input, 5-V tolerant

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Supply voltage	V_{CC}	–0.3	6.5	V
	V_{DD}	–0.3	4	
Ground voltage differences	AGND, DGND		±0.1	V
Digital input voltage, V_I	LRCK, BCK, DOUT	–0.3	(V_{DD} + 0.3) < 4	V
	$\overline{PDWN}$, BYPAS, TEST, SCKI, OSR, FMT0, FMT1, MODE0, MODE1	–0.3	6.5	
Analog input voltage, V_I	V_{IN}L, V_{IN}R, V_{REF}1, V_{REF}2	–0.3	(V_{CC} + 0.3) < 6.5	V
Input current, I_I	Any pins except supplies		±10	mA
Ambient temperature under bias, T_{bias}		–40	125	°C
Junction temperature, T_J			150	°C
Lead temperature (soldering)	5 s		260	°C
Package temperature (IR reflow, peak)			260	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range

		MIN	NOM	MAX	UNIT
Analog supply voltage, V_{CC}		4.5	5	5.5	V
Digital supply voltage, V_{DD}		2.7	3.3	3.6	V
Analog input voltage, full-scale (–0 dB)			3		Vp-p
Digital input logic family			TTL		
Digital input clock frequency	System clock	8.192		49.152	MHz
	Sampling clock	32		96	kHz
Digital output load capacitance				20	pF
Operating free-air temperature, T_A		–25		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		PCM1803A DB (SSOP) 20 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	84.4	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	42.4	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	41.4	°C/W
$ψ_{JT}$	Junction-to-top characterization parameter	8.3	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	40.7	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 44.1 kHz, system clock = 384 f_S, oversampling ratio = ×128, 24-bit data (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution			24		Bits
DATA FORMAT						
	Audio data interface format			Left-justified, I^2S, right-justified		
	Audio data bit length			20, 24		Bits
	Audio data format			MSB-first, 2s complement		
f_S	Sampling frequency		16	44.1	96	kHz
	System clock frequency	256 f_S	4.096	11.2896	24.576	MHz
		384 f_S	6.144	16.9344	36.864	
		512 f_S	8.192	22.5792	49.152	
		768 f_S	12.288	33.8688		
INPUT LOGIC						
V_{IH} (1)	Input logic-level voltage		2		V_{DD}	Vdc
V_{IL} (1)			0		0.8	
V_{IH} (2) (3)			2		5.5	
V_{IL} (2) (3)			0		0.8	
I_{IH} (1) (2)	Input logic-level current	$V_{IN} = V_{DD}$			±10	µA
I_{IL} (1) (2)		V_{IN} = 0			±10	
I_{IH} (3)		$V_{IN} = V_{DD}$		65	100	
I_{IL} (3)		V_{IN} = 0			±10	
OUTPUT LOGIC						
V_{OH} (4)	Output logic-level voltage	I_{OUT} = –4 mA	2.8			Vdc
V_{OL} (4)		I_{OUT} = 4 mA			0.5	
DC ACCURACY						
	Gain mismatch, channel-to-channel			±1	±3	% of FSR
	Gain error			±2	±4	% of FSR
	Bipolar zero error	HPF bypass		±0.4		% of FSR

(1) Pins 10 to 11: LRCK, BCK (Schmitt-trigger input, in slave mode)
(2) Pin 15: SCKI (Schmitt-trigger input, 5-V tolerant)
(3) Pins 7 to 9, 16 to 20: PDWN, BYPAS, TEST, OSR, FMT0, FMT1, MODE0, MODE1 (Schmitt-trigger input, with 50-kΩ typical pulldown resistor, 5-V tolerant)
(4) Pins 10 to 12: LRCK, BCK (in master mode), DOUT

Electrical Characteristics (continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 44.1 kHz, system clock = 384 f_S, oversampling ratio = ×128, 24-bit data (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE(5)						
THD+N	Total harmonic distortion + noise	V_{IN} = –0.5 dB, f_S = 44.1 kHz		–95	–89	dB
		V_{IN} = –0.5 dB, f_S = 96 kHz(6)		–93		
		V_{IN} = –60 dB, f_S = 44.1 kHz		–41		
		V_{IN} = –60 dB, f_S = 96 kHz(6)		–41		
	Dynamic range	f_S = 44.1 kHz, A-weighted	100	103		dB
		f_S = 96 kHz, A-weighted(6)		103		
SNR	Signal-to-noise ratio	f_S = 44.1 kHz, A-weighted	100	103		dB
		f_S = 96 kHz, A-weighted(6)		103		
	Channel separation	f_S = 44.1 kHz	95	98		dB
		f_S = 96 kHz(6)		99		
ANALOG INPUT						
V_I	Input voltage			0.6 × V_{CC}		Vp-p
	Center voltage (V_{REF}1)			0.5 × V_{CC}		V
	Input impedance			40		kΩ
DIGITAL FILTER PERFORMANCE						
	Pass band				0.454 × f_S	Hz
	Stop band		0.583 × f_S			Hz
	Pass-band ripple				±0.05	dB
	Stop-band attenuation		–65			dB
t_{GD}	Group delay time			17.4 / f_S		s
	HPF frequency response	–3 dB		0.019 × f_S		mHz
POWER SUPPLY REQUIREMENTS						
V_{CC}	Supply voltage range		4.5	5	5.5	Vdc
V_{DD}			2.7	3.3	3.6	Vdc
I_{CC}	Supply current(7)			7.7	10	mA
		Power down(8)		5		µA
I_{DD}		f_S = 44.1 kHz		6.5	9	mA
		f_S = 96 kHz (6)		11.7		mA
		Power down(8)		1		µA
	Power dissipation	f_S = 44.1 kHz		60	80	mW
		f_S = 96 kHz (6)		77		mW
		Power down(8)		28		µW
TEMPERATURE RANGE						
T_A	Operating free-air temperature		–40		85	°C

(5) Analog performance specifications are tested using the System Two™ audio measurement system by Audio Precision™, using 400-Hz HPF, 20-kHz LPF in rms mode.
(6) f_S = 96 kHz, system clock = 256 f_S, oversampling ratio = ×64.
(7) Minimum load on DOUT (pin 12), BCK (pin 11), LRCK (pin 10)
(8) Halt SCKI, BCK, LRCK

6.6 Typical Characteristics

6.6.1 Typical Curves of Internal Filter

6.6.1.1 Decimation Filter Frequency Response

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 44.1 kHz, system clock = 384 f_S, oversampling ratio = ×128, 24-bit data (unless otherwise noted)

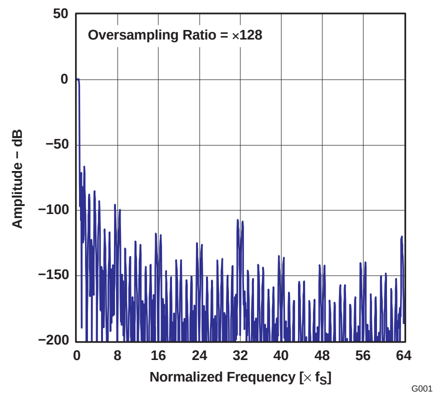


Figure 1. Overall Characteristics

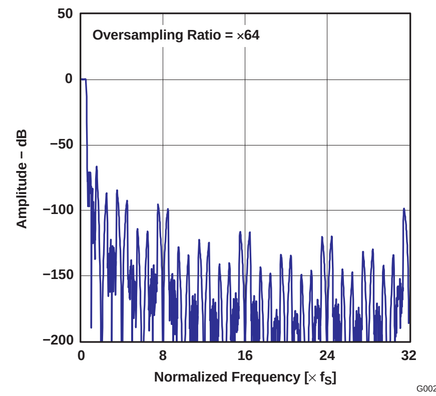


Figure 2. Overall Characteristics

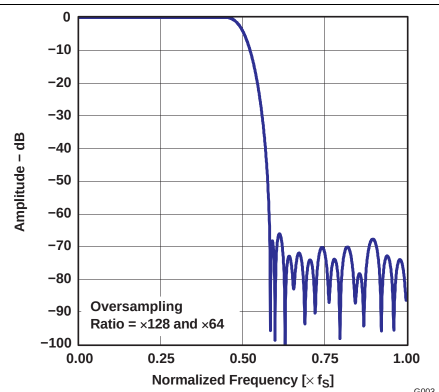


Figure 3. Stop-Band Attenuation Characteristics

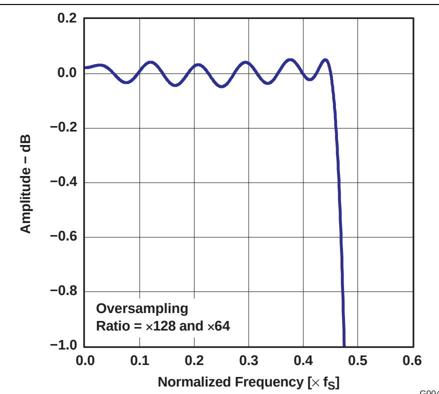


Figure 4. Pass-Band Ripple Characteristics

6.6.1.2 Low-Cut Filter Frequency Response

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 44.1 kHz, system clock = 384 f_S, oversampling ratio = ×128, 24-bit data (unless otherwise noted)

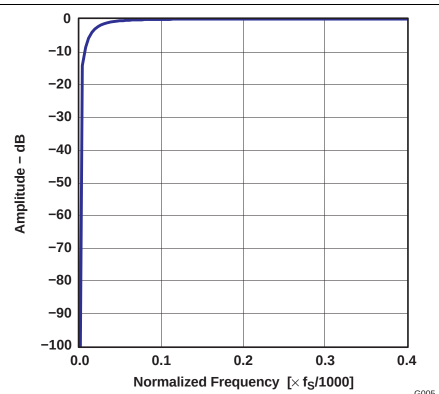


Figure 5. HPF Stop-Band Characteristics

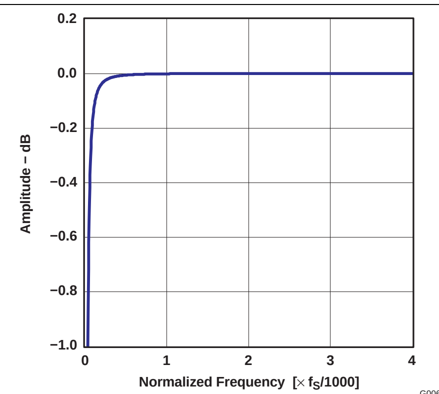


Figure 6. HPF Pass-Band Characteristics

6.6.2 Typical Performance Curves

All specifications at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, master mode, f_S = 44.1 kHz, system clock = 384 f_S, oversampling ratio = ×128, 24-bit data (unless otherwise noted)

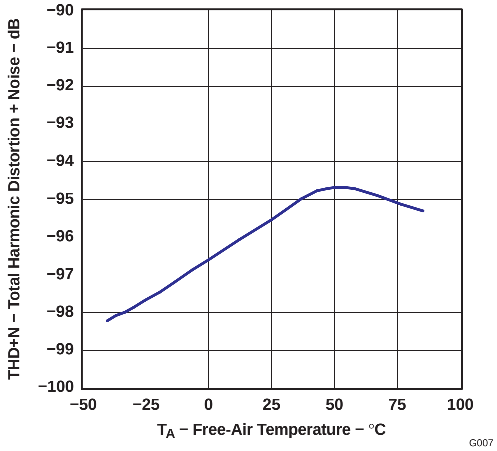


Figure 7. Total Harmonic Distortion + Noise vs Temperature

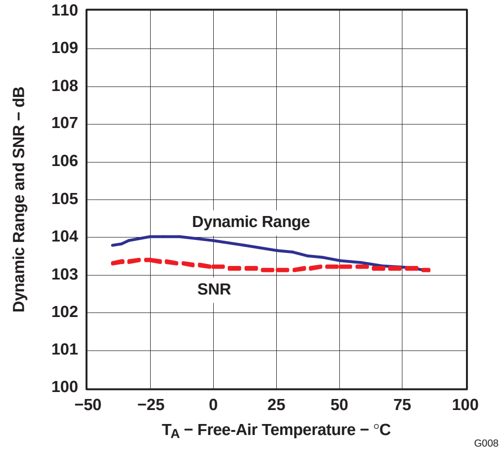


Figure 8. Dynamic Range and Signal-to-Noise Ratio vs Temperature

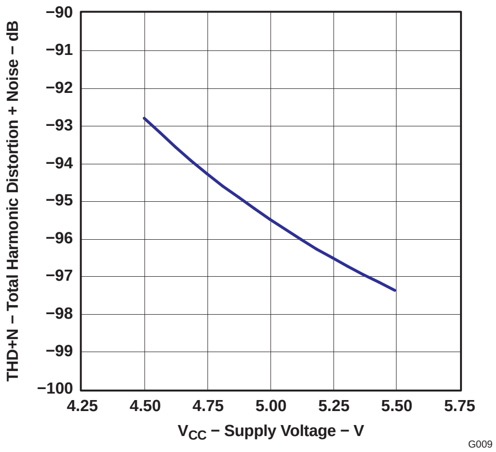


Figure 9. Total Harmonic Distortion + Noise vs Supply Voltage

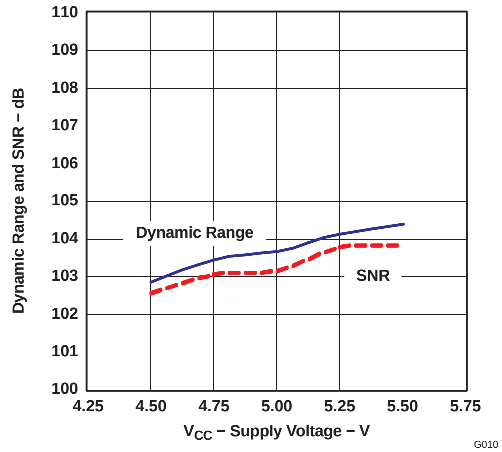


Figure 10. Dynamic Range and Signal-to-Noise Ratio vs Supply Voltage

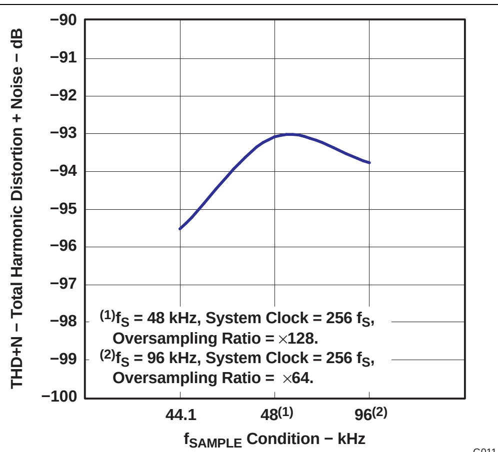


Figure 11. Total Harmonic Distortion + Noise vs f_{SAMPLE} Condition

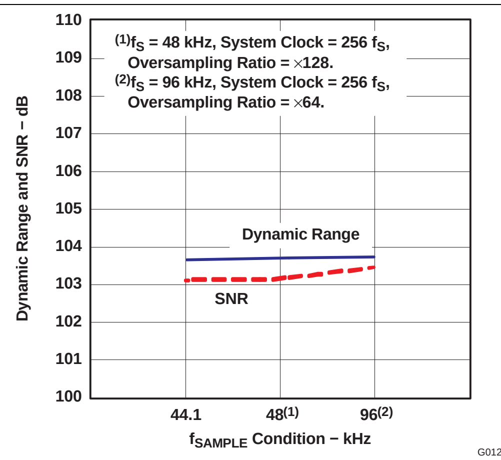


Figure 12. Dynamic Range and Signal-to-Noise Ratio vs f_{SAMPLE} Condition

6.6.3 Output Spectrum

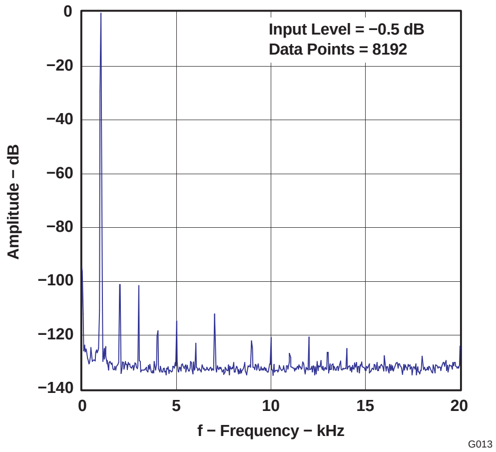


Figure 13. Output Spectrum

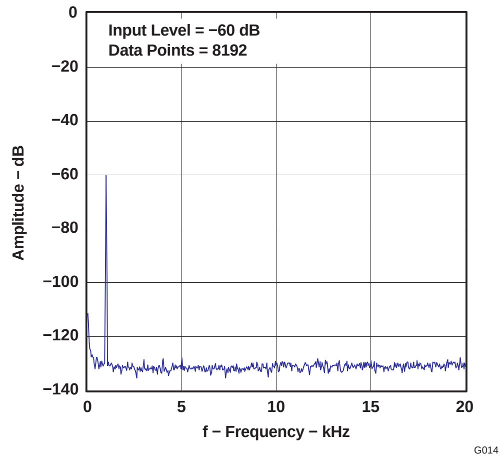


Figure 14. Output Spectrum

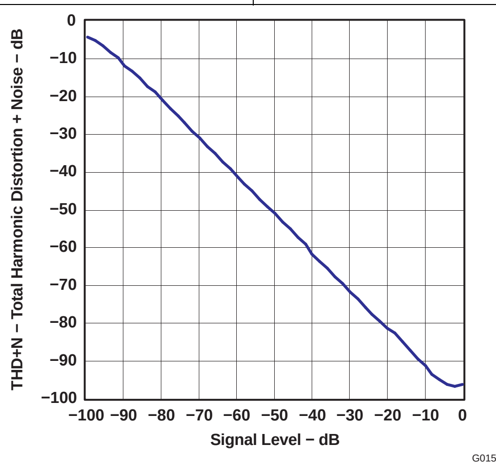


Figure 15. Total Harmonic Distortion + Noise vs Signal Level

6.6.4 Supply Current

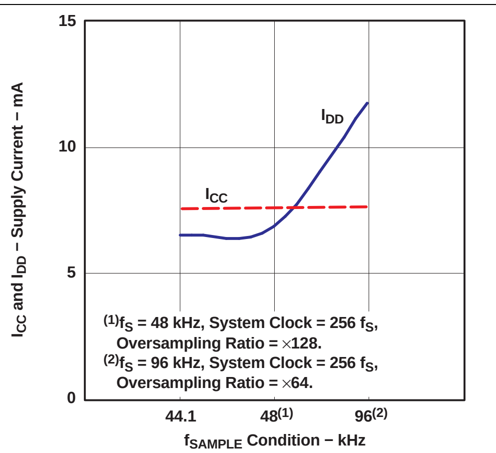


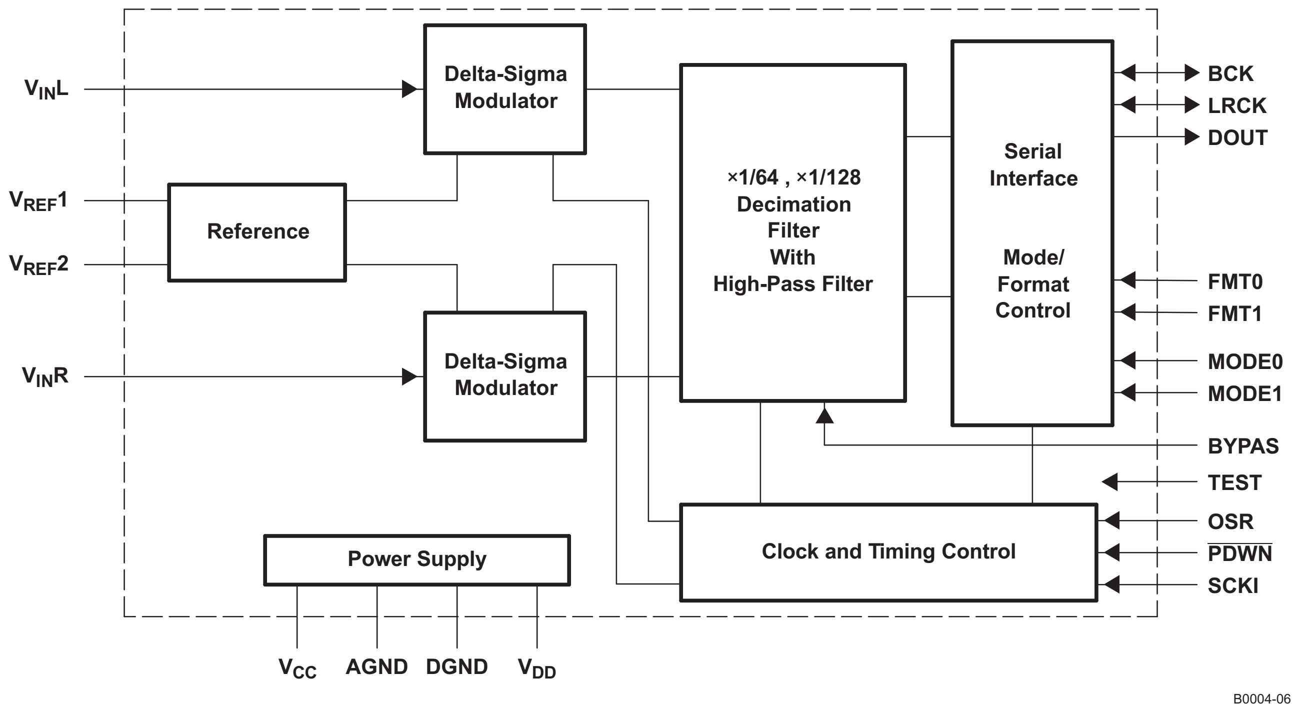
Figure 16. Supply Current vs f_{SAMPLE} Condition

7 Detailed Description

7.1 Overview

The PCM1803A is suitable for a wide variety of cost-sensitive consumer applications where good performance and operation from a 5-V analog supply and 3.3-V digital supply are required. With hardware control and straightforward operation, the PCM1803A can quickly be implemented into an application. The PCM1803A supports sampling rates from 16 kHz to 96 kHz as well as left justified, right justified, and I^2S formats, allowing its use in a variety of audio systems.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Hardware Control

Pins FMT0, FMT1, OSR, BYPASS, MD0, and MD1 allow the device to be controlled by either tying these pins to GND, or VDD, as well as GPIO, from a host IC. These controls allow full configuration of the PCM1803A.

7.3.2 Power-On-Reset Sequence

The PCM1803A has an internal power-on-reset circuit, and initialization (reset) is performed automatically at the time when power-supply voltage (V_{DD}) exceeds 2.2 V (typical). While V_{DD} < 2.2 V (typical) and for 1024 system clock cycles after V_{DD} > 2.2 V (typical), the PCM1803A stays in the reset state, and the digital output is forced to zero. The digital output becomes valid when a time period of $4480/f_S$ has elapsed following release from the reset state. Figure 17 illustrates the internal power-on-reset timing and the digital output for power-on reset.

Feature Description (continued)

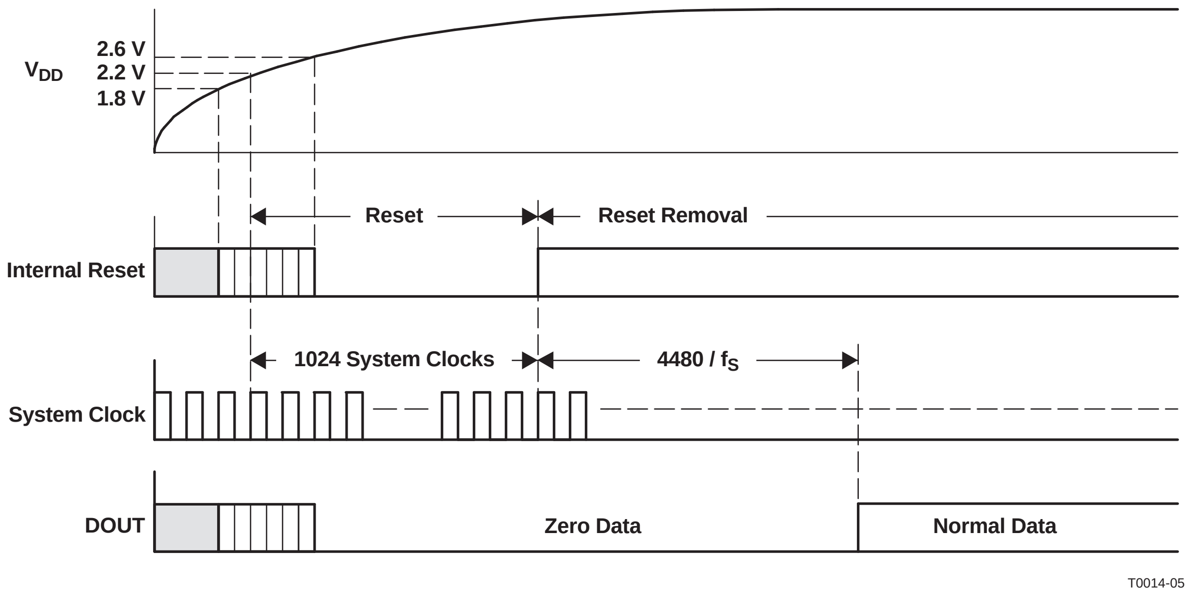


Figure 17. Internal Power-On-Reset Timing

7.3.3 System Clock

The PCM1803A supports 256 f_S, 384 f_S, 512 f_S, and 768 f_S as the system clock, where f_S is the audio sampling frequency. The system clock must be supplied on SCKI (pin 15).

The PCM1803A has a system clock-detection circuit that automatically senses if the system clock is operating at 256 f_S, 384 f_S, 512 f_S, or 768 f_S in slave mode. In master mode, the system clock frequency must be selected by MODE0 (pin 19) and MODE1 (pin 20), and 768 f_S is not available. The system clock is divided automatically into 128 f_S and 64 f_S, and these frequencies are used to operate the digital filter and the delta-sigma modulator.

Table 1 shows the relationship of typical sampling frequency and system clock frequency, and Figure 18 shows system clock timing.

Table 1. Sampling Frequency and System Clock Frequency

SAMPLING FREQUENCY (kHz)	SYSTEM CLOCK FREQUENCY (MHz)			
	256 f_S	384 f_S	512 f_S	768 f_S (1)
32	8.1920	12.2880	16.3840	24.5760
44.1	11.2896	16.9344	22.5792	33.8688
48	12.2880	18.4320	24.5760	36.8640
64	16.3840	24.5760	32.7680	49.1520
88.2	22.5792	33.8688	45.1584	–
96	24.5760	36.8640	49.1520	–

(1) Slave mode only

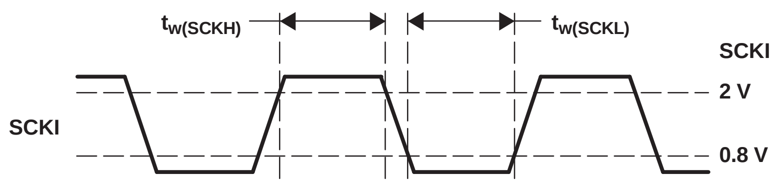


Figure 18. System Clock Timing

Table 2. System Clock Timing Requirements

PARAMETER		MIN	MAX	UNIT
$t_{w(SCKH)}$	System clock pulse duration, HIGH	8		ns
$t_{w(SCKL)}$	System clock pulse duration, LOW	8		ns

The quality of the system clock can influence the dynamic performance, because the PCM1803A operates based on a system clock. Therefore, it may be required to consider the system-clock duty, jitter, and the time difference between system-clock transition and BCK or LRCK transition in the slave mode.

7.4 Device Functional Modes

7.4.1 Serial Audio Data Interface

The PCM1803A interfaces the audio system through BCK (pin 11), LRCK (pin 10), and DOUT (pin 12).

7.4.1.1 Interface Mode

The PCM1803A supports master mode and slave mode as interface modes, and they are selected by MODE1 (pin 20) and MODE0 (pin 19) as shown in Table 3.

In master mode, the PCM1803A provides the timing of serial audio data communications between the PCM1803A and the digital audio processor or external circuit. While in slave mode, the PCM1803A receives the timing for data transfers from an external controller.

Table 3. Interface Mode

MODE1	MODE0	INTERFACE MODE
0	0	Slave mode (256 f_S, 384 f_S, 512 f_S, 768 f_S)
0	1	Master mode (512 f_S)
1	0	Master mode (384 f_S)
1	1	Master mode (256 f_S)

7.4.1.1.1 Master Mode

In master mode, BCK and LRCK work as output pins, and these pins are controlled by timing, which is generated in the clock circuit of the PCM1803A. The frequency of BCK is fixed at LRCK × 64. The 768-f_S system clock is not available in master mode.

7.4.1.1.2 Slave Mode

In slave mode, BCK and LRCK work as input pins. The PCM1803A accepts the 64-BCK/LRCK or 48-BCK/LRCK format (only for 384 f_S and 768 f_S system clocks), not the 32-BCK/LRCK format.

7.4.1.2 Data Format

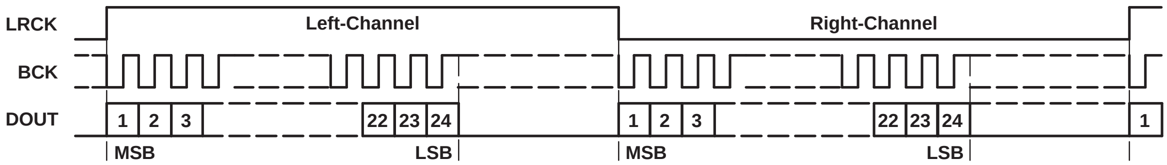
The PCM1803A supports four audio data formats in both master and slave modes, and the data formats are selected by FMT1 (pin 18) and FMT0 (pin 17) as shown in Table 4. Figure 19 illustrates the data formats in slave and master modes.

Table 4. Data Formats

FORMAT	FMT1	FMT0	DESCRIPTION
0	0	0	Left-justified, 24-bit
1	0	1	I^2S, 24-bit
2	1	0	Right-justified, 24-bit
3	1	1	Right-justified, 20-bit

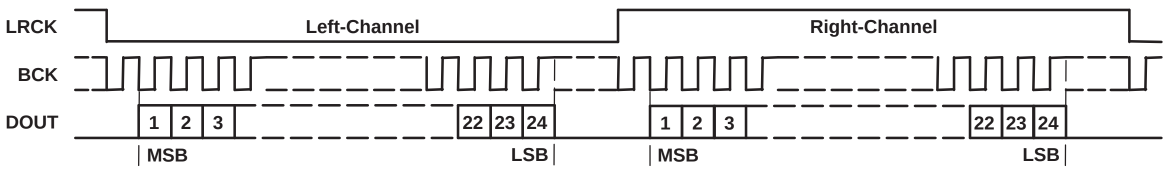
FORMAT 0: FMT[1:0] = 00

24-Bit, MSB-First, Left-Justified



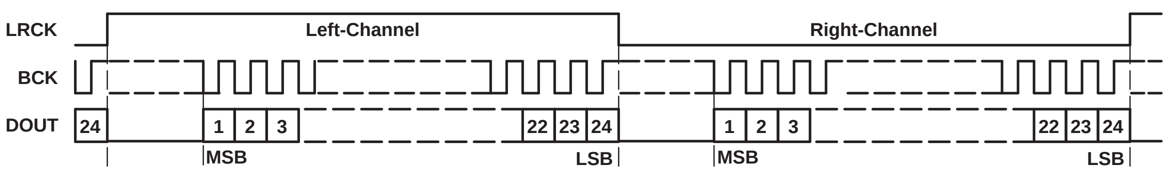
FORMAT 1: FMT[1:0] = 01

24-Bit, MSB-First, I2S



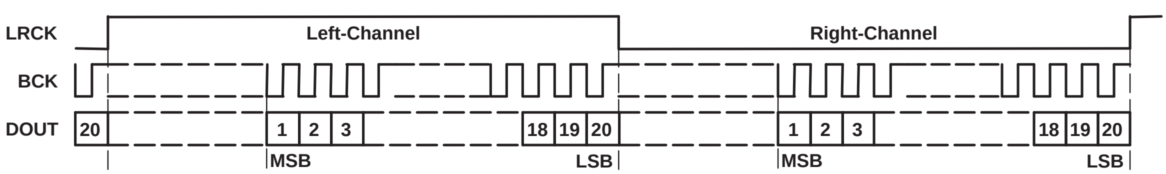
FORMAT 2: FMT[1:0] = 10

24-Bit, MSB-First, Right-Justified



FORMAT 3: FMT[1:0] = 11

20-Bit, MSB-First, Right-Justified



T0016-11

Figure 19. Audio Data Formats (LRCK and BCK Work as Inputs in Slave Mode and as Outputs in Master Mode)

7.4.1.3 Interface Timing

Figure 20 illustrates the interface timing in slave mode; Figure 21 and Figure 22 illustrate the interface timing in master mode.

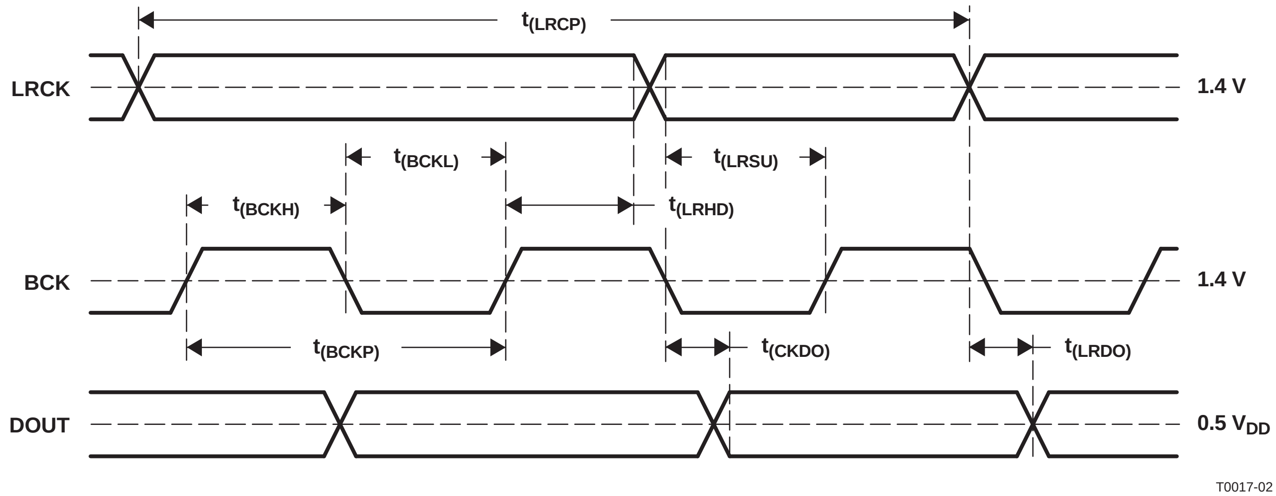


Figure 20. Audio Data Interface Timing (Slave Mode: LRCK and BCK Work as Inputs)

Table 5. Audio Data Interface Slave Mode Timing Requirements(1)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{(BCKP)}$	BCK period	1/(64 f_S)			ns
$t_{(BCKH)}$	BCK pulse duration, HIGH	1.5 × $t_{(SCKI)}$			ns
$t_{(BCKL)}$	BCK pulse duration, LOW	1.5 × $t_{(SCKI)}$			ns
$t_{(LRSU)}$	LRCK setup time to BCK rising edge	40			ns
$t_{(LRHD)}$	LRCK hold time to BCK rising edge	20			ns
$t_{(LRCP)}$	LRCK period	10			µs
$t_{(CKDO)}$	Delay time, BCK falling edge to DOUT valid	–10		40	ns
$t_{(LRDO)}$	Delay time, LRCK edge to DOUT valid	–10		40	ns
t_r	Rising time of all signals			20	ns
t_f	Falling time of all signals			20	ns

(1) Timing measurement reference level is 1.4 V for input and 0.5 V_{DD} for output. Rising and falling time is measured from 10% to 90% of IN/OUT signal swing. Load capacitance of DOUT is 20 pF. $t_{(SCKI)}$ means SCKI period time.

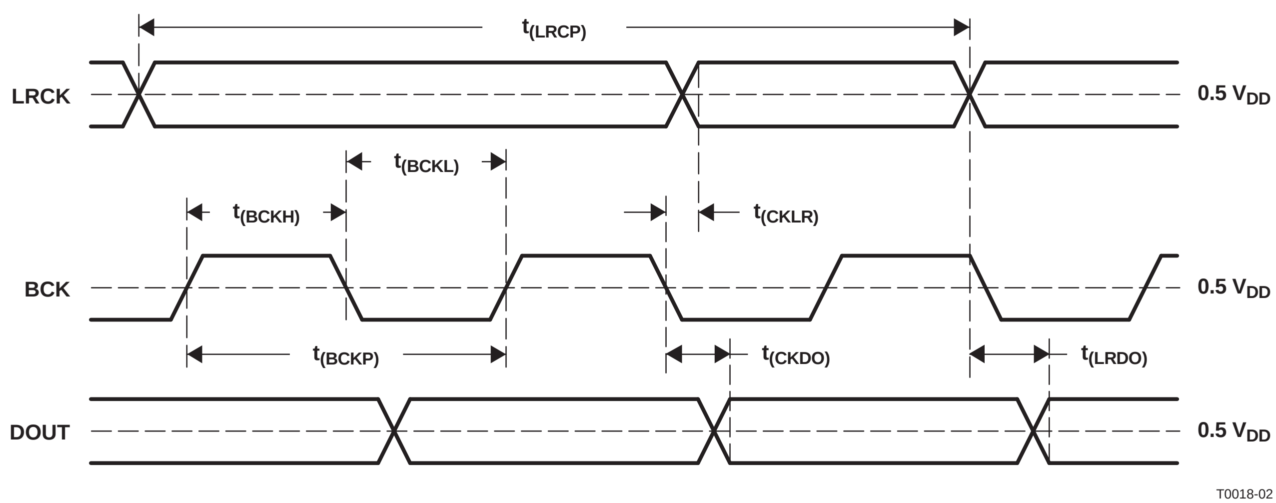


Figure 21. Audio Data Interface Timing (Master Mode: LRCK and BCK Work as Outputs)

Table 6. Audio Data Interface Master Mode Timing Requirements[1]

PARAMETER		MIN	TYP	MAX	UNIT
$t_{(BCKP)}$	BCK period	150	1/(64 f_S)	1000	ns
$t_{(BCKH)}$	BCK pulse duration, HIGH	65		600	ns
$t_{(BCKL)}$	BCK pulse duration, LOW	65		600	ns
$t_{(CKLR)}$	Delay time, BCK falling edge to LRCK valid	–10		20	ns
$t_{(LRCP)}$	LRCK period	10	1/f_S	65	µs
$t_{(CKDO)}$	Delay time, BCK falling edge to DOUT valid	–10		20	ns
$t_{(LRDO)}$	Delay time, LRCK edge to DOUT valid	–10		20	ns
t_r	Rising time of all signals			20	ns
t_f	Falling time of all signals			20	ns

(1) Timing measurement reference level is 1.4 V for input and 0.5 V_{DD} for output. Rising and falling time is measured from 10% to 90% of IN/OUT signal swing. Load capacitance of all signals is 20 pF.

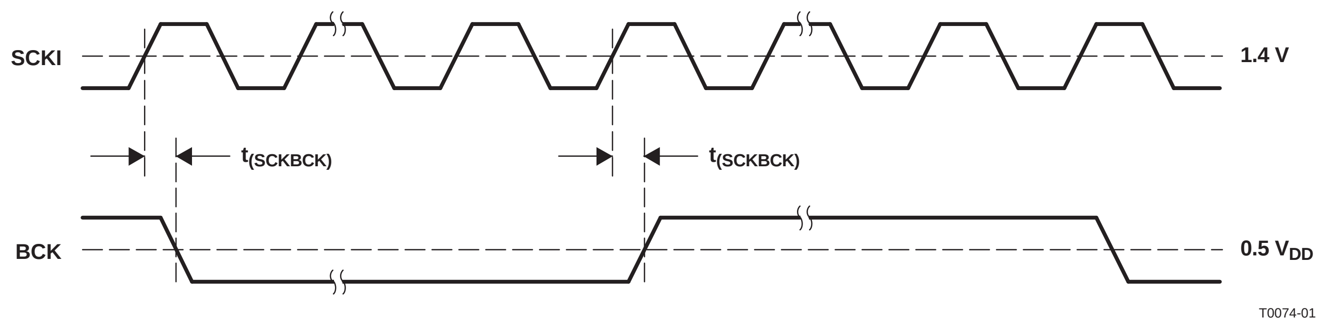


Figure 22. Audio Clock Interface Timing (Master Mode: BCK Works as Output)

Table 7. Audio Data Interface Master Mode BCK Timing Requirements[1]

PARAMETER		MIN	TYP	MAX	UNIT
$t_{(SCKBCK)}$	Delay time, SCKI rising edge to BCK edge	5		30	ns

(1) Timing measurement reference level is 1.4 V for input and 0.5 V_{DD} for output. Load capacitance of BCK is 20 pF.

7.4.2 Synchronization With Digital Audio System

In slave mode, the PCM1803A operates under LRCK, synchronized with system clock SCKI. The PCM1803A does not need a specific phase relationship between LRCK and SCKI, but does require the synchronization of LRCK and SCKI.

If the relationship between LRCK and SCKI changes more than ±6 BCKs for 64 BCK/frame (±5 BCKs for 48 BCK/frame) during one sample period due to LRCK or SCKI jitter, internal operation of the ADC halts within 1/f_S, and digital output is forced to zero data (BPZ code) until resynchronization between LRCK and SCKI occurs.

In case of changes less than ±5 BCKs for 64 BCK/frame (±4 BCKs for 48 BCK/frame), resynchronization does not occur and the previously explained digital output control and discontinuity do not occur.

Figure 23 illustrates the digital output response for loss of synchronization and resynchronization. During undefined data, the PCM1803A can generate some noise in the audio signal. Also, the transition of normal to undefined data and undefined or zero data to normal creates a discontinuity in the data of the digital output, which can generate some noise in the audio signal.

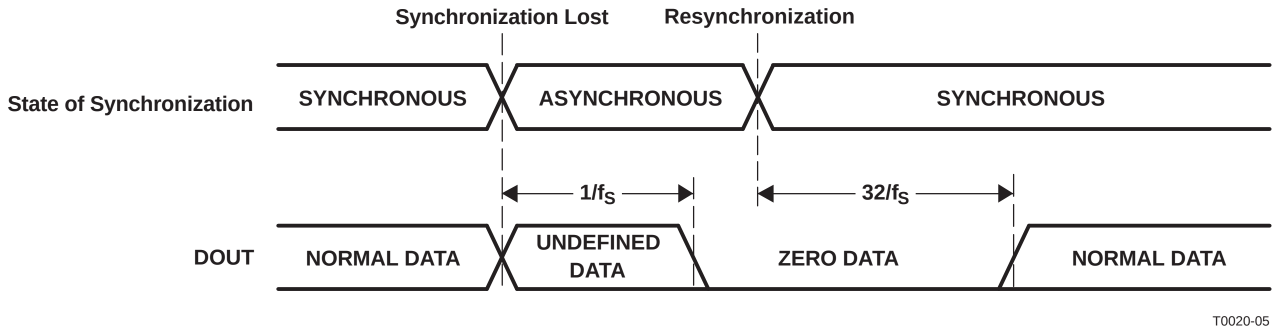


Figure 23. ADC Digital Output for Loss of Synchronization and Resynchronization

7.4.3 Power Down

$\overline{PDWN}$ (pin 7) controls operation of the entire ADC. During power-down mode, supply current for the analog portion is shut down and the digital portion is reset; also, DOUT (pin 12) is disabled. It is acceptable to halt the system clock during power-down mode so that power dissipation is minimized. The minimum LOW pulse duration on the $\overline{PDWN}$ pin is 100 ns.

TI recommends setting $\overline{PWDN}$ (pin 7) to LOW once to obtain stable analog performance when the sampling rate, interface mode, data format, or oversampling control is changed.

Table 8. Power-Down Control

$\overline{PWDN}$	POWER-DOWN MODE
LOW	Power-down mode
HIGH	Normal operation mode

7.4.4 HPF Bypass

The built-in function for DC-component rejection can be bypassed by BYPAS (pin 8) control. In bypass mode, the DC component of the input analog signal, internal DC offset, and so forth, also are converted and included in the digital output data.

Table 9. HPF Bypass Control

BYPAS	HPF (HIGH-PASS FILTER) MODE
LOW	Normal (no DC component in DOUT) mode
HIGH	Bypass (DC component in DOUT) mode

7.4.5 Oversampling Ratio Control

OSR (pin 16) controls the oversampling ratio of the delta-sigma modulator, ×64 or ×128. The ×128 mode is available for $f_S \leq 48$ kHz.

Table 10. Oversampling Control

OSR	OVERSAMPLING RATIO
LOW	×64
HIGH	×128 ($f_S \leq 48$ kHz)

8 Application and Implementation

NOTE

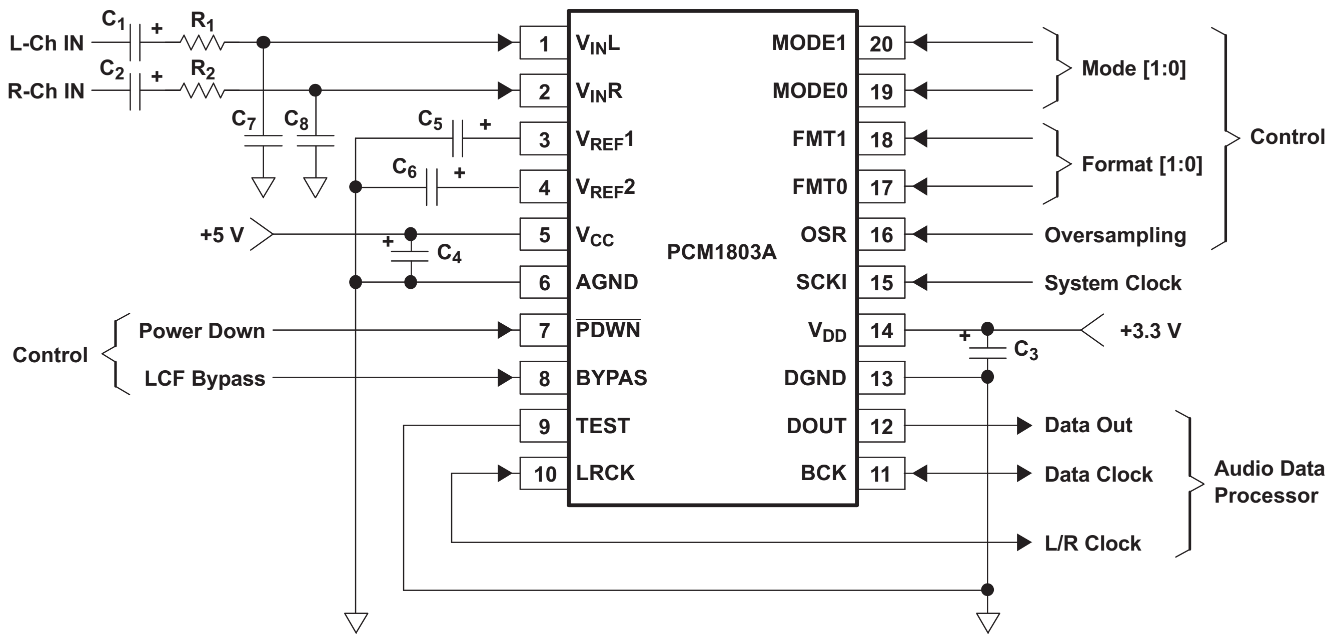
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The PCM1803A device is suitable for wide variety of cost-sensitive consumer applications requiring good performance and operation with a 5-V analog supply and 3.3-V digital supply.

8.2 Typical Application

Figure 24 illustrates a typical circuit connection diagram where the cutoff frequency of the input HPF is about 160 kHz.



A. C_1, C_2: A 1-µF electrolytic capacitor gives a 4-Hz (τ = 1 µF × 40 kΩ) cutoff frequency for the input HPF in normal operation and requires a power-on settling time with a 40-ms time constant during the power-on initialization period.

B. C_3, C_4: Bypass capacitors are 0.1-µF ceramic and 10-µF electrolytic, depending on layout and power supply.

C. C_5, C_6: Recommended capacitors are 0.1-µF ceramic and 10-µF electrolytic.

D. C_7, C_8, R_1, R_2: A 0.01-µF film-type capacitor and 100-Ω resistor give a 160-kHz (τ = 0.01 µF × 100 Ω) cutoff frequency for the anti-aliasing filter in normal operation.

Figure 24. Typical Application Diagram

Typical Application (continued)

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 11 as the input parameters.

Table 11. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Analog Input Voltage Range	0 V_{p-p} to 3 V_{p-p}
Output	PCM audio data
System Clock Input Frequency	2.048 MHz to 49.152 MHz
Output Sampling Frequency	8 kHz to 96 kHz
Power Supply	3.3 V and 5 V

8.2.2 Detailed Design Procedure

8.2.2.1 Control Pins

The control pins such as the FMT, MODE, OSR, and BYPASS can be controlled by tying up to VDD, down to GND, or driven with GPIO from the DSP or audio processor.

8.2.2.2 DSP or Audio Processor

In this application a DSP or audio processor is acting as the audio master, and the PCM1803A is acting as the audio slave. This means the DSP or audio processor must be able to output audio clocks that the PCM1803A can use to process audio signals.

8.2.2.3 Input Filters

For the analog input circuit an AC coupling capacitor must be placed in series with the input. This removes the DC component of the input signal. An RC filter can also be implemented to filter out of band noise to reduce aliasing. Equation 1 can be used to calculate the cutoff frequency of the optional RC filter for the input.

$$f_c = \frac{1}{2\pi RC} \tag{1}$$

8.2.3 Application Curve

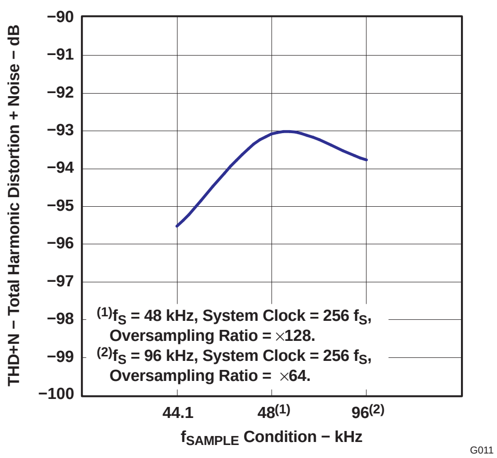


Figure 25. Total Harmonic Distortion + Noise vs f_{SAMPLE} Condition

9 Power Supply Recommendations

The PCM1803A requires a 5-V nominal supply and a 3.3-V nominal supply. The 5-V supply is for the analog circuitry powered by the VCC pin. The 3.3-V supply is for the digital circuitry powered by the VDD pin. The decoupling capacitors for the power supplies must be placed close to the device terminals.

10 Layout

10.1 Layout Guidelines

10.1.1 V_{CC}, V_{DD} Pins

The digital and analog power-supply lines to the PCM1803A must be bypassed to the corresponding ground pins with 0.1-µF ceramic and 10-µF electrolytic capacitors, as close to the pins as possible, to maximize the dynamic performance of the ADC.

10.1.2 AGND, DGND Pins

To maximize the dynamic performance of the PCM1803A, the analog and digital grounds are not connected internally. These grounds must have low impedance to avoid digital noise feeding back into the analog ground. Therefore, they must be connected directly to each other under the part to reduce potential noise problems.

10.1.3 $V_{IN}L$, $V_{IN}R$ Pins

The $V_{IN}L$ and $V_{IN}R$ pins need a simple external RC filter (f_C = 160 kHz) as an antialiasing filter to remove out-of-band noise from the audio band. If the input signal includes noise with a frequency near the oversampling frequency (64 f_S or 128 f_S), the noise is folded into the baseband (audio band) signal through A-to-D conversion. The recommended R value is 100 Ω. Film-type capacitors of 0.01 µF must be placed as close as possible to the $V_{IN}L$ and $V_{IN}R$ pins and must be terminated to GND as close as possible to the AGND pin to maximize the dynamic performance of ADC, by suppressing kickback noise from the PCM1803A.

10.1.4 $V_{REF}1$ Pin

TI recommends a 0.1-µF ceramic capacitor and 10-µF electrolytic capacitor between $V_{REF}1$ and AGND to ensure low source impedance of the ADC references. These capacitors must be placed as close as possible to the $V_{REF}1$ pin to reduce dynamic errors on the ADC reference.

10.1.5 $V_{REF}2$ Pin

The differential voltage between $V_{REF}2$ and AGND sets the analog input full-scale range. A 0.1-µF ceramic capacitor and 10-µF electrolytic capacitor are recommended between $V_{REF}2$ and AGND. These capacitors must be placed as close as possible to the $V_{REF}2$ pin to reduce dynamic errors on the ADC reference.

10.1.6 DOUT Pin

The DOUT pin has enough load drive capability, but if the DOUT line is long, placing a buffer near the PCM1803A and minimizing load capacitance is recommended to minimize the digital-analog crosstalk and maximize the dynamic performance of the ADC.

10.2 Layout Example

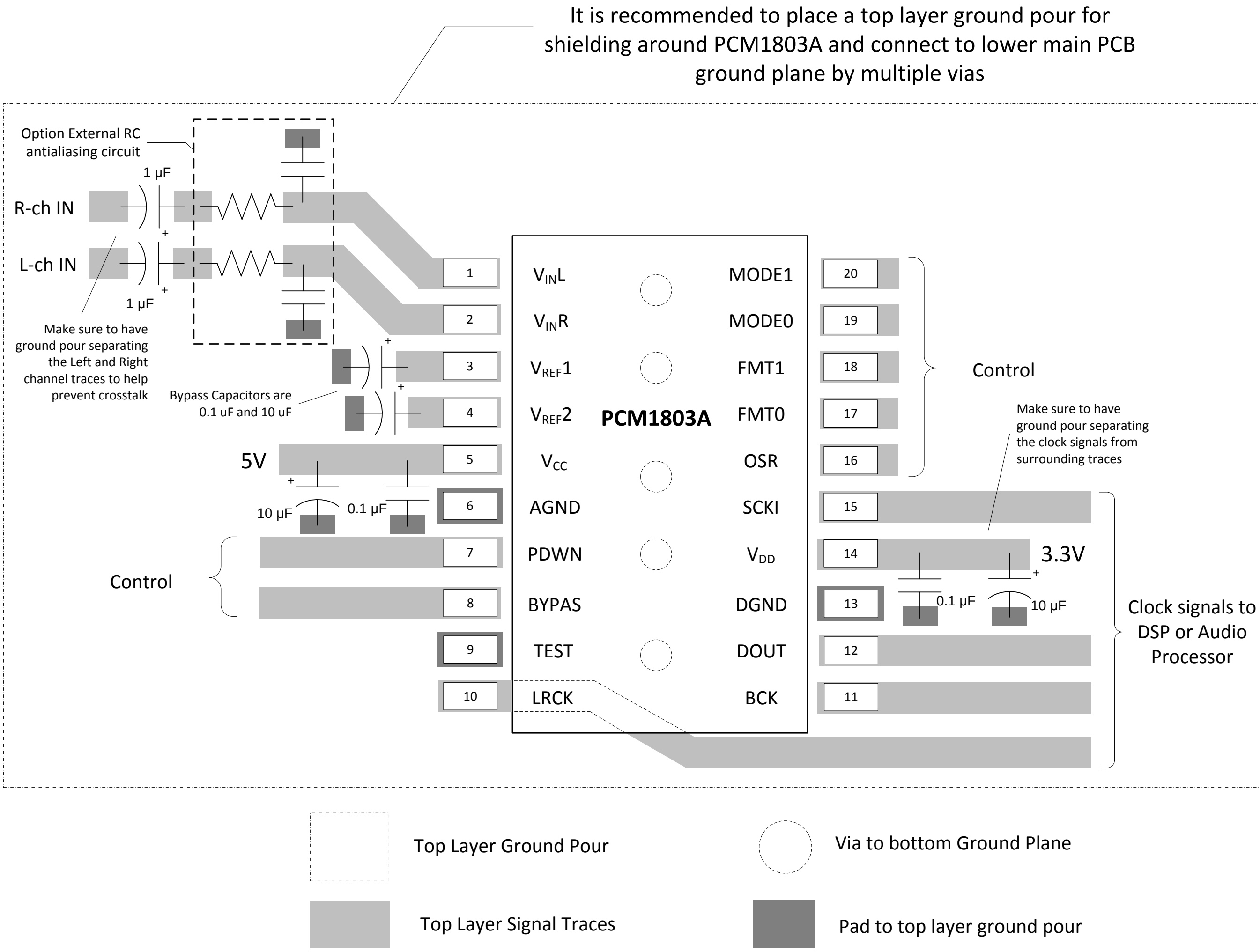


Figure 26. Layout Recommendation

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
System Two, Audio Precision are trademarks of Audio Precision, Inc.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCM1803ADB	ACTIVE	SSOP	DB	20	65	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCM1803A	Samples
PCM1803ADBG4	ACTIVE	SSOP	DB	20	65	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCM1803A	Samples
PCM1803ADBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCM1803A	Samples
PCM1803ADBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCM1803A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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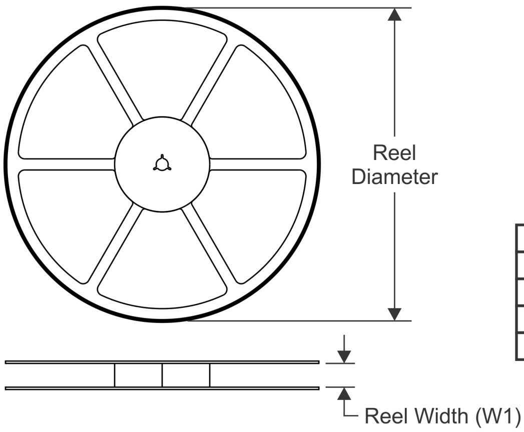
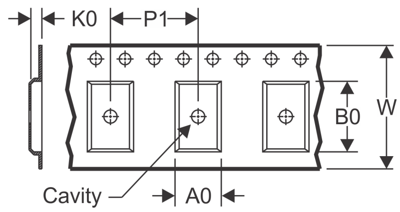
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

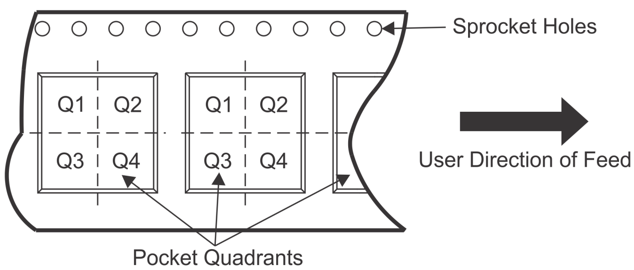


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

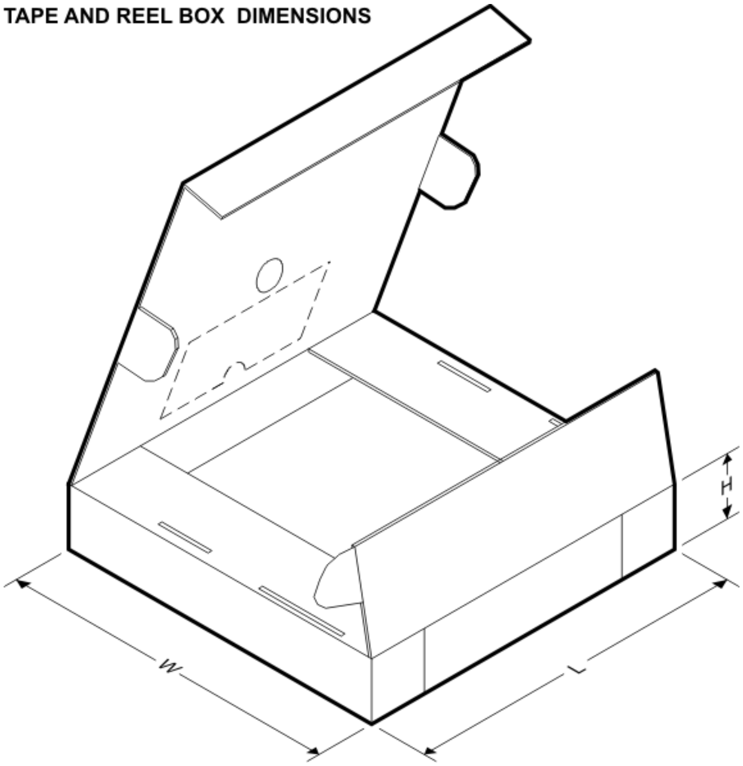
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM1803ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
PCM1803ADBR	SSOP	DB	20	2000	330.0	17.4	8.5	7.6	2.4	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

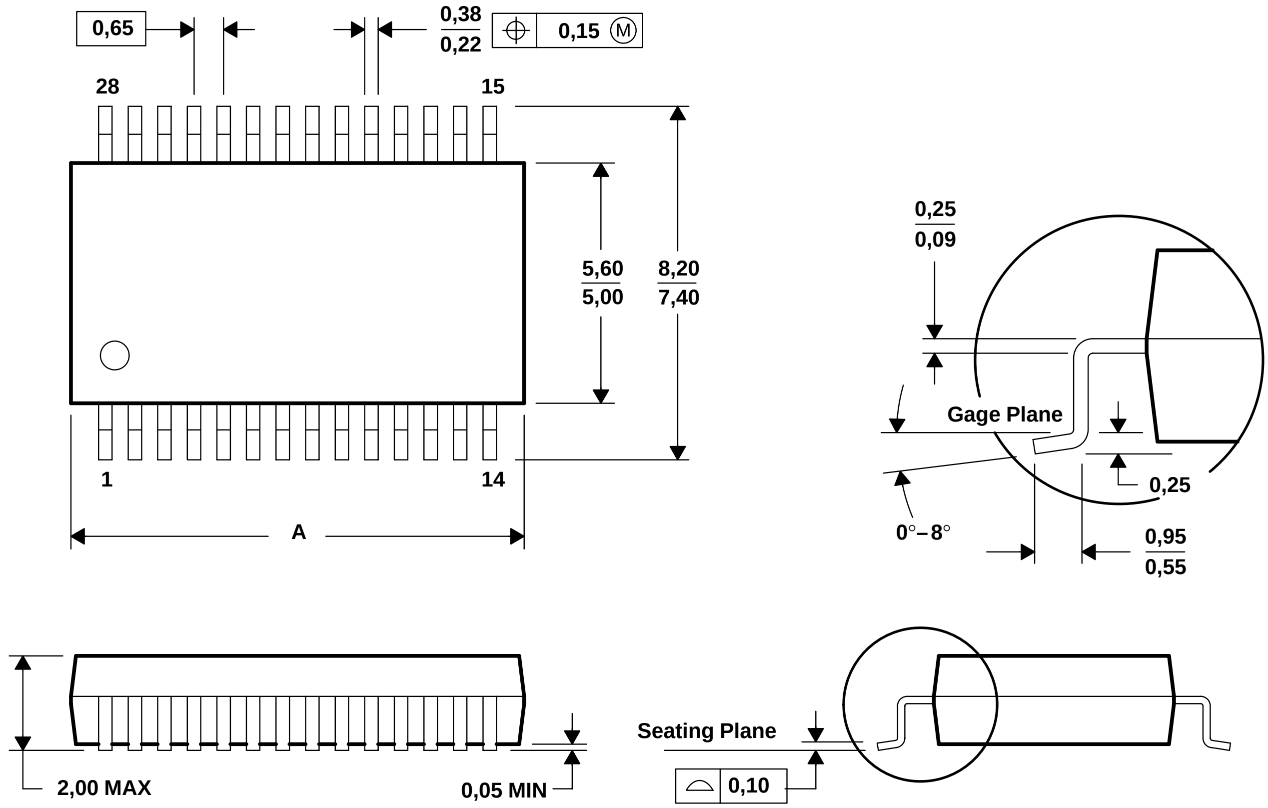


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM1803ADBR	SSOP	DB	20	2000	367.0	367.0	38.0
PCM1803ADBR	SSOP	DB	20	2000	336.6	336.6	28.6

DB (R-PDSO-G**) PLASTIC SMALL-OUTLINE

28 PINS SHOWN



PINS ** / DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150