

# TPS54427 4.5-V to 18-V Input, 4-A Output Single Synchronous Step-Down Switcher With Integrated FET

## 1 Features

- D-CAP2™ Mode Enables Fast Transient Response
- Low Output Ripple and Allows Ceramic Output Capacitor
- Wide  $V_{IN}$  Input Voltage Range: 4.5 V to 18 V
- Output Voltage Range: 0.76 V to 7.0 V
- Highly Efficient Integrated FETs Optimized for Lower Duty Cycle Applications
  - 70 m $\Omega$  (High Side) and 53 m $\Omega$  (Low Side)
- High Efficiency, Less Than 10  $\mu$ A at Shutdown
- High Initial Bandgap Reference Accuracy
- Adjustable Soft Start
- Pre-Biased Soft Start
- 650-kHz Switching Frequency ( $f_{sw}$ )
- Cycle by Cycle Over Current Limit

## 2 Applications

- Wide Range of Applications for Low Voltage System
  - Digital TV Power Supply
  - High Definition Blu-ray Disc™ Players
  - Networking Home Terminal
  - Digital Set Top Box (STB)

## 3 Description

The TPS54427 is an adaptive on-time D-CAP2™ mode synchronous buck converter. The TPS54427 enables system designers to complete the suite of various end equipment's power bus regulators with a cost effective, low component count, low standby current solution.

The main control loop for the TPS54427 uses the D-CAP2™ mode control which provides a fast transient response with no external compensation components.

The TPS54427 also has a proprietary circuit that enables the device to adopt to both low equivalent series resistance (ESR) output capacitors, such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors.

The device operates from 4.5-V to 18-V  $V_{IN}$  input. The output voltage can be programmed between 0.76 V and 7 V.

The device also features an adjustable soft start time.

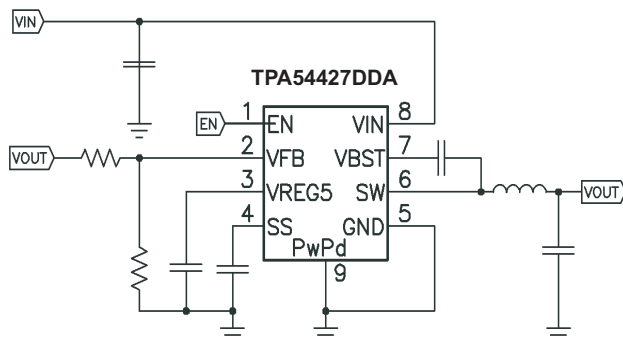
The TPS54427 is available in the 8-pin DDA package and 10-pin DRC, and is designed to operate from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

### Device Information<sup>(1)</sup>

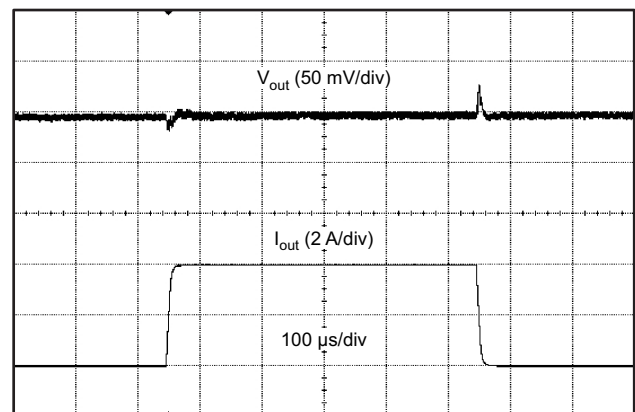
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS54427	SO PowerPAD™ (8)	4.89 mm x 3.90 mm
	VSON (10)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Simplified Schematic



### TPS54427 Transient Response



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	<b>8 Application and Implementation</b> .....	<b>11</b>
<b>2 Applications</b> .....	<b>1</b>	8.1 Application Information.....	11
<b>3 Description</b> .....	<b>1</b>	8.2 Typical Application .....	11
<b>4 Revision History</b> .....	<b>2</b>	<b>9 Power Supply Recommendations</b> .....	<b>15</b>
<b>5 Pin Configuration and Functions</b> .....	<b>3</b>	<b>10 Layout</b> .....	<b>15</b>
<b>6 Specifications</b> .....	<b>4</b>	10.1 Layout Guidelines .....	15
6.1 Absolute Maximum Ratings .....	4	10.2 Layout Examples.....	16
6.2 ESD Ratings.....	4	10.3 Thermal Considerations .....	17
6.3 Recommended Operating Conditions.....	4	<b>11 Device and Documentation Support</b> .....	<b>19</b>
6.4 Thermal Information .....	5	11.1 Device Support.....	19
6.5 Electrical Characteristics.....	5	11.2 Documentation Support .....	19
6.6 Typical Characteristics .....	6	11.3 Community Resources.....	19
<b>7 Detailed Description</b> .....	<b>8</b>	11.4 Trademarks .....	19
7.1 Overview .....	8	11.5 Electrostatic Discharge Caution.....	19
7.2 Functional Block Diagram .....	8	11.6 Glossary .....	19
7.3 Feature Description.....	8	<b>12 Mechanical, Packaging, and Orderable Information</b> .....	<b>19</b>
7.4 Device Functional Modes.....	10		

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision B (October 2015) to Revision C Page

- Deleted (SWIFT™) from the data sheet title .....

1

### Changes from Revision A (June 2013) to Revision B Page

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section .....
- Added the DRC-10 Pin package pin out .....

1

3

### Changes from Original (November 2011) to Revision A Page

- Added "and 10-pin DRC" to the DESCRIPTION .....
- Added the DRC-10 pin Package to the ORDERING INFORMATION table.....
- Changed the VBST(vs SW) MAX value From: 5.7V to 6V in the ROC table.....
- Changed  $V_{FB}$  input current MAX value From:  $\pm 0.15 \mu A$  To:  $\pm 0.1 \mu A$  .....
- Added High side switch resistance (DRC) .....
- Changed [Figure 9](#).....
- Added [Figure 9](#).....
- Added [Figure 23](#).....

1

1

4

5

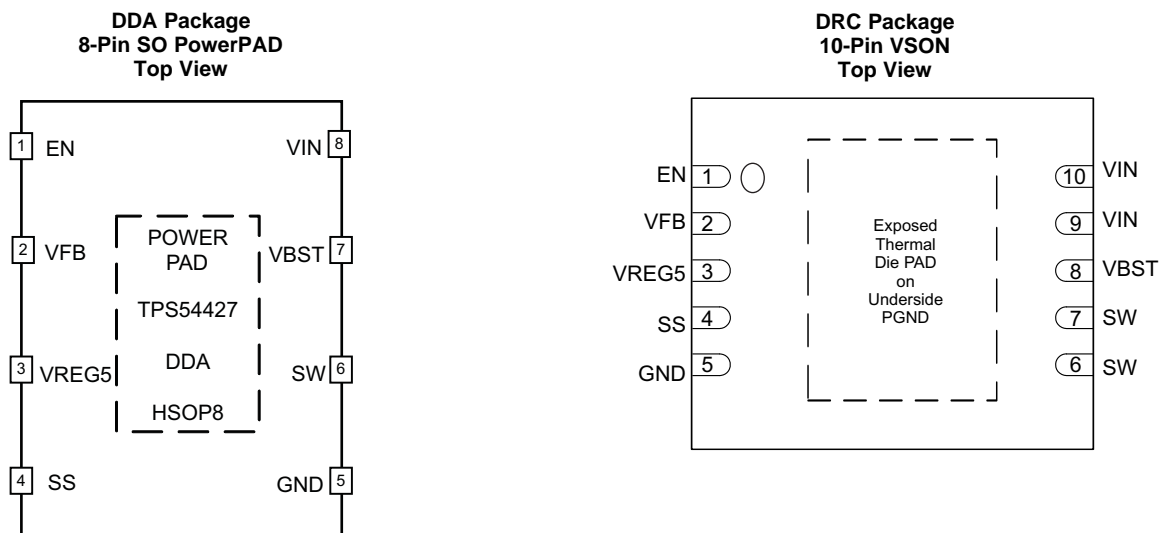
5

7

7

17

## 5 Pin Configuration and Functions



### Pin Functions

NAME	PIN		DESCRIPTION
	DDA	DRC	
EN	1	1	Enable input control. Active high and must be pulled up to enable the device.
VFB	2	2	Converter feedback input. Connect to output voltage with feedback resistor divider.
VREG5	3	3	5.5 V power supply output. A capacitor (typical 1 $\mu$ F) should be connected to GND. VREG5 is not active when EN is low.
SS	4	4	Soft-start control. An external capacitor should be connected to GND.
GND	5	5	Ground pin. Power ground return for switching circuit. Connect sensitive SS and VFB returns to GND at a single point.
SW	6	6, 7	Switch node connection between high-side NFET and low-side NFET.
VBST	7	8	Supply input for the high-side FET gate drive circuit. Connect 0.1 $\mu$ F capacitor between VBST and SW pins. An internal diode is connected between VREG5 and VBST.
VIN	8	9, 10	Input voltage supply pin.
Exposed Thermal Pad	Back side		Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Must be connected to GND.
		Back side	Thermal pad of the package. PGND power ground return of internal low-side FET. Must be soldered to achieve appropriate dissipation.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Input voltage	VIN, EN	-0.3	20	V
	VBST	-0.3	26	V
	VBST (10 ns transient)	-0.3	28	V
	VBST (vs SW)	-0.3	6.5	V
	VFB, SS	-0.3	6.5	V
	SW	-2	20	V
	SW (10 ns transient)	-3	22	V
Output voltage	VREG5	-0.3	6.5	V
	GND	-0.3	0.3	V
Voltage from GND to thermal pad, V <sub>diff</sub>		-0.2	0.2	V
Operating junction temperature, T <sub>J</sub>		-40	150	°C
Storage temperature, T <sub>stg</sub>		-55	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V <sub>IN</sub>	Supply input voltage	4.5	18	V	
V <sub>I</sub>	Input voltage	VBST	-0.1	24	V
		VBST (10 ns transient)	-0.1	27	
		VBST(vs SW)	-0.1	6	
		SS	-0.1	5.7	
		EN	-0.1	18	
		VFB	-0.1	5.5	
		SW	-1.8	18	
		SW (10 ns transient)	-3	21	
	GND	-0.1	0.1		
V <sub>O</sub>	Output voltage	VREG5	-0.1	5.7	V
I <sub>O</sub>	Output current	I <sub>VREG5</sub>	0	10	mA
T <sub>A</sub>	Operating free-air temperature	-40	85	°C	
T <sub>J</sub>	Operating junction temperature	-40	150	°C	

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS54427		UNIT
		DDA [SO PowerPAD]	DRC [VSON]	
		8 PINS	10 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	42.1	43.2	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	50.9	53.8	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	31.8	18.2	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	5	0.6	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	13.5	18.3	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	7.1	4.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

## 6.5 Electrical Characteristics

over operating free-air temperature range, V<sub>IN</sub> = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY CURRENT</b>						
I <sub>VIN</sub>	Operating - non-switching supply current	V <sub>IN</sub> current, T <sub>A</sub> = 25°C, EN = 5 V, V <sub>FB</sub> = 0.8 V		950	1400	μA
I <sub>VINSDN</sub>	Shutdown supply current	V <sub>IN</sub> current, T <sub>A</sub> = 25°C, EN = 0 V		3.0	10	μA
<b>LOGIC THRESHOLD</b>						
V <sub>ENH</sub>	EN high-level input voltage	EN	1.6			V
V <sub>ENL</sub>	EN low-level input voltage	EN			0.6	V
R <sub>EN</sub>	EN pin resistance to GND	V <sub>EN</sub> = 12 V	225	450	900	kΩ
<b>V<sub>FB</sub> VOLTAGE AND DISCHARGE RESISTANCE</b>						
V <sub>FBTH</sub>	V <sub>FB</sub> threshold voltage	T <sub>A</sub> = 25°C, V <sub>O</sub> = 1.05 V, continuous mode mode	757	765	773	mV
		T <sub>A</sub> = -40°C to 85°C, V <sub>O</sub> = 1.05 V, continuous mode mode <sup>(1)</sup>	751	765	779	
I <sub>VFB</sub>	V <sub>FB</sub> input current	V <sub>FB</sub> = 0.8 V, T <sub>A</sub> = 25°C		0	±0.1	μA
<b>V<sub>REG5</sub> OUTPUT</b>						
V <sub>VREG5</sub>	V <sub>REG5</sub> output voltage	T <sub>A</sub> = 25°C, 6.0 V < V <sub>IN</sub> < 18 V, 0 < I <sub>VREG5</sub> < 5 mA	5.2	5.5	5.7	V
V <sub>LN5</sub>	Line regulation	6 V < V <sub>IN</sub> < 18 V, I <sub>VREG5</sub> = 5 mA			25	mV
V <sub>LD5</sub>	Load regulation	0 mA < I <sub>VREG5</sub> < 5 mA			100	mV
I <sub>VREG5</sub>	Output current	V <sub>IN</sub> = 6 V, V <sub>REG5</sub> = 4.0 V, T <sub>A</sub> = 25°C		60		mA
<b>MOSFET</b>						
R <sub>DS(on)h</sub>	High side switch resistance (DDA)	25°C, V <sub>BST</sub> - SW = 5.5 V	70			mΩ
	High side switch resistance (DRC)		74			
R <sub>DS(on)l</sub>	Low side switch resistance	25°C	53			mΩ
<b>CURRENT LIMIT</b>						
I <sub>ocl</sub>	Current limit	L out = 1.5 μH <sup>(1)</sup>	4.6	5.3	6.8	A

(1) Not production tested.

### Electrical Characteristics (continued)

over operating free-air temperature range,  $V_{IN} = 12\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>THERMAL SHUTDOWN</b>						
$T_{SDN}$	Thermal shutdown threshold	Shutdown temperature <sup>(1)</sup>	170			°C
		Hysteresis <sup>(1)</sup>	35			
<b>ON-TIME TIMER CONTROL</b>						
$t_{ON}$	On time	$V_{IN} = 12\text{ V}, V_O = 1.05\text{ V}$	150			ns
$t_{OFF(MIN)}$	Minimum off time	$T_A = 25^\circ\text{C}, V_{FB} = 0.7\text{ V}$	260	310	ns	
<b>SOFT START</b>						
$I_{SSC}$	SS charge current	$V_{SS} = 1\text{ V}$	4.2	6.0	7.8	μA
$I_{SSD}$	SS discharge current	$V_{SS} = 0.5\text{ V}$	0.1	0.2	mA	
<b>UVLO</b>						
UVLO	UVLO threshold	Wake up $V_{REG5}$ voltage	3.45	3.75	4.05	V
		Hysteresis $V_{REG5}$ voltage	0.19	0.32	0.45	

### 6.6 Typical Characteristics

$V_{IN} = 12\text{ V}, T_A = 25^\circ\text{C}$  (unless otherwise noted)

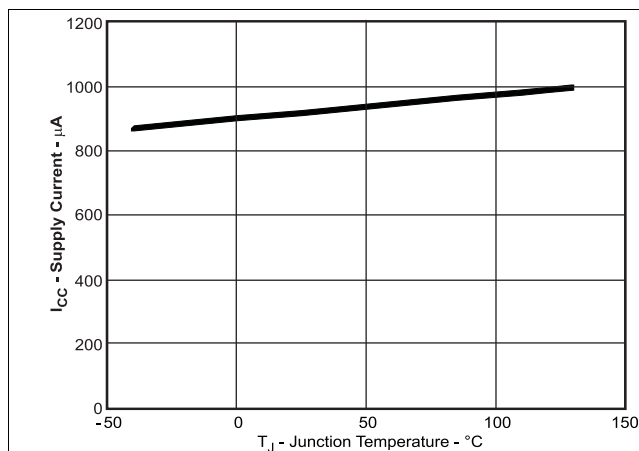


Figure 1. VIN Current vs Junction Temperature

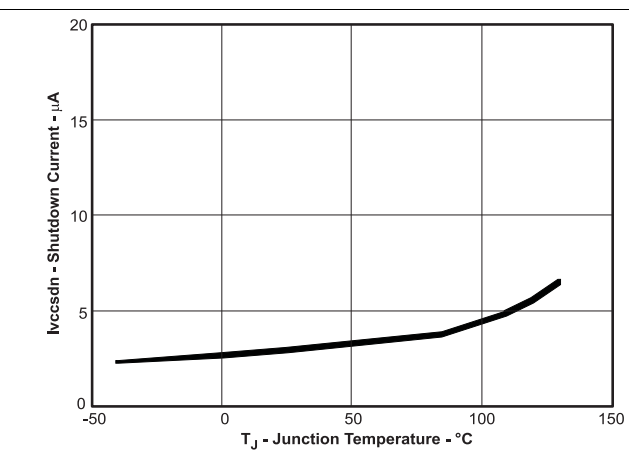


Figure 2. VIN Shutdown Current vs Junction Temperature

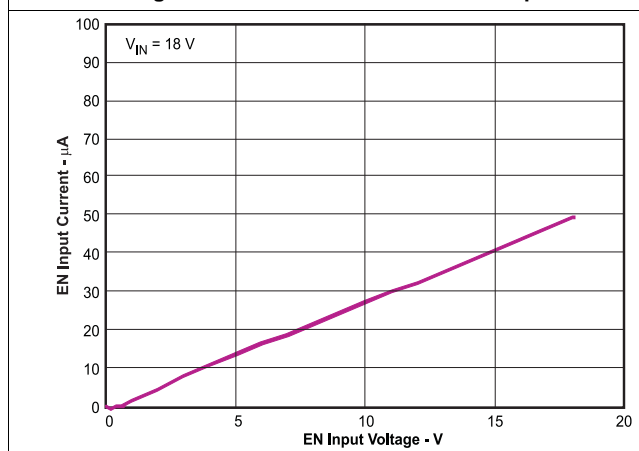


Figure 3. EN Current vs EN Voltage

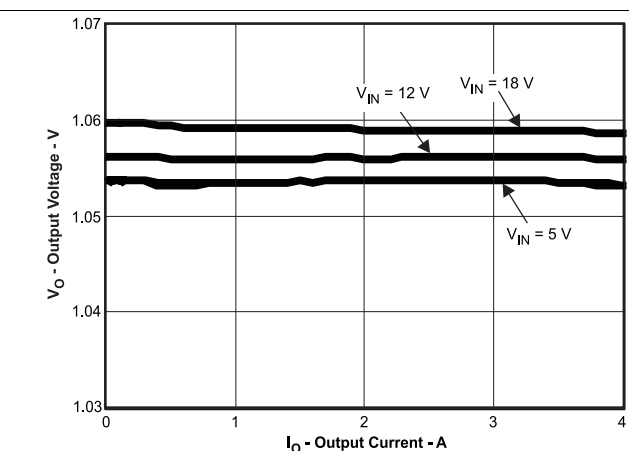


Figure 4. 1.05-V Output Voltage vs Output Current

Typical Characteristics (continued)

VIN = 12 V, TA = 25°C (unless otherwise noted)

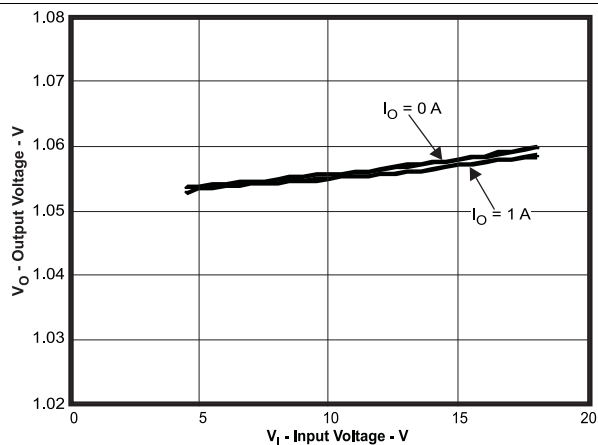


Figure 5. 1.05-V Output Voltage vs Vin Voltage

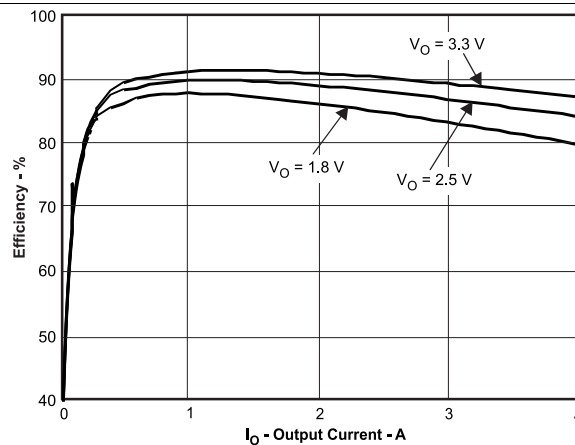


Figure 6. Efficiency vs Output Current

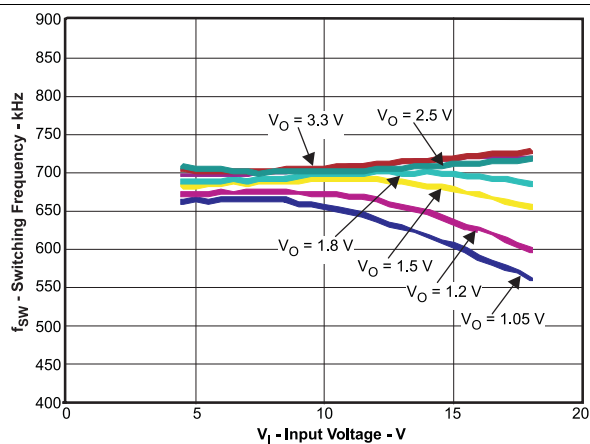


Figure 7. Switching Frequency vs Input Voltage

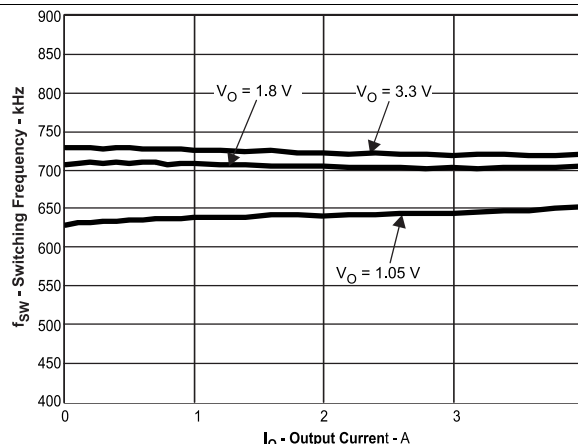


Figure 8. Switching Frequency vs Output Current

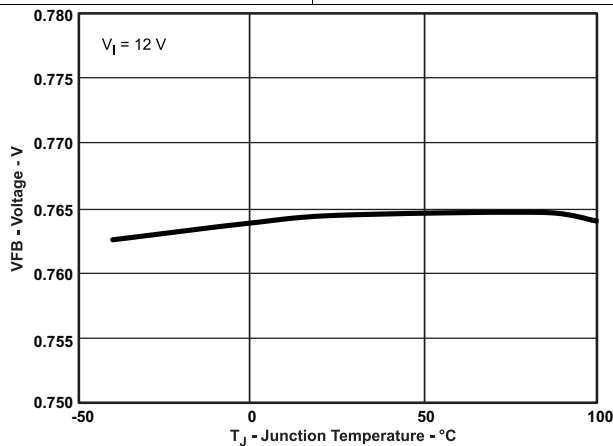


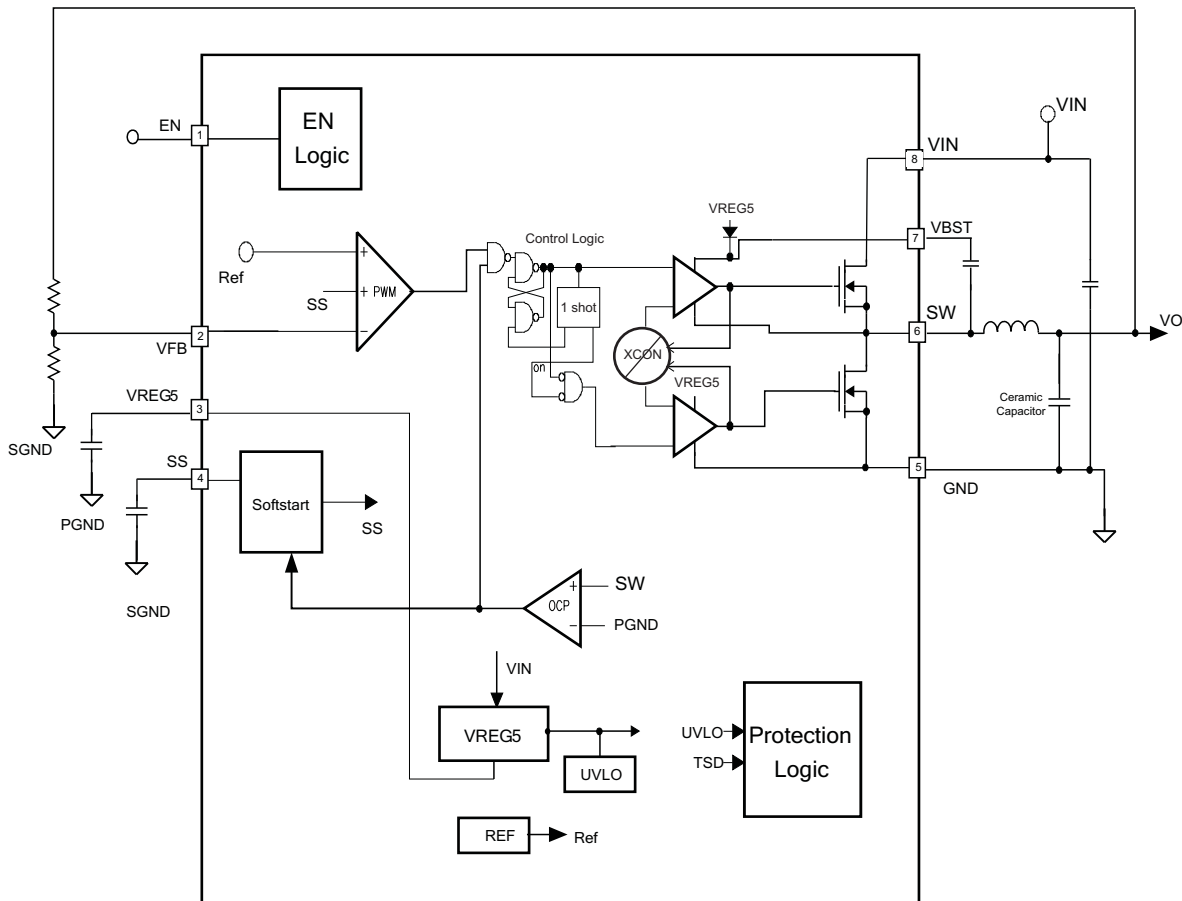
Figure 9. VFB Voltage vs Junction Temperature

## 7 Detailed Description

### 7.1 Overview

The TPS54427 is a 4-A synchronous step-down (buck) converter with two integrated N-channel MOSFETs. It operates using D-CAP2™ mode control. The fast transient response of D-CAP2™ control reduces the output capacitance required to meet a specific level of performance. Proprietary internal circuitry allows the use of low ESR output capacitors including ceramic and special polymer types.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 PWM Operation

The main control loop of the TPS54427 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ mode control. D-CAP2™ mode control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot is set by the converter input voltage, VIN, and the output voltage, VO, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2™ mode control.



## Feature Description (continued)

### 7.3.2 PWM Frequency and Adaptive On-Time Control

TPS54427 uses an adaptive on-time control scheme and does not have a dedicated on board oscillator. The TPS54427 runs with a pseudo-constant frequency of 650 kHz by using the input voltage and output voltage to set the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage, therefore, when the duty ratio is  $V_{OUT}/V_{IN}$ , the frequency is constant.

### 7.3.3 Soft Start and Pre-Biased Soft Start

The soft start function is adjustable. When the EN pin becomes high, 6- $\mu$ A current begins charging the capacitor which is connected from the SS pin to GND. Smooth control of the output voltage is maintained during start up. The equation for the slow start time is shown in [Equation 1](#). VFB voltage is 0.765 V and SS pin source current is 6- $\mu$ A.

$$T_{ss}(ms) = \frac{C6(nF) \times V_{fb} \times 1.1}{I_{ss}(\mu A)} = \frac{C6(nF) \times 0.765 \times 1.1}{6} \quad (1)$$

The TPS54427 contains a unique circuit to prevent current from being pulled from the output during startup if the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft start becomes greater than feedback voltage VFB), the controller slowly activates synchronous rectification by starting the first low side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by  $(1-D)$ , where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-bias output, and ensure that the out voltage (VO) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased start-up to normal mode operation.

### 7.3.4 Current Protection

The output overcurrent protection (OCP) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored by measuring the low-side FET switch voltage between the SW pin and GND. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by  $V_{in}$ ,  $V_{out}$ , the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current  $I_{OUT}$ . The TPS54427 constantly monitors the low-side FET switch voltage, which is proportional to the switch current, during the low-side on-time. If the measured voltage is above the voltage proportional to the current limit, an internal counter is incremented per each SW cycle and the converter maintains the low-side switch on until the measured voltage is below the voltage corresponding to the current limit at which time the switching cycle is terminated and a new switching cycle begins. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner. If the over current condition exists for 7 consecutive switching cycles, the internal OCL threshold is set to a lower level, reducing the available output current. When a switching cycle occurs where the switch current is not above the lower OCL threshold, the counter is reset and the OCL limit is returned to the higher value.

There are some important considerations for this type of over-current protection. The load current one half of the peak-to-peak inductor current higher than the over-current threshold. Also when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output voltage to fall. When the over current condition is removed, the output voltage will return to the regulated value. This protection is non-latching.

### 7.3.5 UVLO Protection

Undervoltage lock out protection (UVLO) monitors the voltage of the VREG5 pin. When the VREG5 voltage is lower than UVLO threshold voltage, the TPS54427 is shut off. This protection is non-latching.

### 7.3.6 Thermal Shutdown

TPS54427 monitors the temperature of itself. If the temperature exceeds the threshold value (typically 170°C), the device is shut off. This is non-latch protection.

## 7.4 Device Functional Modes

### 7.4.1 Normal Operation

When the input voltage is above the UVLO threshold and the EN voltage is above the enable threshold, the TPS54427 operates in normal switching mode. Normal continuous conduction mode (CCM) occurs when the minimum switch current is above 0 A. In CCM the TPS54427 operates at a quasi-fixed frequency of 650 kHz.

### 7.4.2 Forced CCM Operation

When the TPS54427 is in normal CCM operating mode and switch current falls below 0 A, the device begins operating in forced CCM.

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The TPS54427 is used as a step converter that convert an voltage of 4.5 V to 18 V to a lower voltage. WEBENCH® software is available to aid in the design and analysis of circuits.

### 8.2 Typical Application

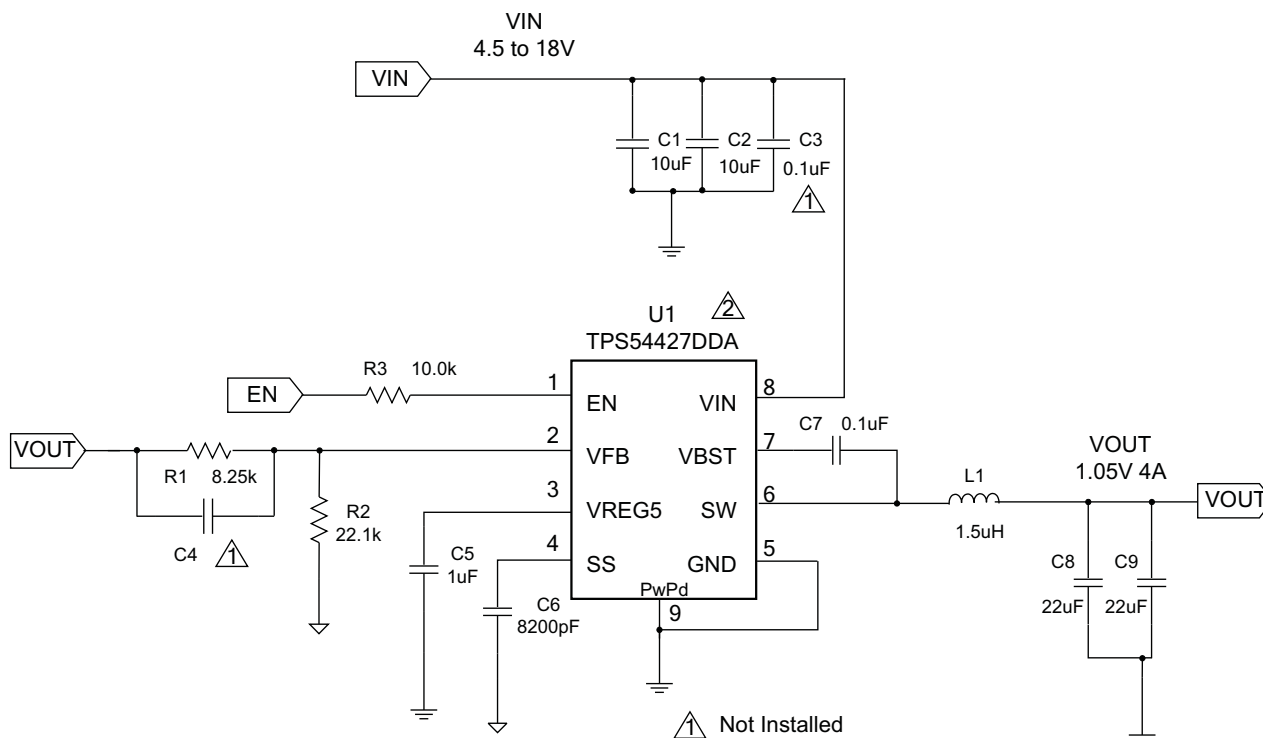


Figure 10. Typical Application Schematic

#### 8.2.1 Design Requirements

Table 1 shows the input and output connections.

Table 1. TPS54427 Performance Specifications Summary

SPECIFICATIONS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range, $V_{IN}$		4.5	12	18	V
Output voltage, $V_{OUT}$			1.05		V
Operating frequency	$V_{IN} = 12\text{ V}$ , $I_O = 4\text{ A}$		650		kHz
Output current range		0		4	A
Output ripple voltage	$V_{IN} = 12\text{ V}$ , $I_O = 4\text{ A}$		15		mV <sub>PP</sub>

## 8.2.2 Detailed Design Procedure

To begin the design process, you must know a few application parameters:

- Input voltage range
- Output voltage
- Output current
- Output voltage ripple
- Input voltage ripple

### 8.2.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. It is recommended to use 1% tolerance or better divider resistors. Start by using [Equation 2](#) to calculate  $V_{OUT}$ .

To improve efficiency at very light loads consider using larger value resistors, too high of resistance will be more susceptible to noise and voltage errors from the VFB input current will be more noticeable.

$$V_{OUT} = 0.765 \times \left( 1 + \frac{R1}{R2} \right) \quad (2)$$

### 8.2.2.2 Output Filter Selection

The output filter used with the TPS54427 is an LC circuit. This LC filter has double pole at:

$$F_p = \frac{1}{2\pi \sqrt{L_{OUT} \times C_{OUT}}} \quad (3)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS54427. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP2™ introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor selected for the output filter must be selected so that the double pole of [Equation 3](#) is located below the high frequency zero but close enough that the phase boost provided by the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in [Table 2](#).

**Table 2. Recommended Component Values**

OUTPUT VOLTAGE (V)	R1 (kΩ)	R2 (kΩ)	C4 (pF) <sup>(1)</sup>	L1 (μH)	C8 + C9 (μF)
1	6.81	22.1		1.5	22 - 68
1.05	8.25	22.1		1.5	22 - 68
1.2	12.7	22.1		1.5	22 - 68
1.5	21.5	22.1		1.5	22 - 68
1.8	30.1	22.1	5 - 22	2.2	22 - 68
2.5	49.9	22.1	5 - 22	2.2	22 - 68
3.3	73.2	22.1	5 - 22	2.2	22 - 68
5	124	22.1	5 - 22	3.3	22 - 68
6.5	165	22.1	5 - 22	3.3	22 - 68

(1) Optional

For higher output voltages at or above 1.8 V, additional phase boost can be achieved by adding a feed forward capacitor (C4) in parallel with R1.

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using [Equation 4](#), [Equation 5](#) and [Equation 6](#). The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current. Use 650 kHz for  $f_{SW}$ .

Use 650 kHz for  $f_{SW}$ . Make sure the chosen inductor is rated for the peak current of [Equation 5](#) and the RMS current of [Equation 6](#).

$$I_{P-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \quad (4)$$

$$I_{PEAK} = I_O + \frac{I_{P-P}}{2} \quad (5)$$

$$I_{L(O,RMS)} = \sqrt{I_O^2 + \frac{1}{12} I_{P-P}^2} \quad (6)$$

For this design example, the calculated peak current is 4.51 A and the calculated RMS current is 4.01 A. The inductor used is a TDK SPM6530-1R5M100 with a peak current rating of 11.5 A and an RMS current rating of 11 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS54427 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 22µF to 68µF. Use [Equation 7](#) to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \quad (7)$$

For this design two TDK C3216X5R0J226M 22µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.286A and each output capacitor is rated for 4A.

### 8.2.2.3 Input Capacitor Selection

The TPS54427 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10 µF is recommended for the decoupling capacitor. An additional 0.1 µF capacitor (C3) from pin 8 to ground is optional to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

### 8.2.2.4 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the VBST to SW pin for proper operation. It is recommended to use a ceramic capacitor.

### 8.2.2.5 VREG5 Capacitor Selection

A 1-µF ceramic capacitor must be connected between the VREG5 to GND pin for proper operation. It is recommended to use a ceramic capacitor.

## 8.2.3 Application Curves

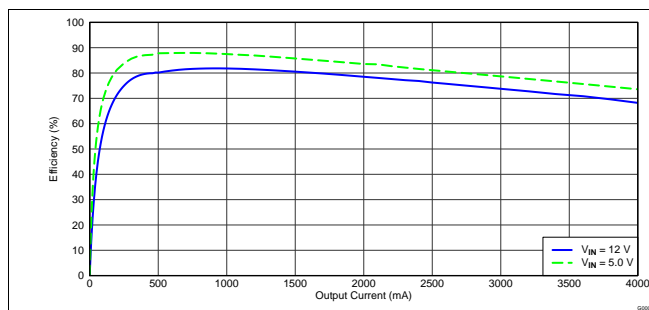


Figure 11. TPS54427 Efficiency

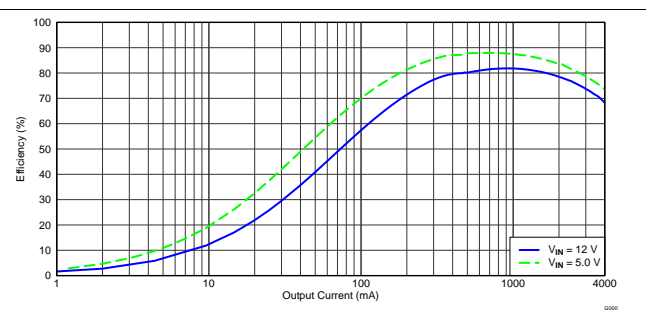


Figure 12. TPS54427 Light-Load Efficiency

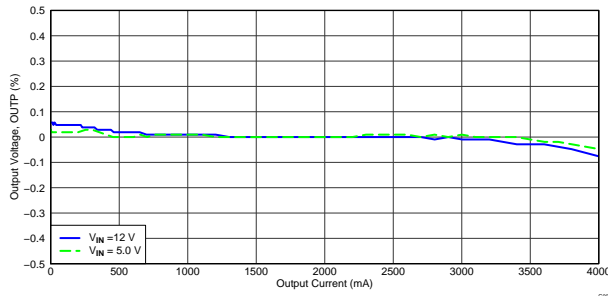


Figure 13. TPS54427 Load Regulation,  $V_{IN} = 5\text{ V}$  and  $V_{IN} = 12\text{ V}$ .

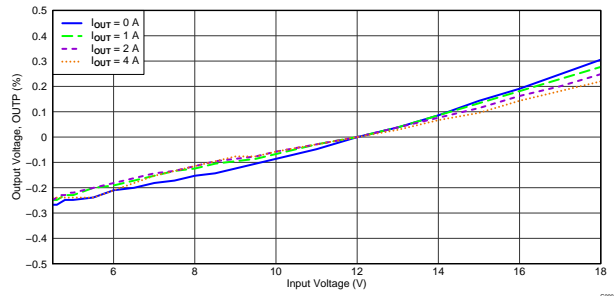


Figure 14. TPS54427 Line Regulation

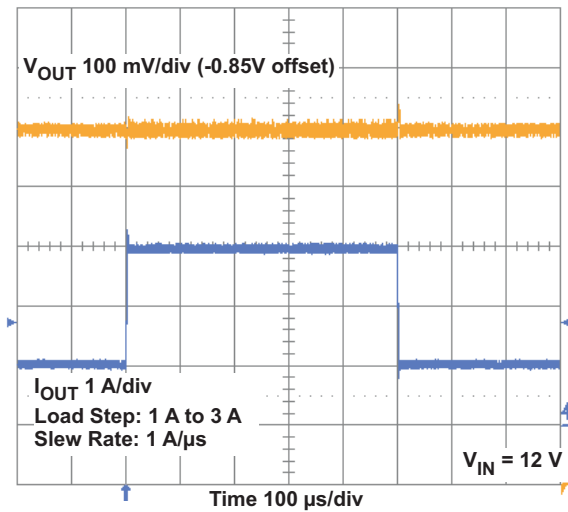


Figure 15. TPS54427 Load Transient Response

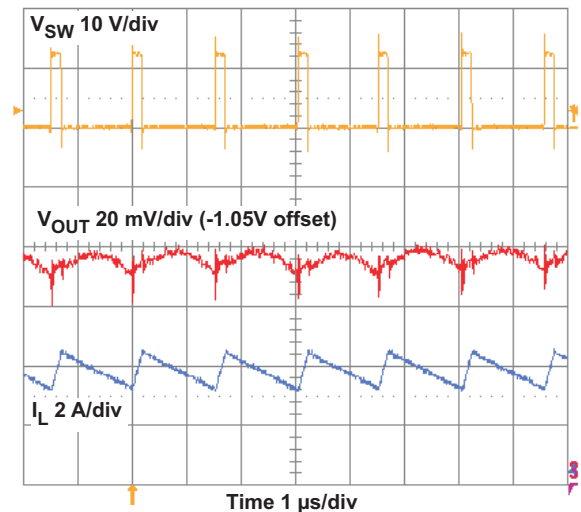


Figure 16. TPS54427 Output Voltage Ripple

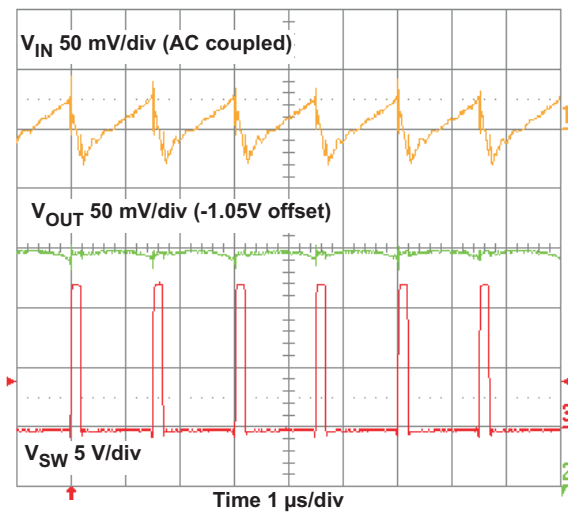


Figure 17. TPS54427 Input Voltage Ripple

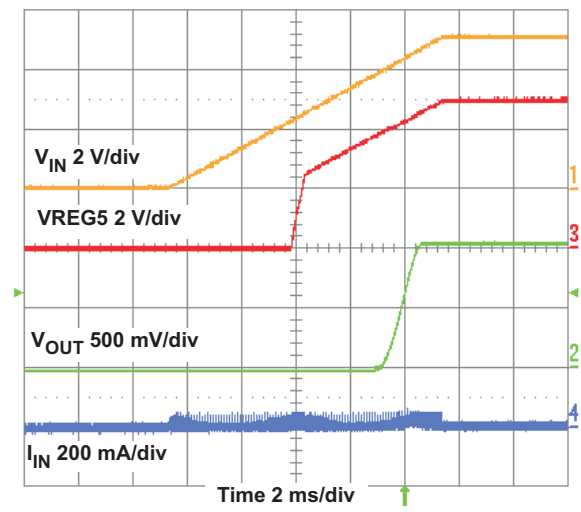
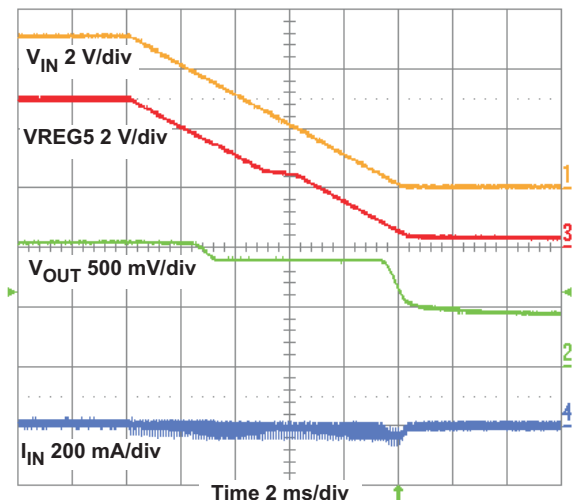
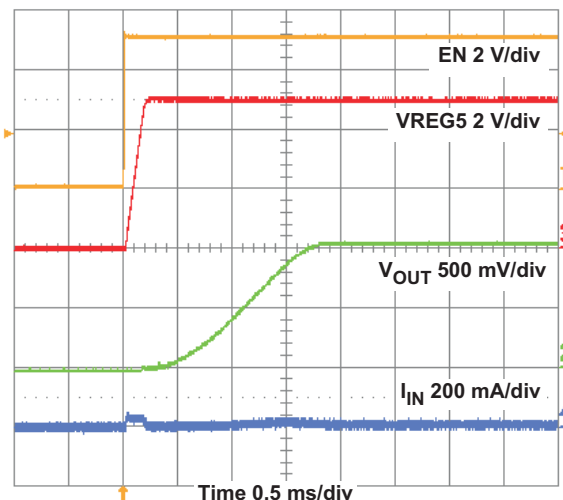
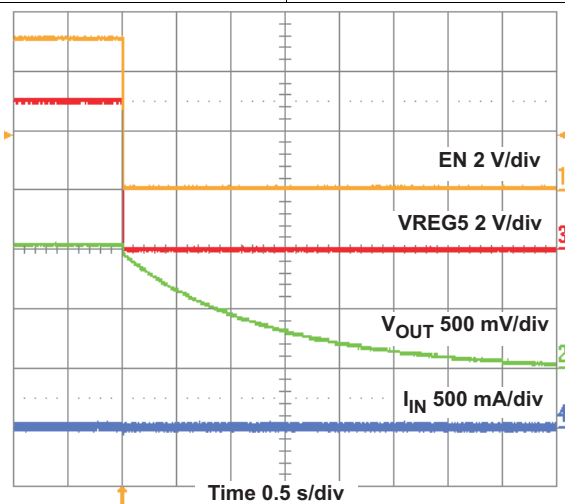


Figure 18. TPS54427 Start-Up Relative to  $V_{IN}$


**Figure 19. TPS54427 Shut-down Relative to  $V_{IN}$** 

**Figure 20. TPS54427 Start-Up Relative to EN**

**Figure 21. TPS54427 Shut-down Relative to EN**

## 9 Power Supply Recommendations

The TPS54427 is designed to operate from input supply voltage in the range of 4.5 V to 18 V. Buck converters require the input voltage to be higher than the output voltage. In this case the maximum recommended operating duty cycle is 65%. Using that criteria, the minimum recommended input voltage is  $V_o/0.65$ .

## 10 Layout

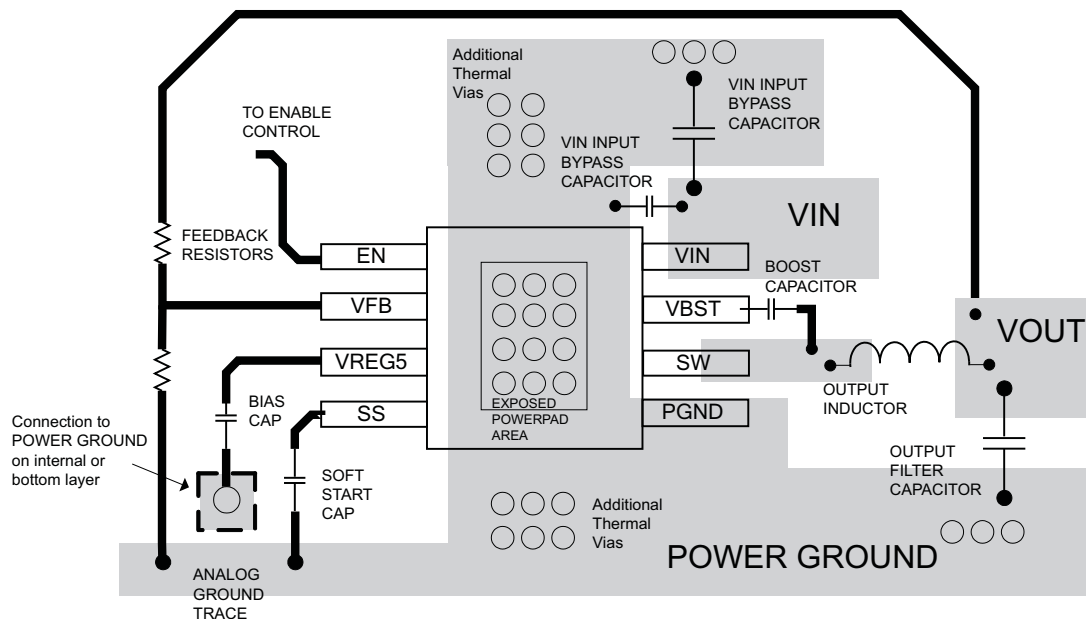
### 10.1 Layout Guidelines

1. The TPS54427 can supply relatively large current up to 4A. So heat dissipation may be a concern. The top side area adjacent to the TPS54427 should be filled with ground as much as possible to dissipate heat.
2. The bottom side area directly below the IC should have a dedicated ground area. It should be directly connected to the thermal pad of the using vias as shown. The ground area should be as large as practical. Additional internal layers can be dedicated as ground planes and connected to vias as well.
3. Keep the input switching current loop as small as possible.
4. Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections should be brought from the output to the feedback pin of the device.

## Layout Guidelines (continued)

5. Keep analog and non-switching components away from switching components.
6. Make a single point connection from the signal ground to power ground.
7. Do not allow switching current to flow under the device.
8. Keep the pattern lines for VIN and PGND broad.
9. Exposed pad of device must be connected to PGND with solder.
10. VREG5 capacitor should be placed near the device, and connected PGND.
11. Output capacitor should be connected to a broad pattern of the PGND.
12. Voltage feedback loop should be as short as possible, and preferably with ground shield.
13. Lower resistor of the voltage divider which is connected to the VFB pin should be tied to SGND.
14. Providing sufficient via is preferable for VIN, SW and PGND connection.
15. PCB pattern for VIN, SW, and PGND should be as broad as possible.
16. VIN Capacitor should be placed as near as possible to the device.

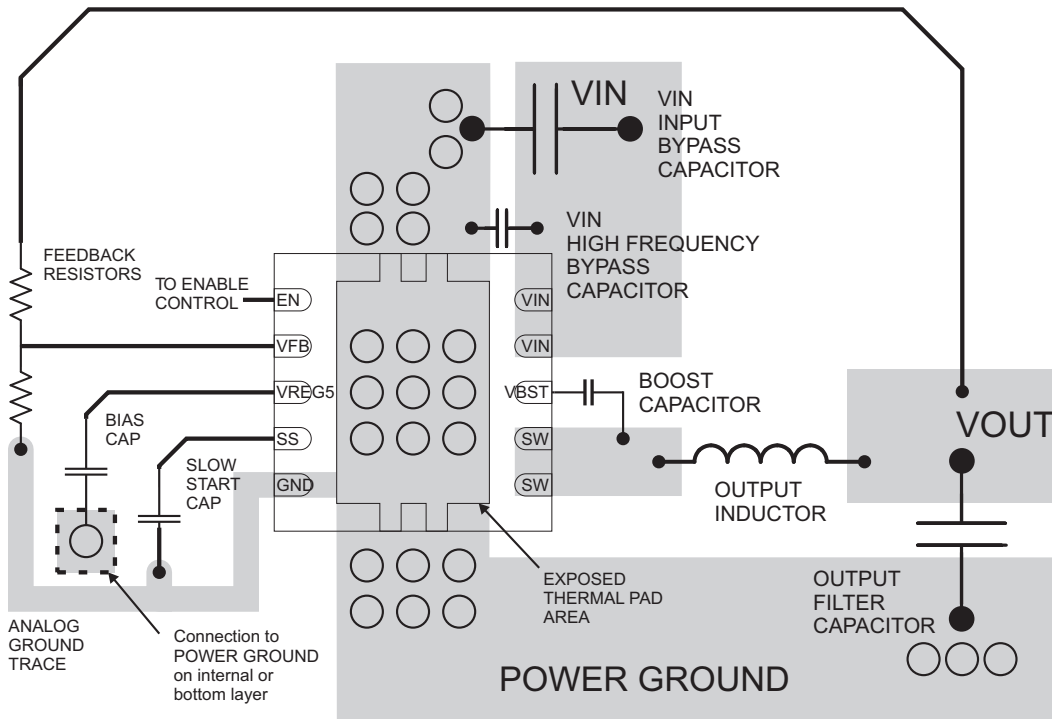
## 10.2 Layout Examples



**Figure 22. TPS54427 Layout**



Layout Examples (continued)



○ VIA to Ground Plane

Figure 23. PCB Layout for the DRC Package

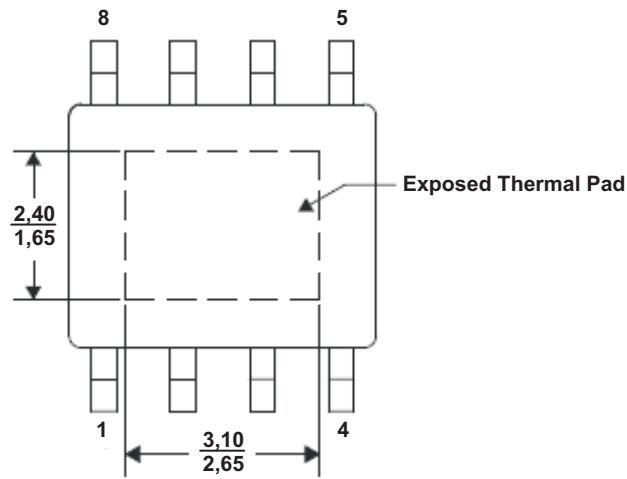
10.3 Thermal Considerations

This 8-pin DDA package incorporates an exposed thermal pad that is designed to be directly to an external heatsink. The thermal pad must be soldered directly to the printed board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the exposed thermal pad and how to use the advantage of its heat dissipating abilities, refer to Technical Brief, *PowerPAD™ Thermally Enhanced Package*, [SLMA002](#) and Application Brief, *PowerPAD™ Made Easy*, [SLMA004](#).

The exposed thermal pad dimensions for this package are shown in the following illustration.

**Thermal Considerations (continued)**



**Figure 24. Thermal Pad Dimensions**

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

#### 11.1.2 Design Support

WEBENCH™ software uses an iterative design procedure and accesses comprehensive databases of components. For more details, go to [www.ti.com/webench](http://www.ti.com/webench).

### 11.2 Documentation Support

#### 11.2.1 Related Documentation

For related documentation see the following:

- *PowerPAD™ Thermally Enhanced Package*, [SLMA002](#)
- *PowerPAD™ Made Easy*, [SLMA004](#)

### 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.4 Trademarks

D-CAP2, PowerPAD, E2E are trademarks of Texas Instruments.  
WEBENCH is a registered trademark of Texas Instruments.  
Blu-ray Disc is a trademark of Blu-ray Disc Association.  
All other trademarks are the property of their respective owners.

### 11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54427DDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-2-260C-1 YEAR	-40 to 85	54427	<a href="#">Samples</a>
TPS54427DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-2-260C-1 YEAR	-40 to 85	54427	<a href="#">Samples</a>
TPS54427DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	54427	<a href="#">Samples</a>
TPS54427DRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	54427	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54427DDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
TPS54427DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS54427DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54427DDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0
TPS54427DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS54427DRCT	VSON	DRC	10	250	210.0	185.0	35.0



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL-OUTLINE



4202561/F 12/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - This package complies to JEDEC MS-012 variation BA

PowerPAD is a trademark of Texas Instruments.

DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206322-6/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

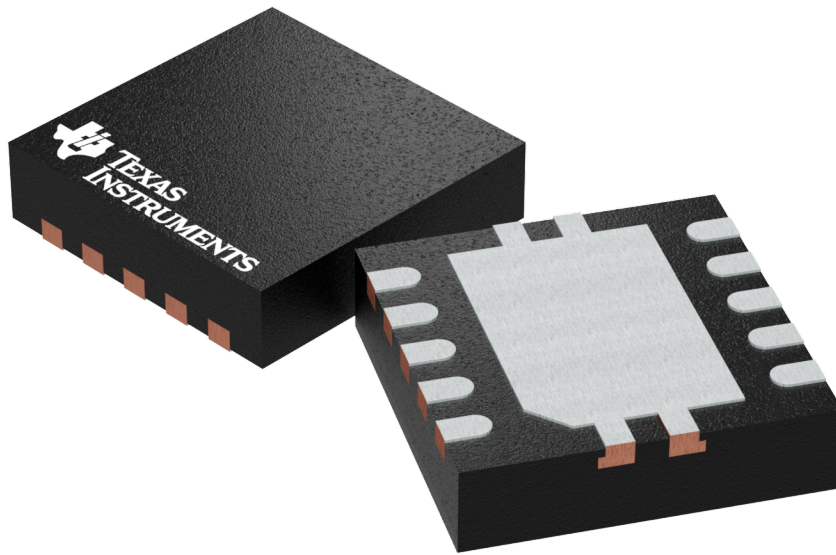
PowerPAD is a trademark of Texas Instruments.

## GENERIC PACKAGE VIEW

DRC 10

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4204102-3/M



# EXAMPLE BOARD LAYOUT

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:20X



SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:  
80% PRINTED SOLDER COVERAGE BY AREA  
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.