Beyond Innovation Technology Co., Ltd.

Data Sheet

BIT3102A

Low Cost PWM CCFL Controller

Version: 1.3

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BIT3102A

Features:

- **PWM Modulation**
- **Open Lamp Protection**
- **Internal UVLO (Under Voltage Look Out) function**
- **Dimming Control**
- **CMOS Totem Pole output**
- **NMOS output driving**
- **SOP /DIP Packing**
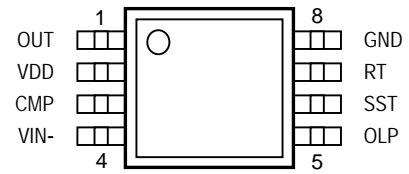
Applications:

- **Cold Cathode Fluorescent Lamps system**
- **Notebook PC**
- **LCD Monitor**
- **Palm-top Computers**
- **Video Phone/ Door Phone**
- **Portable Instrumentation**
- **Personal Digital Assistants**
- **Airline Entertainment Centers**
- **Automotive Display**
- **ATM/ Financial Terminal**
- **POS Terminal**
- **Navigation Devices (GPS Equipment)**
- **Test Equipment**
- **Copiers and Office Equipment**
- **Medical Equipment**

Recommended Operating Condition:

Supply Voltage……………………………4.5 ~ 13.2 V
Operating Frequency………………...…50K ~ 250K Hz
Operating Ambient Temperature………...0 ~ 70

Pin Layout:

OUT	1	8 GND
VDD		RT
CMP		SST
VIN-	4	5 OLP

General Description:

To aim at the Cold Cathode Fluorescent Lamp (CCFL) applications, the BIT3102A integrated all functions required in a single 8 pin chip.   The chip provides a fully functioned PWM control circuit with a true lamp current feedback protection.   By setting the required time for striking the lamp through SST , the open-lamp condition can be detected after lamp striking period.   The lamp dimming can be done through a PWM feedback loop. CMOS process reduces the operating current (1mA typical) and NMOS output driving capability enhances the system efficiency.
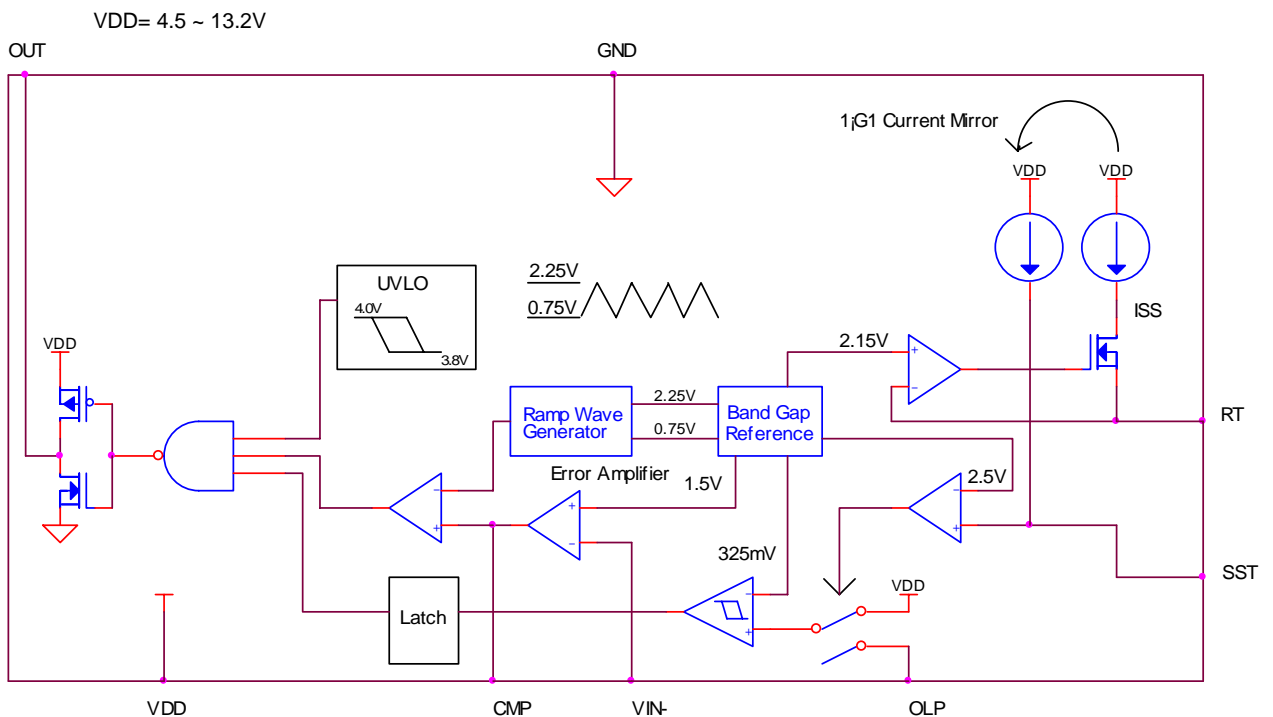
Absolute Ratings: *(if Ta=25)*

VDD…………………………………-0.3 ~ +13.7 V
GND…………………………………±0.3 V
Input Voltage……………………….-0.3 ~ VDD+0.3 V
Operating Ambit Temperature…….0 ~ +70
Operating Junction Temperature….+150
Storage Temperature………………-55~+150

Functional Block Diagram:

Function Description:

UVLO: The Under-Voltage-Look-Out circuit turns the output driver off when supplying voltage drops to a specified low level.

Band Gap Reference: This circuit provides a accuracy voltage reference which is very stable even though the operating temperature is variable.   Base on this reference, a specified voltage can be generated which is used by another circuit.

Ramp Wave Generator: This circuit generates a typical 140KHz ramp wave. (as R_T =100 K)   The relation between frequency and resistor R_T is as the equation below:

Freq. (KHz) = 14000/R_T(K)

PWM Controller: The pulse width modulation control circuit includes a ramp wave generator, an error amplifier and a comparator.   These devices provide the required active components for the PWM feedback control application.

The Power On Initialization and Open Lamp Protection: The current source I_{SS} charges the external resistor and capacitor during power on process.   The voltage drops on the SST pin will be increased as

$V_{SST} = I_{SS}R_{SS} (1-e^{-t/R_{SS}C_{SS}})$; (Fig.a)

Where I_{SS}= V_{RT}/R_T ± 10%,and V_{RT} =2.15V

The output is disabled to "low" level and open lamp protection is disable while SST <0.325V. A ~ 180uA current is flow into INN to set the initial state.   The PWM controller is enable while 2.5V < SST < 0.325V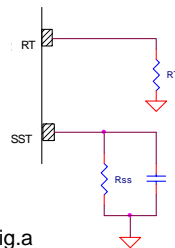. The open lamp protection circuit will be enable when V_{SST} > 2.5V (Fig.b) The required time for striking the lamp could be calculated as bellow:

T_{STRIKE} = ($R_{SS}C_{SS}$) **ln**(($I_{SS}R_{SS}$-0.325)/($I_{SS}R_{SS}$-2.175))
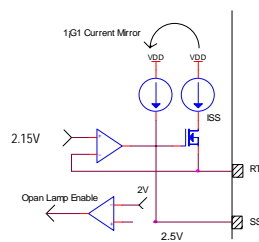
T_{STRIKE} is decided by the characteristic of lamp.

Fig.a

Fig.b

Table 1.   Power On Initialization and Open Lamp Protection

	OUT	OLP	VIN-
SST < 0.325V	Disable to "Low"	Disable	Internally Forced to "High"
2.5V < SST < 0.325V	Enable	Disable	Externally Controlled
SST >2.5V	Enable	Enable	Externally Controlled

Pin Description:

Pin No.	Names	Description
1	OUT	PWM output, logic high active for driving NMOS device.
2	VDD	Supply voltage.
3	CMP	PWM controller input, the output of error amplifier.
4	Vin-	PWM controller input, the inverting input of error amplifier.
5	OLP	A voltage sense input pin. If voltage level is less than 325 mV after a user defined period of time, the chip will shut down the OUT and PWM circuits. A digital latch circuit latches this result. The latch condition will be released if the power be turned off.
6	SST	The timer for open lamp protection.
7	RT	Operation frequency control.
8	GND	Ground

DC/AC Characteristics:

Parameter	Test Conditions	Min.	Typ.(Limits)	Max.	Unit
Reference Voltage					
Output voltage	Measure Vin- VDD=12V, Ta=25°C	1.455	1.5	1.545	V
Line regulation	VDD=4.5 ~ 13.2 V		2	20	mV

Under Voltage Look Out					
Upper threshold voltage	Ta=25	3.8	4	4.2	V
Hysteresis		0.1	0.2	0.3	V
Ramp Wave Generator					
Frequency	R_T=100K	120	140	160	KHz
Operating Frequency	note 1	50		250	KHz
Output peak			2.25		V
Output valley			0.75		V
Error Amplifier					
Input voltage	note 1	0.75		2.25	V
Open loop gain		60	80		dB
Unit gain band width		1	1.5		MHz
Open Lamp Enable					
Output current	VDD=12V, Ta=25		2.15V/R_T		uA
Open lamp detection enable			2.5		V
Open Lamp Protection					
Open lamp detection lower threshold	VDD=12V, Ta=25		325		mV
Hysteresis			50		mV
Output					
CMOS output impedance	note 1		50		
Rising Time	1000pF load,		110		ns
Falling Time	note 1		100		ns

Ta : ambient temperature.

Note 1: It is guaranteed by design not 100% tested.
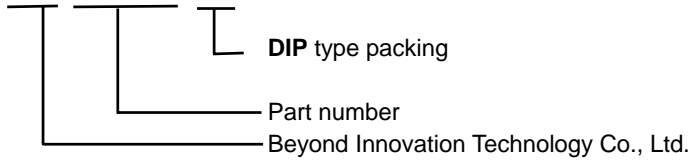
Application Circuit:

A low cost 1~2 lamp design.

VDD=4.5V~13.2V
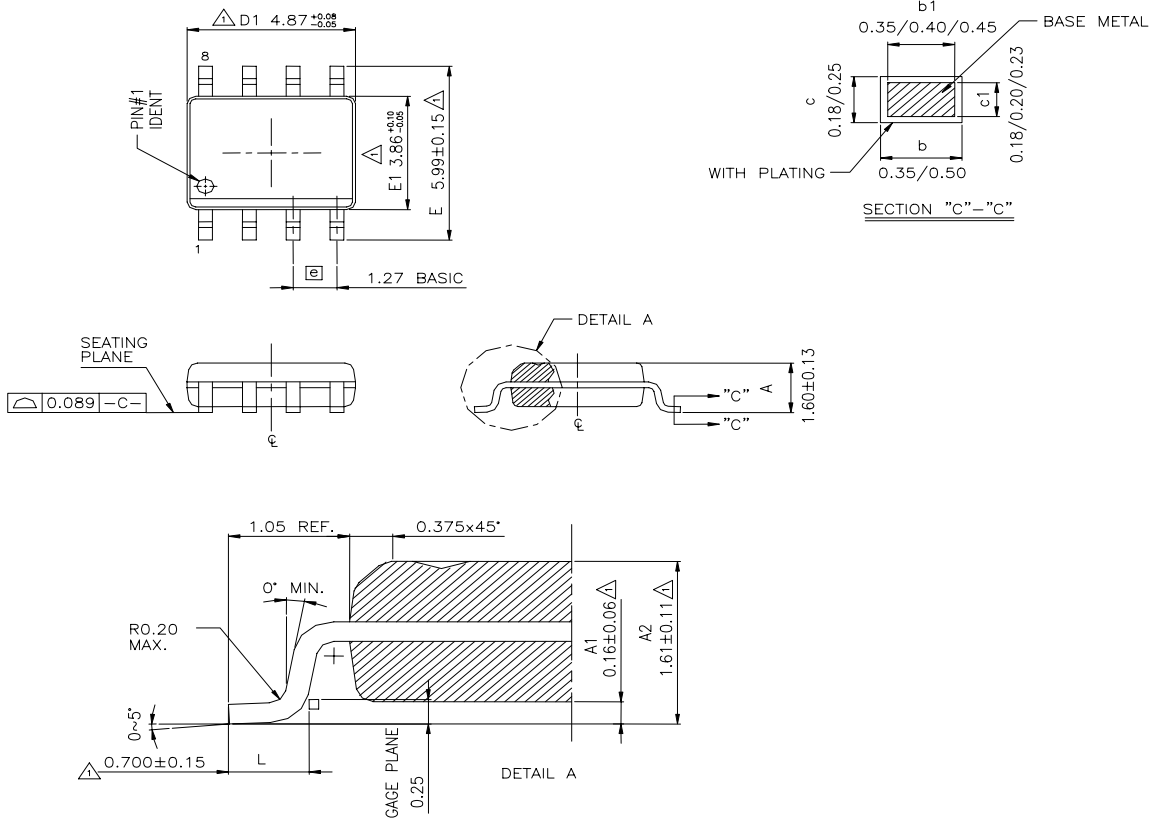BRIGHTNESS=DC 0~3.3V, 0V brightest dimming.
CN2 may connect 1~2 CCFLs
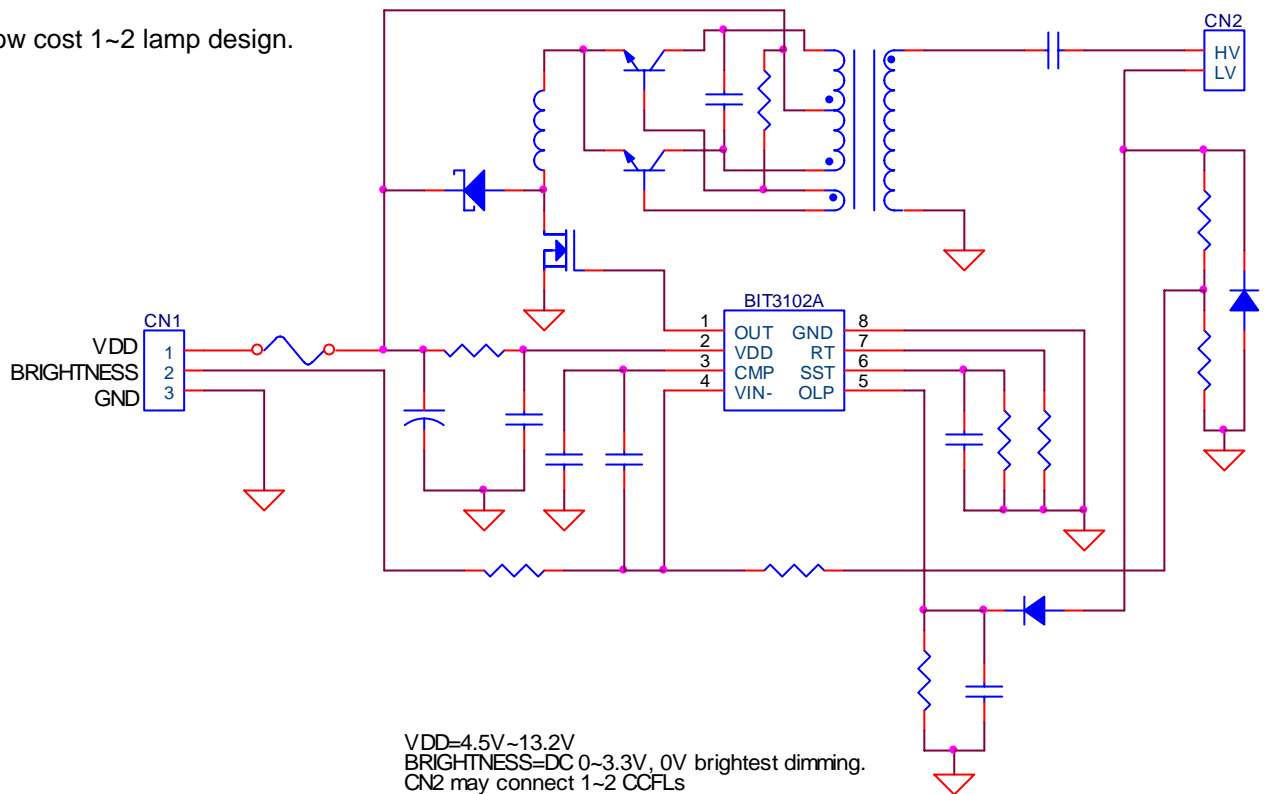
Order Information:

BI T3102A-S0

SOP type packing

Part number
Beyond Innovation Technology Co., Ltd.

BI T3102A-DP

DIP type packing

Part number
Beyond Innovation Technology Co., Ltd.
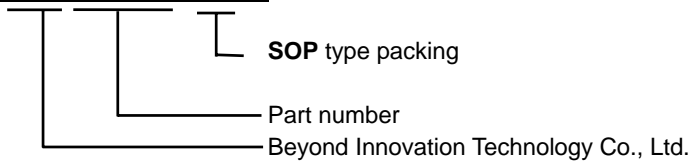
Package Information :

Unit: mm

SOP type :

DIP type :