Low Standby-Power Off-line PWM converters

General Description

The AP8012H consists of a Pulse Width Modulator (PWM) controller and a power MOSFET, specifically designed for a high performance off-line converter with minimal external components. AP8012H offers complete protection coverage with automatic self-recovery feature including Cycle-by-Cycle current limiting (OCP), over temperature protection (OTP), under-voltage Lockout protection(UVLO)，VDD over-voltage protection(OVP), and soft-start. Burst mode operation and device very low consumption helps to meet the standby energy saving regulations. Excellent EMI performance is achieved with frequency modulation. The device consists of a high voltage start-up circuit in order to reduce the system set-up time. The device provides an advanced platform well suited for low standby-power and cost-effective flyback converters.

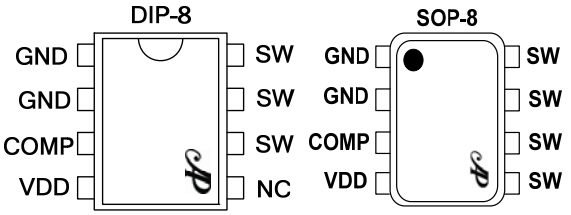
Features

- Integrated 800V avalanche-rugged power MOSFET
- 85V to 265V wide range AC voltage input
- Semi enclosed steady output power 6W(DIP-8)@85~265V_{AC}
- Frequency modulation for low EMI
- Burst-mode Operation
- Built-in Soft Start
- Internal HV Start-up Circuit
- Excellent Protection :
  - ✧ Over Current Protection (OCP)
  - ✧ Over Temperature Protection (OTP)
  - ✧ VDD over-voltage protection (OVP)

Applications

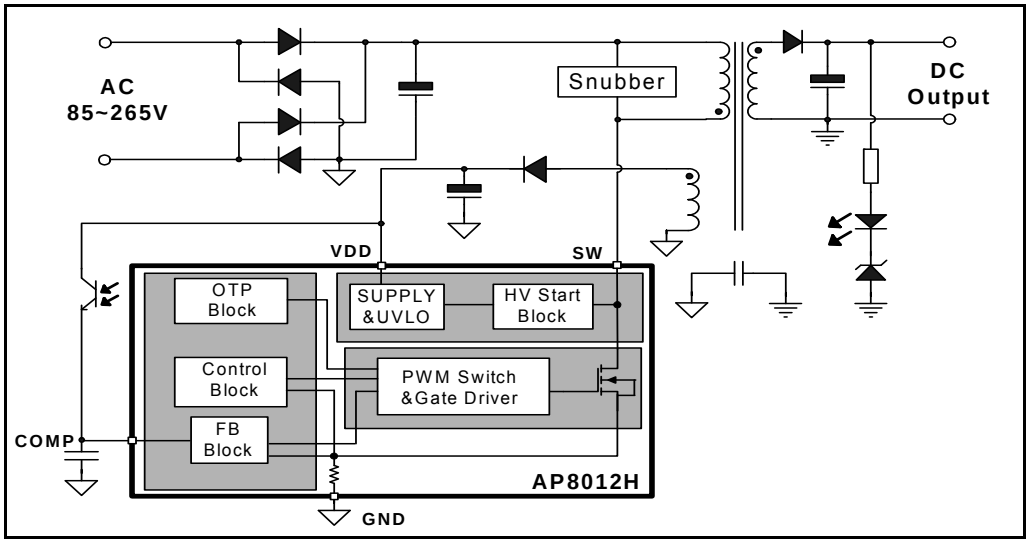
- Electromagnetic Oven power supplies
- Small household application power supplies (Coffee machine, Electric kettle, etc.)

Package/Order Information



Order codes	Package
AP8012HNEC-T1E	DIP-8
AP8012HNEC-T1L	DIP-8
AP8012HSEC-R1	SOP-8

Typical Application



Pin Definitions

Table 1. Pin Definitions

SOP-8 Pin Number	DIP-8 Pin Number	Pin Name	Pin Function Description
1,2	1,2	GND	Ground
3	3	COMP	Voltage feedback. By connecting a opto-coupler to close the control loop and achieve the regulation.
4	4	VDD	Positive Supply voltage Input.
-	5	NC	No connection
5,6,7,8	6,7,8	SW	The SW pin is designed to connect directly to the primary lead of the transformer.

Typical power

Table 2. Typical power

Package	AC line Voltage	continuous power(1)	Peak power(2)
SOP-8	**85-265 V_{AC}**	**3.6W(12V300mA)**	**6W(12V500mA)**
DIP-8	**85-265 V_{AC}**	**6W(12V500mA)**	**8.4W(12V700mA)**

Note:

1. Maximum output power in a semi enclosed design measured at 75°C ambient temperature, Duration:2 hours
2. Peak power in a semi enclosed design measured at 75°C ambient temperature, Duration:1 min

Absolute Maximum Ratings

Supply voltage Pin VDD……..……..……-0.3~45V

High-Voltage Pin, SW……-0.3~750V

COMP……..……..……..……-0.3~7V

Junction temperature ……..……..……..……..……..……-40~150℃

Storage temperature……..……..…… ……..……-55~150℃

Lead Temperature (Soldering, 10secs) ……..……260℃

Package Thermal Resistance $R\theta_{JC}$ (SOP-8)……..……..……...80℃/W

Package Thermal Resistance $R\theta_{JC}$ (DIP-8)……..……..……40℃/W

Electrostatic Discharge Human Body Mode (HBM, ESDA/JEDEC JDS-001-2014)……..……..…….. ±4kV

SD voltage Protection (1) (Air discharge to pins of AP8012H with ESD Generator)……..……..…… ..8kV

Drain Pulse Current（Tpulse=100us）……..……2A

Note: 1. Enterprise internal standards, for reference only.

Electrical Characteristics

(T_J =25°C, VDD = 15 V; unless otherwise specified)

Table 3. Power section

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
B_{VDSS}	VDMOS Breakdown Voltage	I_{SW} =250uA	750	820		V
I_{OFF}	Static Drain-Source off current	V_{SW} =550V			100	uA
R_{DSON}	Static Drain-Source on Resistance	I_{SW} = 400mA, T_J=25°C		18		Ω

Table 4. Control section

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
UVLO SECTION						
V_{START}	VCC Start Threshold Voltage	V_{COMP}=0V	13	14.5	16	V
V_{STOP}	VCC Stop Threshold Voltage	V_{COMP}=0V	7	8	9	V
V_{HYS}	VCC Threshold Hysteresis			6.5		V
V_{RST}	VDD Reset Voltage		5.5	6	6.5	V
OSCILLATOR SECTION						
F_{OSC}	Initial Accuracy	T_A = 25°C	40	45	50	kHz
FD	Frequency Variation			±5		kHz
FM	Modulation frequency			167		Hz
D_{MAX}	Maximum duty cycle		65	80	90	%
FEEDBACK SECTION						
I_{COMP}	Feedback Shutdown Current			1.2		mA
R_{COMP}	COMP Pin Input Impedance			1.15		kΩ
CURRENT LIMIT SECTION						
I_{LIM}	Peak Current Limit	T_A = 25°C	0.44	0.55	0.66	A
T_{LEB}	Minimum Turn On Time	LEB time		350		ns
t_{SS}	Soft-start time			10		ms
I_{D_BM}	Peak drain current during burst mode			100		mA

Thermal Shutdown SECTION						
T_{SD}	Thermal Shutdown Temperature		140	170	-	°C
T_{HYST}	Thermal Shutdown Hysteresis			30		°C
SUPPLY CURRENT SECTION						
I_{CH}	Startup Charging Current (SW pin)	V_{DRAIN} = 105 V, V_{COMP} = GND, V_{DD} = 12 V		-1.2		mA
AP8012H(E) I_{DD}	Operating supply current, switching	V_{DD} = 16 V, V_{COMP}= 0V		4		mA
AP8012H(L) I_{DD}	Operating supply current, switching	V_{DD} = 16 V, V_{COMP}= 0V		0.6		mA
V_{DD}	Operating voltage range	After turn-on	10		35	V
V_{OVP}	VDD over voltage		37	40	43	V
I_{DD_OFF}	Operating supply current with VDD < V_{STOP}	V_{DD} = 6 V	100		400	uA

Typical circuit

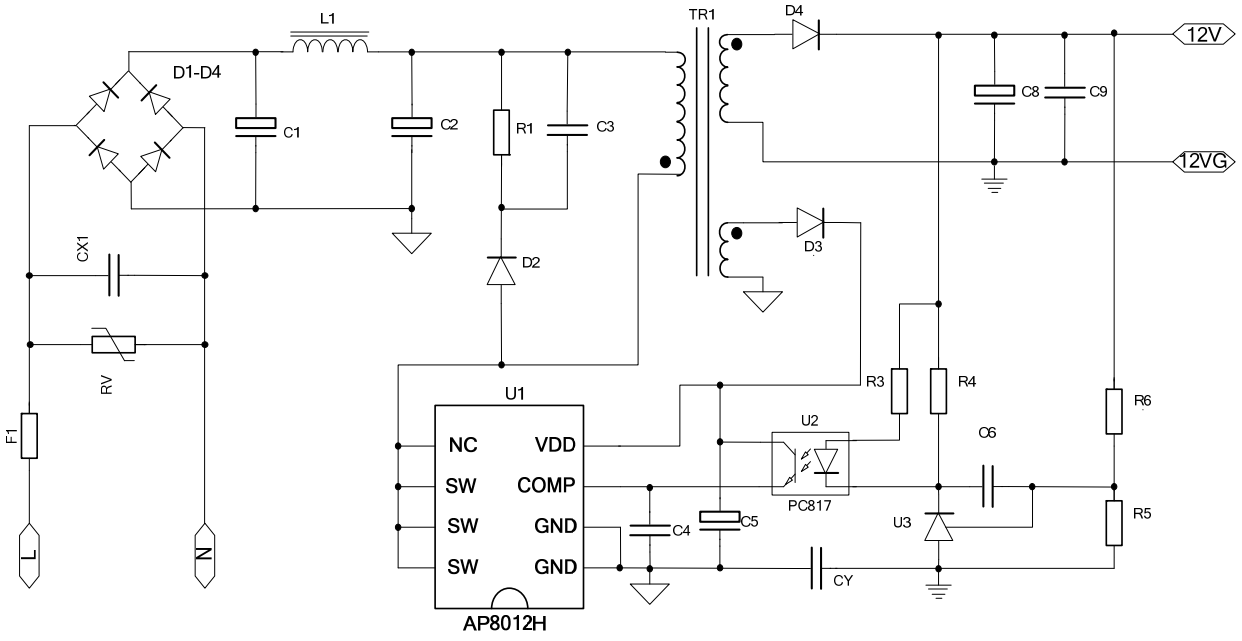
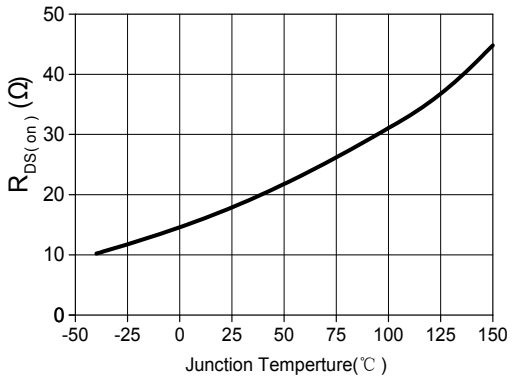
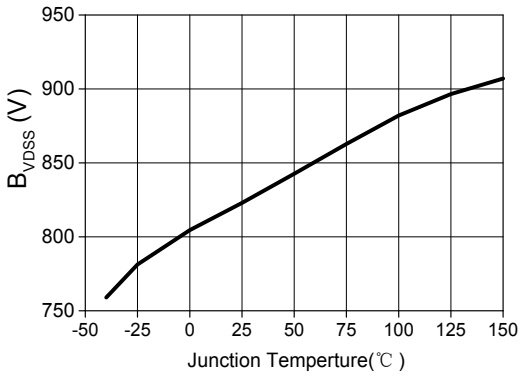


Figure 1. Flyback application (basic)

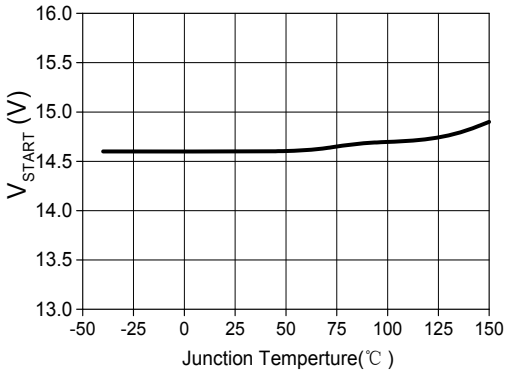
Typical Characteristics Plots



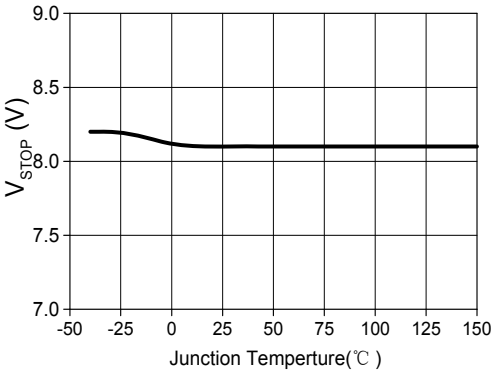
(a) $R_{DS(on)}$ vs T_j



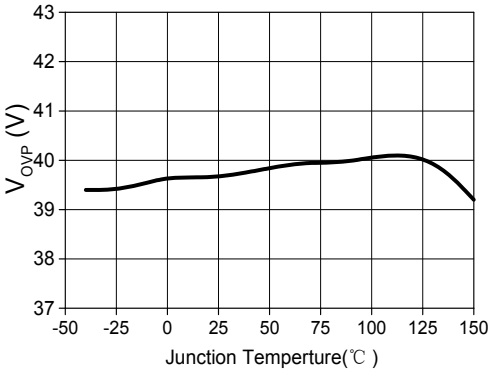
(b) B_{VDSS} vs T_j



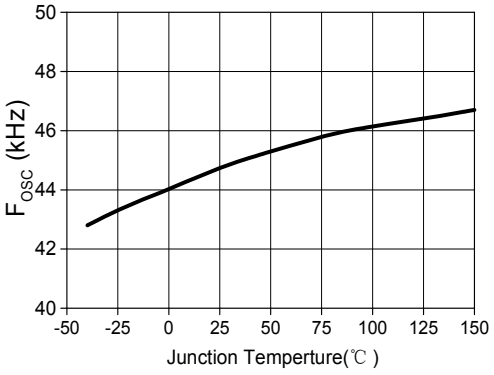
(c) V_{START} vs T_j



(d) V_{STOP} vs T_j



(e) V_{OVP} vs T_j



(f) F_{OSC} vs T_j

Functional Description

1. Startup

This device includes a high voltage start up current source connected on the SW of the device. As soon as a voltage is applied on the input of the converter, this start up current source is activated and to charge the VDD capacitor as long as VDD is lower than V_{START}. When reaching V_{START}, the start up current source is cut off and VDD is sourced by auxiliary side. As VDD falls below V_{STOP}, the HV-Start circuit won't work immediately until VDD is lower than V_{RST}.

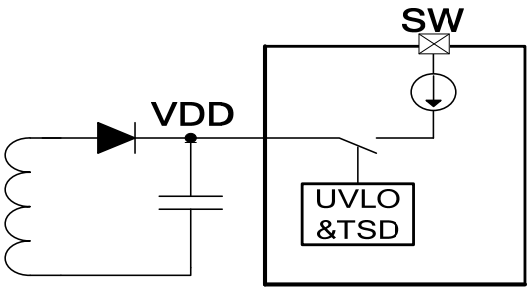


Fig 2. Startup circuit

2. Soft-start up

In the process of start up, the current of drain increases to maximum limitation step by step. As a result, it can reduce the stress of secondary diode greatly and help to prevent the transformer turning into the saturation states. Typically, the duration of soft-start is 10 ms.

3. Gate driver

The internal power MOSFET in AP8012H is driven by a dedicated gate driver for power switch control. Too weak the gate driver strength results in higher conduction and switch loss of MOSFET while too strong gate drive results in worse EMI.

A good tradeoff is achieved through the built-in totem pole gate design with proper output strength and dead time. The good EMI system design and low idle loss is easier to achieve with this dedicated control scheme.

4. Oscillator

The switching frequency of AP8012H is internally fixed at 45 kHz. No external frequency setting components are required for PCB design.

The frequency modulation is implemented in AP8012H. So that, it minimizes the conduction band EMI and therefore eases the system design because the tone energy could be spread out.

5. Feed-back

A feedback pin controls the operation of the device. Unlike conventional PWM control circuits which use a voltage input, the COMP pin is sensitive to current. Figure 3 presents the internal current mode structure. The Power MOSFET delivers a sense current which is proportional to the main current. R2 receives this current and the current coming from the COMP pin. The voltage across R2 (VR2) is then compared to a fixed reference voltage. The MOSFET is switched off when VR2 equals the reference voltage.

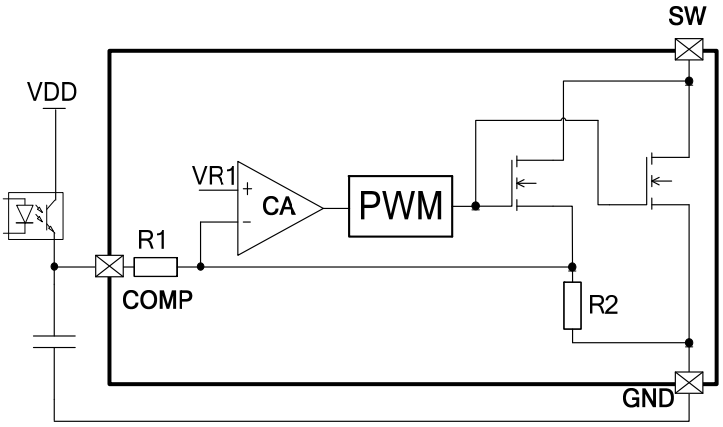


Fig 3. Feedback circuit

6. Leading Edge Blanking (LEB)

At the instant the internal Sense FET is turned on, there usually exists a high current spike through the Sense FET, caused by the primary side capacitance and secondary side rectifier diode reverse recovery. Excessive voltage across the sense resistor would lead to false feedback operation in the current mode PWM control. To counter this effect, the device employs a leading edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for a short time (typically 350ns) after the Sense FET is turned on.

7. Under Voltage Lock Out

Once fault condition occurs, switching is terminated and the Sense FET remains off. This causes VDD to fall. When VDD reaches the VDD reset voltage, 6V, the protection is reset and the internal high voltage current source charges the VDD capacitor. When VDD reaches the UVLO start voltage, 14.5V, the device resumes its normal operation. In this manner, the auto-restart can alternately enable and disable the switching of the power Sense FET until the fault condition is eliminated.

8. Thermal Shutdown (TSD)

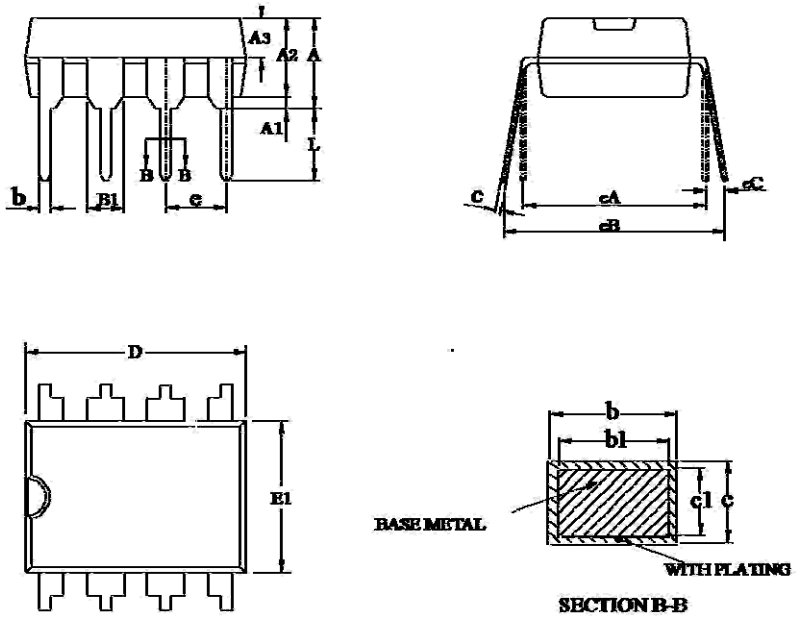
The Sense FET and the control IC are integrated in the same chip, making it easier for the control IC to detect the temperature of the Sense FET. When the temperature exceeds approximately 170°C, thermal shutdown is activated, the device turn off the Sense FET. The device will go back to work when the lower threshold temperature about 140°C is reached.

Package Dimensions (DIP-8)

Table 5. DIP-8 mechanical data

Size / symbol	Min.(mm)	Max.(mm)	Size / symbol	Min.(mm)	Max.(mm)
A	3.60	4.00	c1	0.23	0.27
A1	0.51	——	D	9.05	9.45
A2	3.00	3.40	E1	6.15	6.55
A3	1.55	1.65	e	2.54BSC	
b	0.44	0.53	e A	7.62BSC	
b1	0.43	0.48	e B	7.62	9.30
B1	1.52BSC		e C	0.00	0.84
c	0.24	0.32	L	3.00	——

Figure 4. Package dimensions



TOP MARK	Package
AP8012H YWWXXXXX	DIP-8

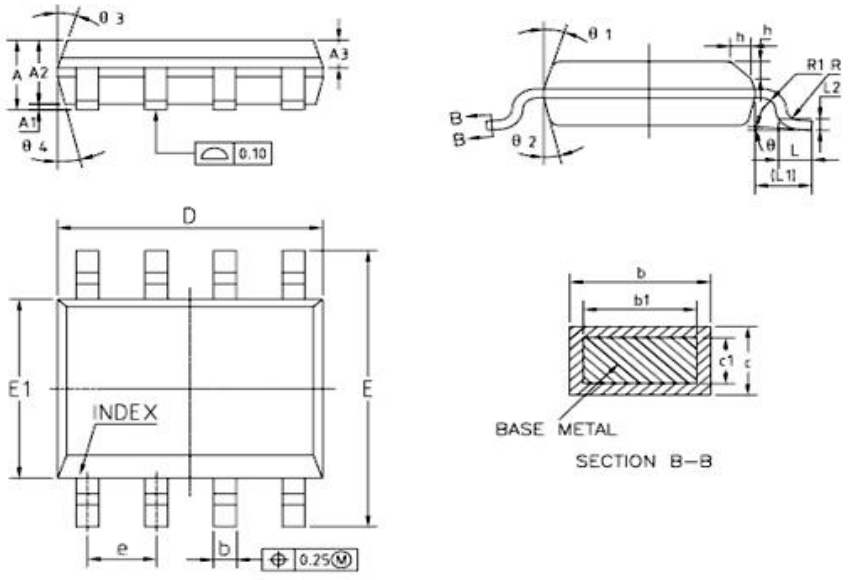
Note: Y: Year Code; WW: Week Code; XXXXX: Internal Code

Package Dimensions (SOP-8)

Table 6. SOP-8 mechanical data

Size / symbol	Min.(mm)	Typ.(mm)	Max.(mm)	Size / symbol	Min.(mm)	Typ.(mm)	Max.(mm)
A	1.35	1.55	1.75	L	0.45	0.60	0.80
A1	0.10	0.15	0.25	L1	1.04REF		
A2	1.25	1.40	1.65	L2	0.25BSC		
A3	0.50	0.60	0.70	R	0.07	—	—
b	0.38	—	0.51	R1	0.07	—	—
b1	0.37	0.42	0.47	h	0.30	0.40	0.50
c	0.17	—	0.25	θ	0°	—	8°
c1	0.17	0.20	0.23	θ1	15°	17°	19°
D	4.80	4.90	5.00	θ2	11°	13°	15°
E	5.80	6.00	6.20	θ3	15°	17°	19°
E1	3.80	3.90	4.00	θ4	11°	13°	15°
e	1.270（BSC）						

Figure 5. Package dimensions



TOP MARK	Package
AP8012H YWWXXXXX	SOP-8

Note: Y: Year Code; WW: Week Code; XXXXX: Internal Code

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