2.5V to 5.5V 12Bit DAC with POWER DOWN

PRODUCT DESCRIPTION

MS5614/5614T is a 12bit four channel output voltage DAC, the interface uses the four wire serial port mode, it can be compatible with TMS320, SPI, QSPI and Microwire serial port. MS5614/5614T control data has 16bit, including DAC address, control byte, and 12bitDAC data, the power range is 2.7V to 5.5V. The output of resistor series is connected to a class AB rail to rail buffer with a gain of 6dB. The output buffer improves the stability and reduces the setup time. MS5614/5614T has power down mode, which can optimize power consumption at work.

MS5614 is SOP16 package and MS5614T is TSSOP16 package.

FEATURES

- 12bit Conversion Accuracy
- Programmable Setup Time 3us or 9us
- Compatible with TMS320, SPI, QSPI, Microwire Interface
- Internal Power on Reset
- Low Power Consumption
- Integration REF Buffer
- The output range is twice the reference voltage
- Software and Hardware Power Down

  Power Supply Voltage: 2.7V ~ 5.5V

SOP16

TSSOP16

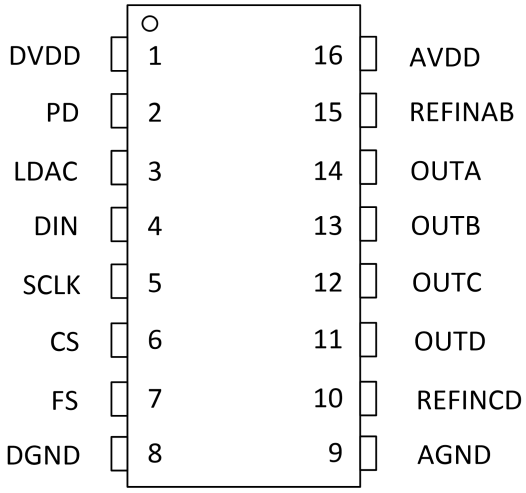
APPLICATIONS

- Digital Servo System Control
- Digital Compensation and Gain Adjustment
- Industrial Process Control
- Mechanical and Mobile Control Equipment
- High Capacity Storage Devices

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS5614	SOP16	MS5614
MS5614T	TSSOP16	MS5614T

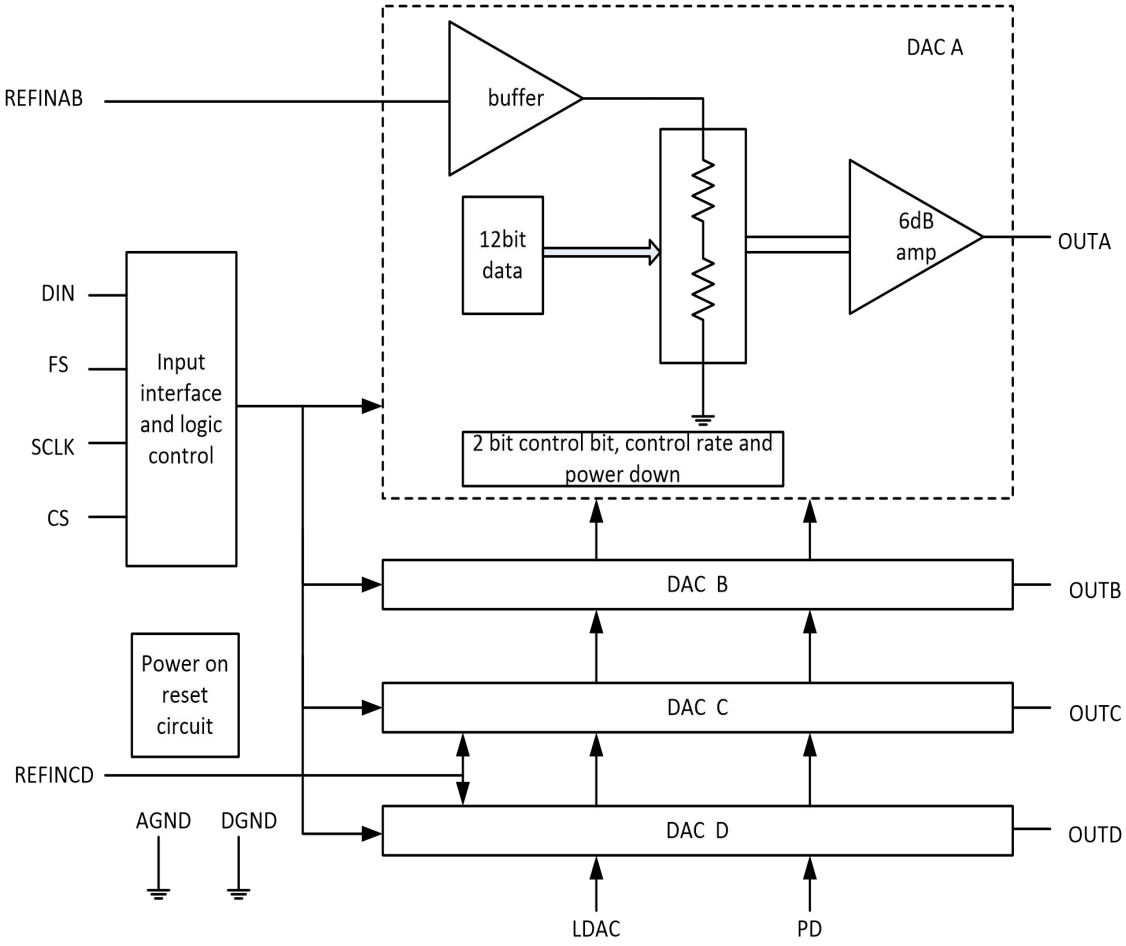
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
1	DVDD	--	Digital Power Supply
2	PD	I	Power Down Pin, when the input low level, turn off the chip
3	LDAC	I	When LDAC input is high level, DAC output is not updated; when LDAC input is low level, DAC output is updated.
4	DIN	I	Serial Data Input
5	SCLK	I	Serial Digital Clock Input
6	CS	I	Chip Select, Low Level Input Valid
7	FS	I	Frame Synchronization Input Signal
8	DGND	--	Digital Ground
9	AGND	--	Analog Ground
10	REFINCD	I	Reference Input Voltage for Channels C and D
11	OUTD	O	Channel D Analog Output
12	OUTC	O	Channel C Analog Output
13	OUTB	O	Channel B Analog Output
14	OUTA	O	Channel A Analog Output
15	REFINAB	I	Reference Input Voltage for Channels A and B
16	AVDD	--	Analog Power Supply

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Range	Unit
Analog Supply Voltage	AVDD	-0.3 ~ +7	V
Digital Supply Voltage	DVDD	-0.3 ~ +7	V
Supply Voltage Difference	AVDD to DVDD	-2.8 ~ +2.8	V
Input Digital Voltage Range	VIN	-0.3 ~ DVDD+0.3	V
Reference Input Voltage Range	VREFIN	-0.3 ~ AVDD+0.3	V
Operating Temperature Range	TA	-40 ~ +105	°C
Storage Temperature Range	Tstg	-65 ~ +150	°C
Maximum Junction Temperature	Jt	150	°C
Welding Temperature(10s)		260	°C

ELECTRICAL CHARACTERISTICS (3.3V)

Recommend Operating Conditions

Parameter	Condition	Min	Typ	Max	Unit
Supply Voltage	5V Power	4.5	5	5.5	V
	3V Power	2.7	3	3.3	
Digital Input High Level VIH	DVDD=2.7V	2			V
	DVDD=5.5V	2.4			
Digital Input Low Level VIL	DVDD=2.7V			0.6	V
	DVDD=5.5V			1	
REF Voltage	5V Power(See Note 1)	0	2.048	VDD-1.5	V
	3V Power(See Note 1)	0	1.024	VDD-1.5	
Load Resistance		2	10		kΩ
Load Capacitance				100	pF
SCLK Rate				20	MHz

Note 1: Input voltage greater than AVDD/2 will result in saturated output at large DAC input codes.

Static DAC Specifications

Parameter		Condition	Min	Typ	Max	Unit
Resolution			12			Bits
DNL		See Note 2		±1.5	±4	LSB
INL		See Note 3		±0.5	±1	LSB
Zero Scale Error		See Note 4			±12	mV
Zero Scale Error Temperature Coefficient		See Note 5		10		ppm/°C
Gain Error		See Note 6			±0.6	%of FS Voltage
Gain Error Temperature Coefficient		See Note 7		10		ppm/°C
PSRR	Zero Scale	See Note 8 and 9		-80		dB
	Full Scale			-80		dB

Note:

2. Relative accuracy or integrated nonlinearity (INL) refers to linear error, which is the maximum deviation of the output from the ideal output by eliminating zero error and full error.

3. Differential Nonlinearity (DNL), the differential error, refers to the maximum amplitude change adjacent to LSB.

4. Zero scale offset refers to the analog output of zero input.

5. Zero scale temperature drift refers to the temperature change of the analog output when digital input is zero.

6. Gain error refers to the deviation between analog output and ideal output after zero error is removed.

7. Gain Error Temperature Drift refers to the variation of the deviation between analog output and ideal output with temperature after zero error is removed.

8. The power rejection ratio at zero points refers to the ratio of change in output caused by a change in AVDD of 5 +0.5 V and 3 +0.3 V when the digital input is all zero.

9. When the full-amplitude output power rejection ratio is all higher than the exponential word input, the change ratio of output is caused by the change of AVDD by 5 +0.5 V and 3 +0.3 V.

DAC Output Specifications

Parameter	Condition	Min	Typ	Max	Unit
Voltage Output Range	RL=10kΩ	0		AVDD-0.4	V
Output Load Regulation Accuracy	RL=2kΩ to 10kΩ		0.1	0.25	%of FS

Reference Inputs

Parameter	Condition		Min	Typ	Max	Unit
Input Voltage Range	See Note 10		0		AVDD-1.5	V
Reference Feed Through	REFIN = 1Vpp(1 kHz) + 1.024 V (See Note 11)			-75		dB
Reference Input Bandwidth	REFIN = 0.2Vpp+ 1.024 V	Slow		0.5		MHz
		Fast		1		

Note:

10. Reference input voltage over VDD/2 will cause output saturation distortion.

11. Reference feed through refers to the analog output rejection ratio when the output number is zero and REFIN = 1Vpp (1 kHz) +1.024V.

Digital Inputs

Parameter	Condition	Min	Typ	Max	Unit
High-level Digital Input Current	VI＝VDD			±1	uA
Low-level Digital Input Current	VI＝0V			±1	uA

Power Supply

Parameter	Condition		Min	Typ	Max	Unit
Power Supply Current	5-V supply,No load Clock running, All inputs 0 V or VDD	Slow		1.6	2.4	mA
		Fast		3.8	5.6	
	3-V supply,No load Clock running, All inputs 0 V or VDD	Slow		1.2	1.6	mA
		Fast		3.2	4.8	
Power Down Supply Current				10		nA

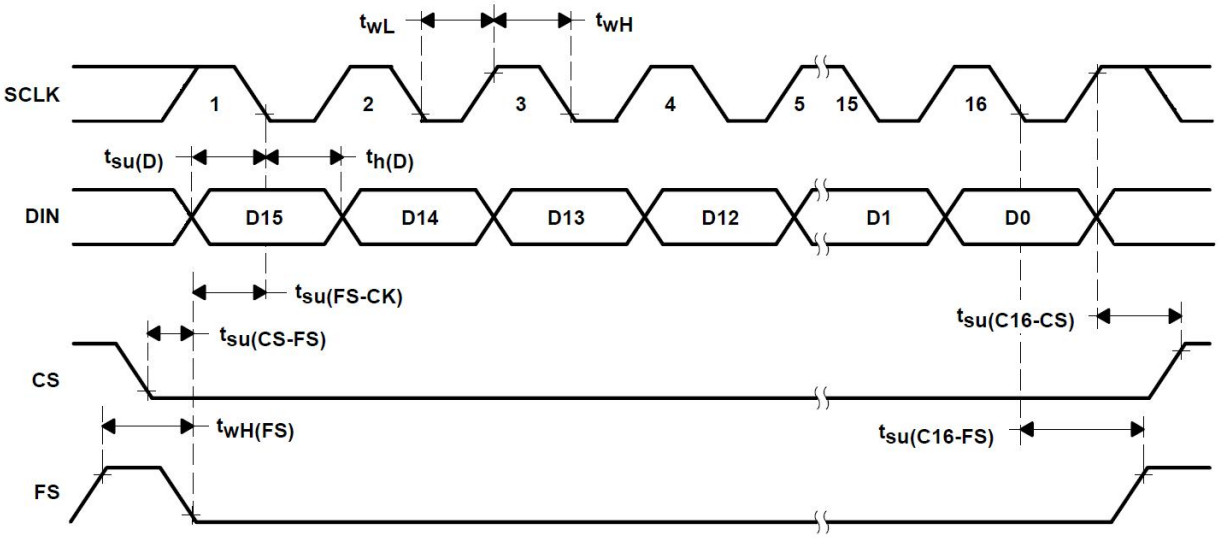
Analog Output Dynamic Performance

Parameter	Condition		Min	Typ	Max	Unit
SR	CL=100pF,RL=10kΩ,Vo=10% to 90%，Vref=2.048,1.024	Slow		5		V/us
		Fast		1		
Ts	to ±0.5LSB,CL=100pF,RL=10kΩ	Slow		3	5.5	V/us
		Fast		9	20	
Ts(c)	to ±0.5LSB,CL=100pF,RL=10kΩ	Slow		1		us
		Fast		2		
Glitch Energy	from 7FF to 800			10		nV-sec
SNR	Vref=1.024@3V；Vref=2.048@5V,fs=400KSPS,fout=1.1kHz sinewave,CL=100pF,RL=10kΩ,BW=20kHz			74		dB
S/(N+D)				66		
THD				-68		
SFDR				70		

Digital Input Timing Requirements

		Min	Typ	Max	Unit
tsu(CS–FS)	Setup time, CS low before FS falling	10			ns
tsu(FS–CK)	FS low before first negative SCLK edge	8			ns
tsu(C16–FS) of FS	sixteenth negative SCLK edge after FS low on which bit D0 is sampled before rising edge of FS	10			ns
tsu(C16–CS)	The first positive SCLK edge after D0 is sampled before CS rising edge. If FS is used instead of the SCLK positive edge to update the DAC, then the setup time is between the FS rising edge and CS rising edge.	10			ns
twH	SCLK high Pulse duration,	25			ns
twL	SCLK low Pulse duration,	25			ns
tsu(D)	data ready before SCLK falling edge	8			ns
th(D)	data held valid after SCLK falling edge	5			ns
twH(FS)	FS high Pulse duration	20			ns

Timing Diagram



APPLICATIONS INFORMATION

Functional Description

MS5614/5614T is a 12-bit single-power digital-to-analog converter. Its architecture uses a resistance array structure, which integrates serial interface, rate and interrupt logic control, reference input buffer, resistance string and output track-to-track amplifier.

The output voltage can be expressed as:

$$Vout=2x\frac{VREFxD}{2^{12}}$$

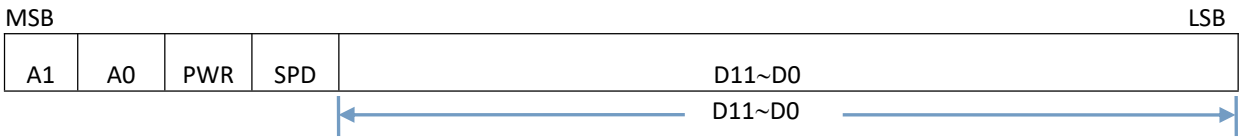
Serial Interface

MS5614/5614T must be set to be valid at low CS level, then the internal DAC updates the corresponding output level at the beginning of bitwise input data (starting at high level) along the descent of FS, after 16 bits have been transferred or when FS becomes higher.

The MS5614/5614T serial port can use two basic modes: four-wire (using chip-selected CS) and three-wire (not using chip-selected CS), which allows multiple devices to connect to the serial port German data source.

Data Format

The data digits of MS5614/5614T consist of two parts: control bits (D15-D12) and digital data (D11-D0).



Data Bits

PWR: Power consumption control, 1 in off mode, 0 in normal mode

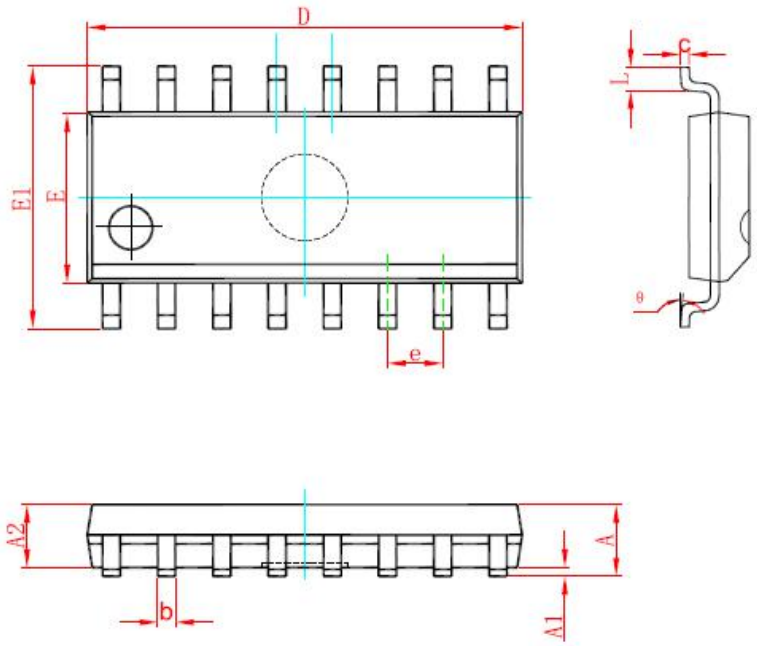
SPD: Rate control, 1 for fast mode, 0 for slow mode

A1, A0 are the internal DAC channel address selection bits, the true value table is as follows:

A1	A0	DAC Addres
0	0	DAC-A
0	1	DAC-B
1	0	DAC-C
1	1	DAC-D

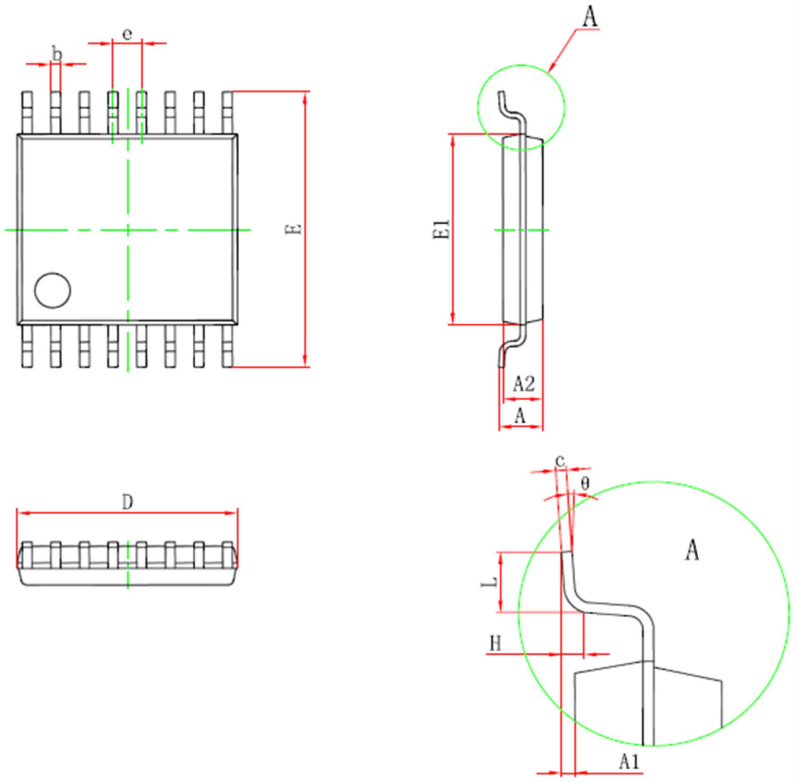
PACKAGE OUTLINE DIMENSIONS

SOP16



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

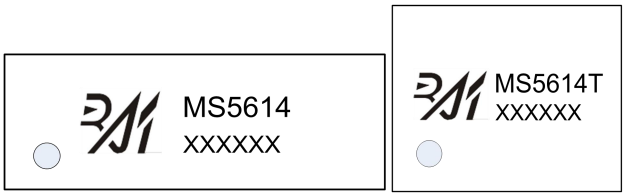
TSSOP16



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
D	4.900	5.100	0.193	0.201
E	6.250	6.550	0.246	0.258
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	4.300	4.500	0.169	0.177
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65(BSC)		0.026(BSC)	
L	0.400	1.270	0.016	0.050
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description



Product Name: MS5614,MS5614T

Product Code: XXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specifications

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS5614	SOP16	2500	1	2500	8	20000
MS5614T	TSSOP16	3000	1	3000	8	24000

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MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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