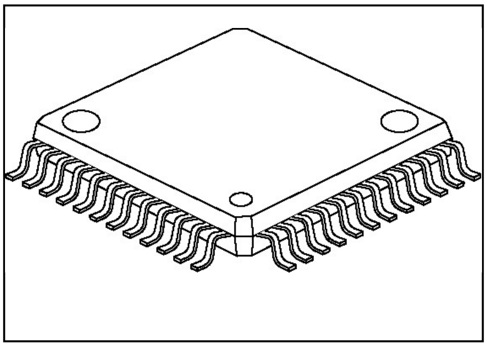
8-channel x 3 Constant Current LED Sink Driver

Features

- 24 constant-current output channels
- Constant output current invariant to load voltage change
- 256-step run-time programmable output current gain control
- Output current adjusted through three external resistors
- Constant output current range: 10 -60 mA
- Excellent output current accuracy:
  between channels: < ±5% (max.), and
  between ICs: < ±6% (max.)
- 25MHz clock frequency
- Schmitt trigger input
- 3.3V / 5V supply voltage
- Optional for "Pb-free & Green" Package

Low Profile Quad Flat Pack (LQFP)



GLQ: 48L (7 x 7 mm^2)

Current Accuracy		Conditions
Between Channels	Between ICs	
< ±5%	< ±6%	I_{OUT} = 10 ~ 60 mA, V_{DS} = 0.8V

Product Description

MBI5368 is designed for fine pitch LED display applications and exploits PrecisionDrive™ technology to provide uniform and constant current sinks for driving LEDs within a large range of V_F variations. In one package, MBI5368 incorporate three 8-channel drivers that output current can be adjusted through three external resistors and moreover be programmable to 256 gain steps for LED white balance

MBI5368 provides users with great flexibility and small package while using surface mounted RGB LEDs to display precisely video color. Users may adjust the output current from 10 mA to 60 mA through separately external resistor R_{ext} and 8-bit current gain control, which gives users flexibility in the color correction of LEDs.

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Applications

Indoor/outdoor LED video display

Typical Application Circuit

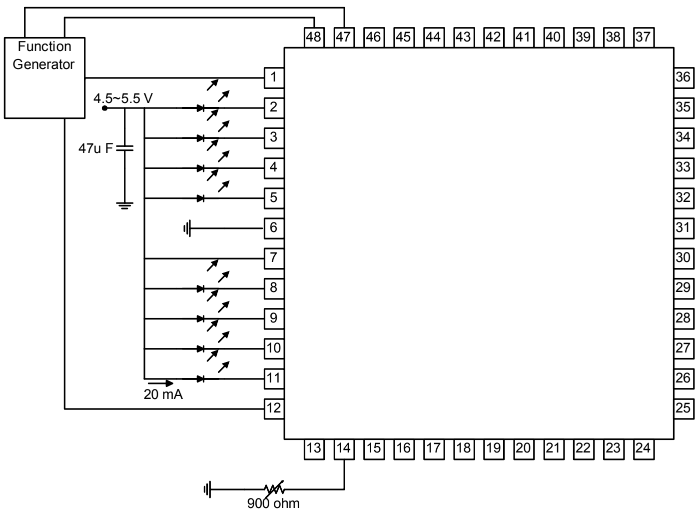


Figure 1

Pin Configuration

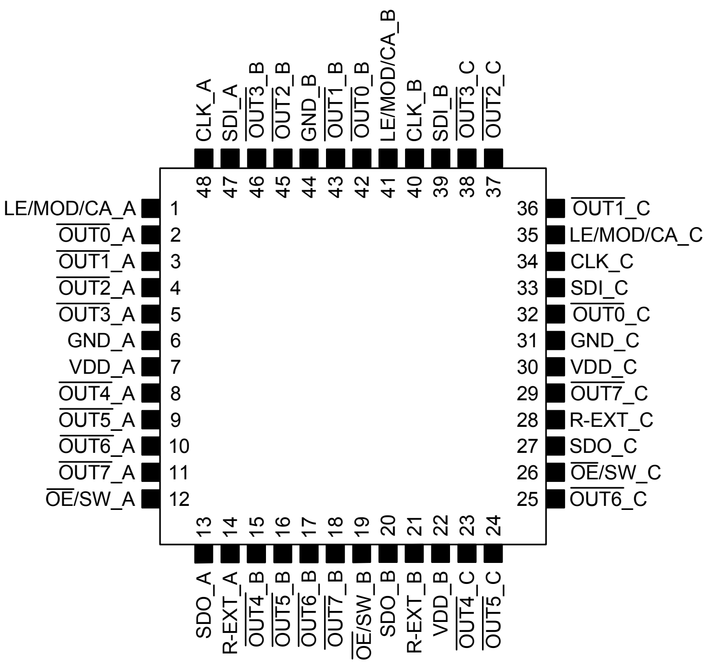


Figure 2

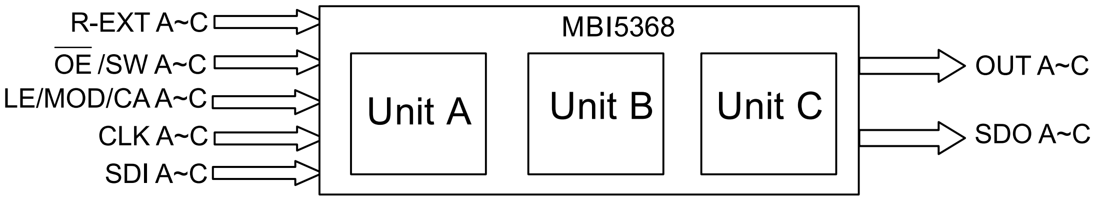
Terminal Description

Pin No.	Pin Name	Function
6, 44, 31	GND_A, GND_B, GND_C	Ground terminal for control logic and current sinks
47, 39, 33	SDI_A, SDI_B, SDI_C	Serial-data input to the shift register
48, 40, 34	CLK_A, CLK_B, CLK_C	Clock input terminal for data shift on rising edge
1, 41, 35	LE/MOD/CA_A, LE/MOD/CA _B, LE/MOD/CA _C	**Output channel data strobe input terminal:** in the Normal Mode phase, serial data in the Shift Register is transferred to the respective Output Latch when LE/MOD/CA is high; the data is latched inside the Output Latch when LE/MOD/CA goes low. If the data in the Output Latch is “1” (High), the respective output channel will be enabled after $\overline{OE}$ /SW is pulled down to low. **Mode selection input terminal:** in the Mode Switching phase, LE/MOD/CA couldn’t strobe serial data but its level is used for determining the next mode to which MBI5170 is going to switch. When LE/MOD/CA is high, the next mode is the Current Adjust Mode; when low, the next mode is the Normal Mode. **Configuration data strobe input terminal:** in the Current Adjust Mode phase, serial data is latched into the Configuration Latch, instead of the Output Latch in the Normal Mode. The serial data here is regarded as the Configuration Code, which affect the output current level of all channels. (See **Operation Principle**)
2-5, 8-11, 15-18, 23-25, 32, 36-38, 42, 43, 45, 46	$\overline{OUT0}$ _A ~ $\overline{OUT7}$ _A, $\overline{OUT0}$ _B ~ $\overline{OUT7}$ _B, $\overline{OUT0}$ _C ~ $\overline{OUT7}$ _C	Constant current output terminals
12, 19, 26	$\overline{OE}$ /SW_A, $\overline{OE}$ /SW_B, $\overline{OE}$ /SW_C	**Output enable terminal:** no matter in what phase MBI5368 operates, the signal $\overline{OE}$ /SW can always enable output drivers to sink current. When its level is (active) low, the output drivers are enabled; when high, all output drivers are turned OFF (blanked). **Mode switching trigger terminal:** a one-clock-wide short signal pulse of $\overline{OE}$ /SW could put MBI5368 into the Mode Switching phase. (See **Operation Principle**)
13, 20, 27	SDO_A, SDO_B, SDO_C	Serial-data output to the following SDI of next driver IC
14, 21, 28	R-EXT_A, R-EXT_B, R-EXT_C	Input terminal used to connect an external resistor for setting up output current for all output channels
7, 22, 30	VDD_A, VDD_B, VDD_C	3.3V / 5V supply voltage terminal

In MBI5368, the relationship between the functions of pin1, 41, 35 and pin12, 19, 26 and the operation phases is listed below:

Pin No.	Pin Name	Function	Normal Mode	Mode Switching	Current Adjust Mode
1, 41, 35	LE/MOD/CA	LE: latching serial data into the Output Latch	Yes	No	No
		MOD: mode selection	No	Yes	No
		CA: latching serial data into the Configuration Latch	No	No	Yes
12, 19, 26	$\overline{OE}$ /SW	$\overline{OE}$: enabling the current output drivers	Yes	Yes	Yes
		SW: entering the Mode Switching phase	Yes	Yes	Yes

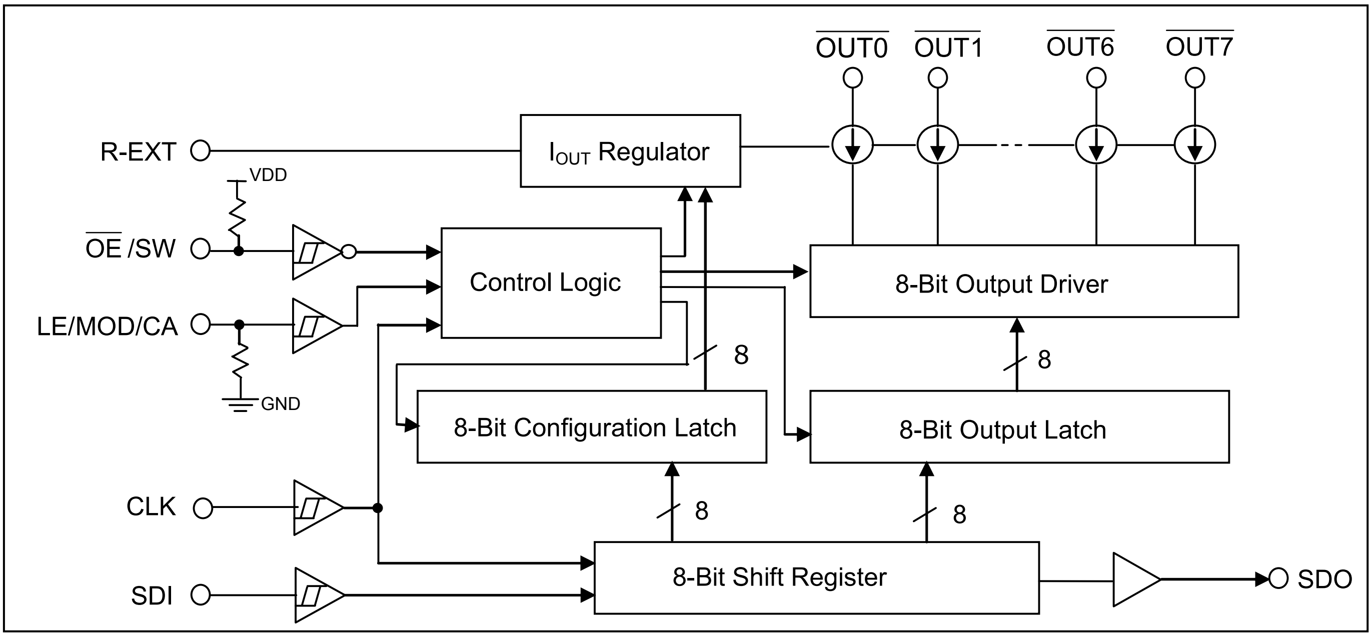
Block Diagram*



* 1. MBI5368 contains three 8-channel constant-current drivers in one package, named as "Unit A", "Unit B", "Unit C". As shown in Pin Configuration, all pins are clearly divided into three groups. To make clear descriptions, the pin names would not be limited to one specific group in the rest of the contents, but all info can be applied to the three groups.

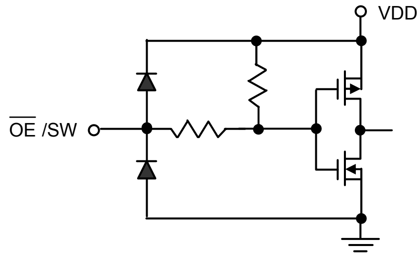
2. The block diagram of each unit is shown as below.

Basic Unit

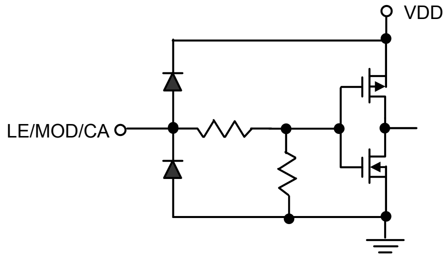


Equivalent Circuits of Inputs and Outputs

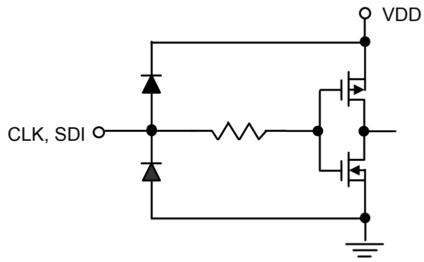
$\overline{\text{OE}}$ /SW Terminal



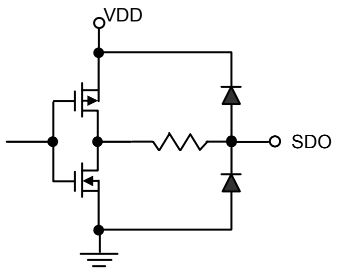
LE/MOD/CA Terminal



CLK, SDI Terminal

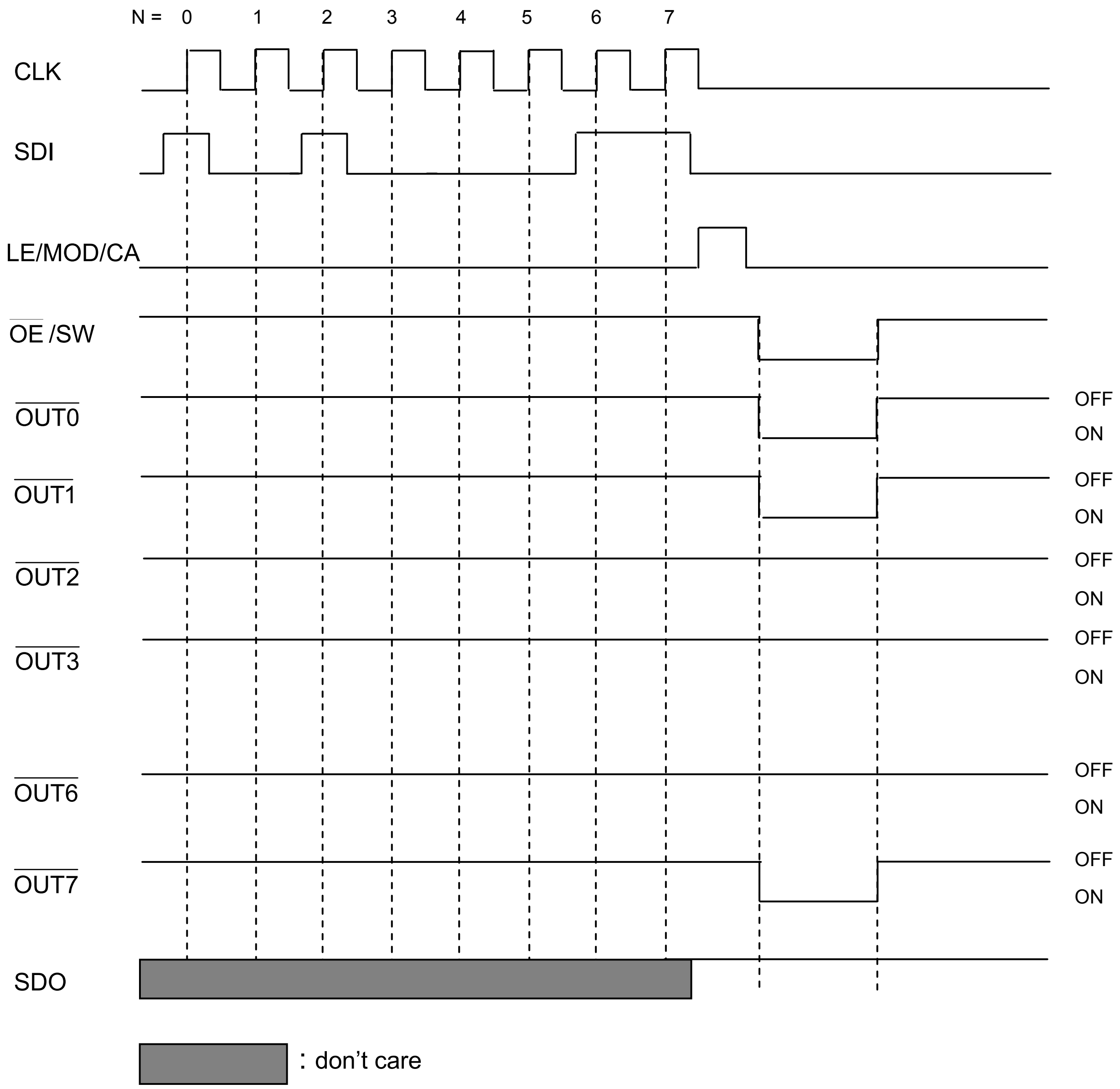


SDO Terminal



Timing Diagram

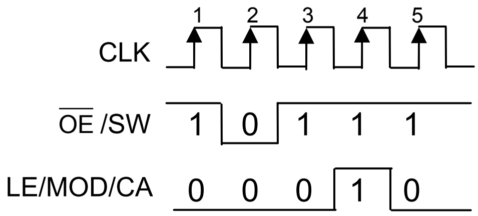
Normal Mode



Truth Table (In Normal Mode)

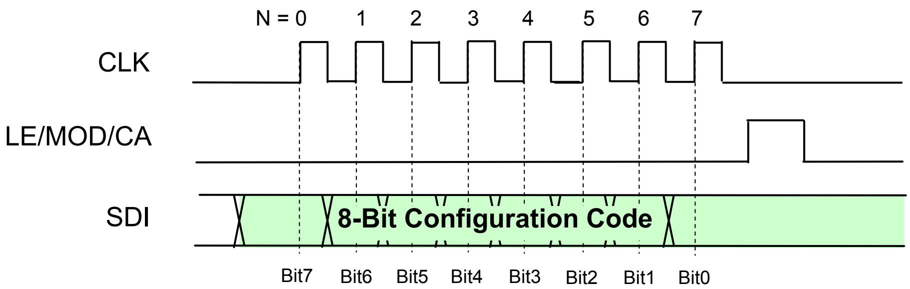
CLK	LE/MOD/CA	$\overline{OE}$ /SW	SDI	$\overline{OUT0}$ … $\overline{OUT5}$ … $\overline{OUT\ 7}$	SDO
↑	H	L	D_n	$\overline{D_n}$ ….. $\overline{D_{n-5}}$ …. $\overline{D_{n-7}}$	D_{n-7}
↑	L	L	D_{n+1}	No Change	D_{n-6}
↑	H	L	D_{n+2}	$\overline{D_{n+2}}$ …. $\overline{D_{n-3}}$ …. $\overline{D_{n-5}}$	D_{n-5}
↓	X	L	D_{n+3}	$\overline{D_{n+2}}$ …. $\overline{D_{n-3}}$ …. $\overline{D_{n-5}}$	D_{n-5}
↓	X	H	D_{n+3}	Off	D_{n-5}

Switching to Current Adjust Mode



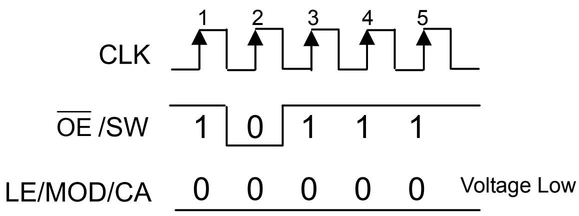
The above shows an example of the signal sequence that can set the next operation mode of MBI5368 to be the Current Adjust Mode. The LE/MOD/CA active pulse here would not latch any serial data.

Writing Configuration Code (In Current Adjust Mode)



In the Current Adjust Mode, by sending the positive pulse of LE/MOD/CA, the content of the Shift Register with a Configuration Code will be written to the 8-bit Configuration Latch.

Switching to Normal Mode



The above signal sequence example can make MBI5368 resume to the Normal Mode.

Note:

If users want to know the whole process, that is how to enter the Current Adjust Mode, write the Configuration Code, and resume to the Normal Mode, please refer to the section **Operation Principle**.

Maximum Ratings

Characteristic		Symbol	Rating	Unit
Supply Voltage		V_{DD}	0 ~ 7.0	V
Input Voltage		V_{IN}	-0.4 ~ V_{DD}+0.4	V
Output Current		I_{OUT}	60	mA
Output Voltage		V_{DS}	-0.5 ~ +20.0	V
Clock Frequency		F_{CLK}	25	MHz
GND Terminal Current		I_{GND}	1440	mA
Power Dissipation (On PCB, Ta=25°C)	GLQ – type	P_D	-	W
Operating Temperature		T_{opr}	-40 ~ +85	°C
Storage Temperature		T_{stg}	-55 ~ +150	°C

Electrical Characteristics (V_{DD}= 5V)

Characteristic		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		4.5	5.0	5.5	V
Output Voltage		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT7}$		-	-	17.0	V
Output Current		I_{OUT}	$\overline{OUT0}$ ~ $\overline{OUT7}$, CM =1, V_{DD} =5V		10	-	60	mA
		I_{OUT}	$\overline{OUT0}$ ~ $\overline{OUT7}$, CM =0, V_{DD} =5V		5	-	40	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta = -40~85ºC		0.7*V_{DD}	-	V_{DD}+0.3	V
	"L" level	V_{IL}	Ta = -40~85ºC		GND	-	0.3*V_{DD}	V
Output Leakage Current			V_{DS} = 17.0V and channel off		-	-	0.5	μA
Output Voltage	SDO	V_{OL}	I_{OL} = +1.0mA		-	-	0.4	V
		V_{OH}	I_{OH} = -1.0mA		4.6	-	-	V
Output Current 1		I_{OUT1}	V_{DS} = 0.5V; R_{ext} = 744Ω; VG* = 0.992; CM = 1		-	25.26	-	mA
Current Skew (between channels)		dI_{OUT1}	I_{OUT} = 25.26mA $V_{DS} \geq$ 0.5V	R_{ext} = 744 Ω	-	±2	±5	%
Output Current 2		I_{OUT2}	V_{DS} = 0.6V; R_{ext} = 372Ω; VG* = 0.992; CM = 1		-	50.52	-	mA
Current Skew (between channels)		dI_{OUT2}	I_{OUT} = 50.52mA $V_{DS} \geq$ 0.6V	R_{ext} = 372 Ω	-	±2	±5	%
Output Current vs. Output Voltage Regulation		%/dV_{DS}	V_{DS} within 1.0V and 3.0V		-	±0.1	-	% / V
Output Current vs. Supply Voltage Regulation		%/dV_{DD}	V_{DD} within 4.5V and 5.5V		-	±1	-	% / V
Pull-up Resistor		R_{IN}(up)	$\overline{OE}$ /SW		250	500	800	KΩ
Pull-down Resistor		R_{IN}(down)	LE/MOD/CA		250	500	800	KΩ
Supply Current	"OFF"	I_{DD}(off) 0	R_{ext}=Open, $\overline{OUT0}$ ~ $\overline{OUT7}$ =Off; CM = 1, VG*= 0.992		-	3.3	-	mA
		I_{DD}(off) 1	R_{ext}=744 Ω, $\overline{OUT0}$ ~ $\overline{OUT7}$ =Off; CM = 1, VG* = 0.992		-	5.9	-	
		I_{DD}(off) 2	R_{ext}=372 Ω, $\overline{OUT0}$ ~ $\overline{OUT7}$ =Off; CM = 1, VG*= 0.992		-	8.5	-	
	"ON"	I_{DD}(on) 1	R_{ext}=744 Ω, $\overline{OUT0}$ ~ $\overline{OUT7}$ =On; CM = 1, VG*= 0.992		-	5.9	-	
		I_{DD}(on) 2	R_{ext}=372 Ω, $\overline{OUT0}$ ~ $\overline{OUT7}$ =On; CM = 1, VG*= 0.992		-	8.5	-	

* In the above table, VG is the programmable gain of the voltage at the terminal R-EXT. The detail description could be found in the section **Operation Principle**.

Electrical Characteristics (V_{DD}= 3.3V)

Characteristic		Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-	3.0	3.3	3.6	V
Output Voltage		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT7}$	-	-	17.0	V
Output Current		I_{OUT}	$\overline{OUT0}$ ~ $\overline{OUT7}$, CM=1	10	-	60	mA
		I_{OUT}	$\overline{OUT0}$ ~ $\overline{OUT7}$, CM=0	5	-	40	mA
		I_{OH}	SDO	-	-	-1.0	mA
		I_{OL}	SDO	-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta = -40~85ºC	0.7*V_{DD}	-	V_{DD}	V
	"L" level	V_{IL}	Ta = -40~85ºC	GND	-	0.3*V_{DD}	V
Output Leakage Current			V_{DS} = 17.0V and channel off	-	-	0.5	μA
Output Voltage	SDO	V_{OL}	I_{OL} = +1.0mA	-	-	0.4	V
		V_{OH}	I_{OH} = -1.0mA	2.9	-	-	V
Output Current 1		I_{OUT1}	V_{DS} = 0.5V; R_{ext} = 744Ω; VG = 0.992; CM = 1	-	25.26	-	mA
Current Skew (between channels)		dI_{OUT1}	I_{OUT} = 25.26mA $V_{DS} \geq$ 0.5V; R_{ext} = 744 Ω	-	±2	±5	%
Output Current 2		I_{OUT2}	V_{DS} = 0.6V; R_{ext} = 372Ω; VG = 0.992; CM = 1	-	50.52	-	mA
Current Skew (between channels)		dI_{OUT2}	I_{OUT} = 50.52mA $V_{DS} \geq$ 0.6V; R_{ext} = 372 Ω	-	±2	±5	%
Output Current vs. Output Voltage Regulation		%/dV_{DS}	V_{DS} within 1.0V and 3.0V	-	±0.1	-	% / V
Output Current vs. Supply Voltage Regulation		%/dV_{DD}	V_{DD} within 3.2V and 3.6V	-	±1	-	% / V
Pull-up Resistor		R_{IN}(up)	$\overline{OE}$ /SW	250	500	800	KΩ
Pull-down Resistor		R_{IN}(down)	LE/MOD/CA	250	500	800	KΩ
Supply Current	"OFF"	I_{DD}(off) 0	R_{ext}=Open, $\overline{OUT0}$ ~ $\overline{OUT7}$ =Off; CM = 1, VG= 0.992	-	0.87	-	mA
		I_{DD}(off) 1	R_{ext}=744 Ω, $\overline{OUT0}$ ~ $\overline{OUT7}$ =Off; CM = 1, VG= 0.992	-	3.7	-	
		I_{DD}(off) 2	R_{ext}=372 Ω, $\overline{OUT0}$ ~ $\overline{OUT7}$ =Off; CM = 1, VG= 0.992	-	6.37	-	
	"ON"	I_{DD}(on) 1	R_{ext}=744 Ω, $\overline{OUT0}$ ~ $\overline{OUT7}$ =On; CM = 1, VG= 0.992	-	3.4	-	
		I_{DD}(on) 2	R_{ext}=372 Ω, $\overline{OUT0}$ ~ $\overline{OUT7}$ =On; CM = 1, VG= 0.992	-	6.1	-	

Switching Characteristics (V_{DD}= 5.0V)

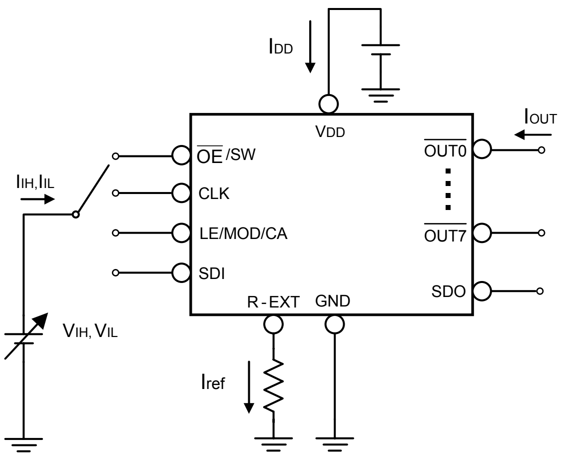
Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation Delay Time ("L" to "H")	CLK - $\overline{\text{OUTn}}$	t_{pLH1}	Test Circuit for Switching Characteristics V_{DD}=5.0 V V_{DS}=0.8 V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=372 Ω V_L=4.0 V R_L=64 Ω C_L=10 pF VG = 0.992 CM = 1	-	100	150	ns
	LE/MOD/CA - $\overline{\text{OUTn}}$	t_{pLH2}		-	100	150	ns
	$\overline{\text{OE}}$ /SW - $\overline{\text{OUTn}}$	t_{pLH3}		-	100	150	ns
	CLK - SDO	t_{pLH}		20	25	30	ns
Propagation Delay Time ("H" to "L")	CLK - $\overline{\text{OUTn}}$	t_{pHL1}		-	100	150	ns
	LE/MOD/CA - $\overline{\text{OUTn}}$	t_{pHL2}		-	100	150	ns
	$\overline{\text{OE}}$ /SW - $\overline{\text{OUTn}}$	t_{pHL3}		-	100	150	ns
	CLK - SDO	t_{pHL}		20	25	30	ns
Pulse Width	CLK	$t_{w(CLK)}$		20	-	-	ns
	LE/MOD/CA	$t_{w(L)}$		20	-	-	ns
	$\overline{\text{OE}}$ /SW (@I_{OUT}< 60mA)	$t_{w(OE)}$		200	-	-	ns
Hold Time for LE/MOD/CA		$t_{h(L)}$		10	-	-	ns
Setup Time for LE/MOD/CA		$t_{su(L)}$		5	-	-	ns
Maximum CLK Rise Time		t_r*		-	-	500	ns
Maximum CLK Fall Time		t_f*		-	-	500	ns
Output Rise Time of V_{OUT} (turn off)		t_{or}		-	120	150	ns
Output Fall Time of V_{OUT} (turn on)		t_{of}		-	200	250	ns
Clock Frequency		F_{CLK}	Cascade Operation	-	-	25.0	MHz

*If the devices are connected in cascade and t_r or t_f is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

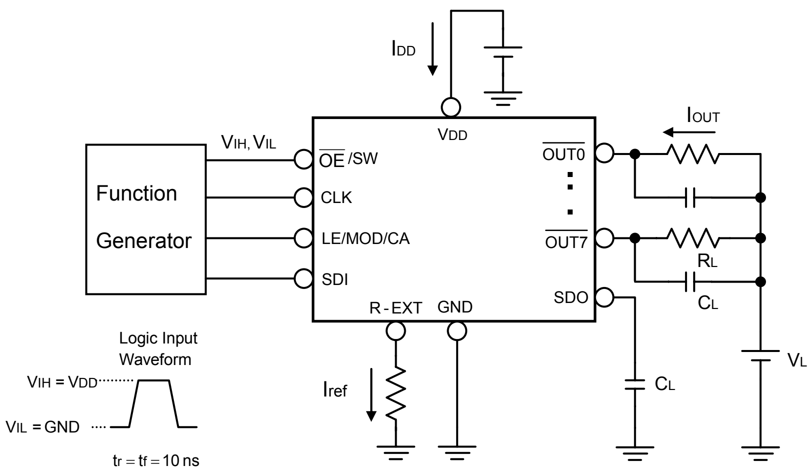
Switching Characteristics (V_{DD}= 3.3V)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation Delay Time ("L" to "H")	CLK - $\overline{\text{OUTn}}$	t_{pLH1}	Test Circuit for Switching Characteristics V_{DD}=3.3 V V_{DS}=0.8 V V_{IH}=V_{DD} V_{IL}=GND R_{ext}=372 Ω V_L=4.0 V R_L=64 Ω C_L=10 pF VG = 0.992 CM = 1	-	100	150	ns
	LE/MOD/CA - $\overline{\text{OUTn}}$	t_{pLH2}		-	100	150	ns
	$\overline{\text{OE}}$ /SW - $\overline{\text{OUTn}}$	t_{pLH3}		-	100	150	ns
	CLK - SDO	t_{pLH}		45	55	65	ns
Propagation Delay Time ("H" to "L")	CLK - $\overline{\text{OUTn}}$	t_{pHL1}		-	130	200	ns
	LE/MOD/CA - $\overline{\text{OUTn}}$	t_{pHL2}		-	130	200	ns
	$\overline{\text{OE}}$ /SW - $\overline{\text{OUTn}}$	t_{pHL3}		-	130	200	ns
	CLK - SDO	t_{pHL}		45	55	65	ns
Pulse Width	CLK	$t_{w(CLK)}$		20	-	-	ns
	LE/MOD/CA	$t_{w(L)}$		20	-	-	ns
	$\overline{\text{OE}}$ /SW (@I_{OUT}< 60mA)	$t_{w(OE)}$		200	-	-	ns
Hold Time for LE/MOD/CA		$t_{h(L)}$		10	-	-	ns
Setup Time for LE/MOD/CA		$t_{su(L)}$		5	-	-	ns
Maximum CLK Rise Time		t_r		-	-	500	ns
Maximum CLK Fall Time		t_f		-	-	500	ns
Output Rise Time of V_{OUT} (turn off)		t_{or}		-	120	150	ns
Output Fall Time of V_{OUT} (turn on)		t_{of}		-	200	400	ns
Clock Frequency		F_{CLK}	Cascade Operation	-	-	12.0	MHz

Test Circuit for Electrical Characteristics

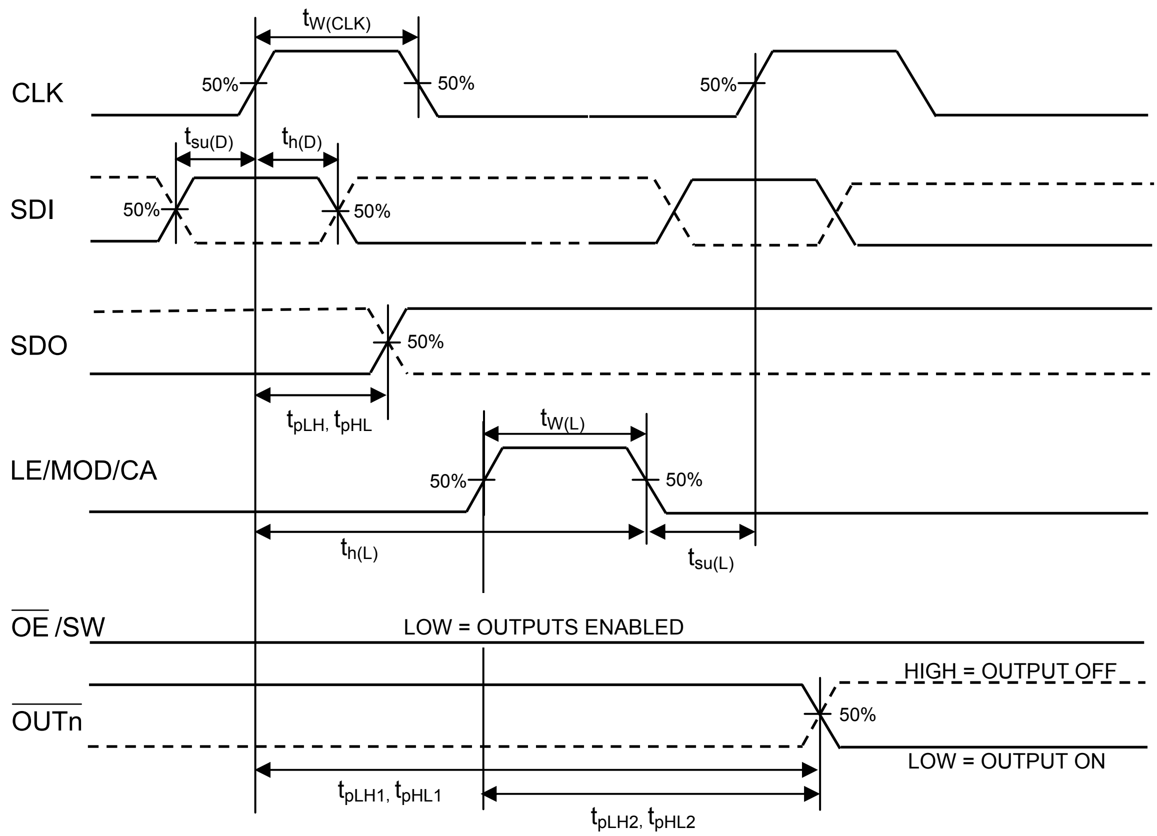


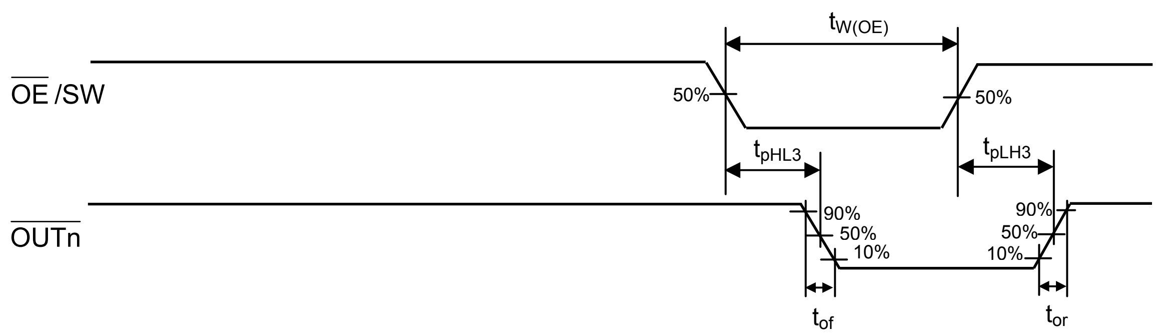
Test Circuit for Switching Characteristics



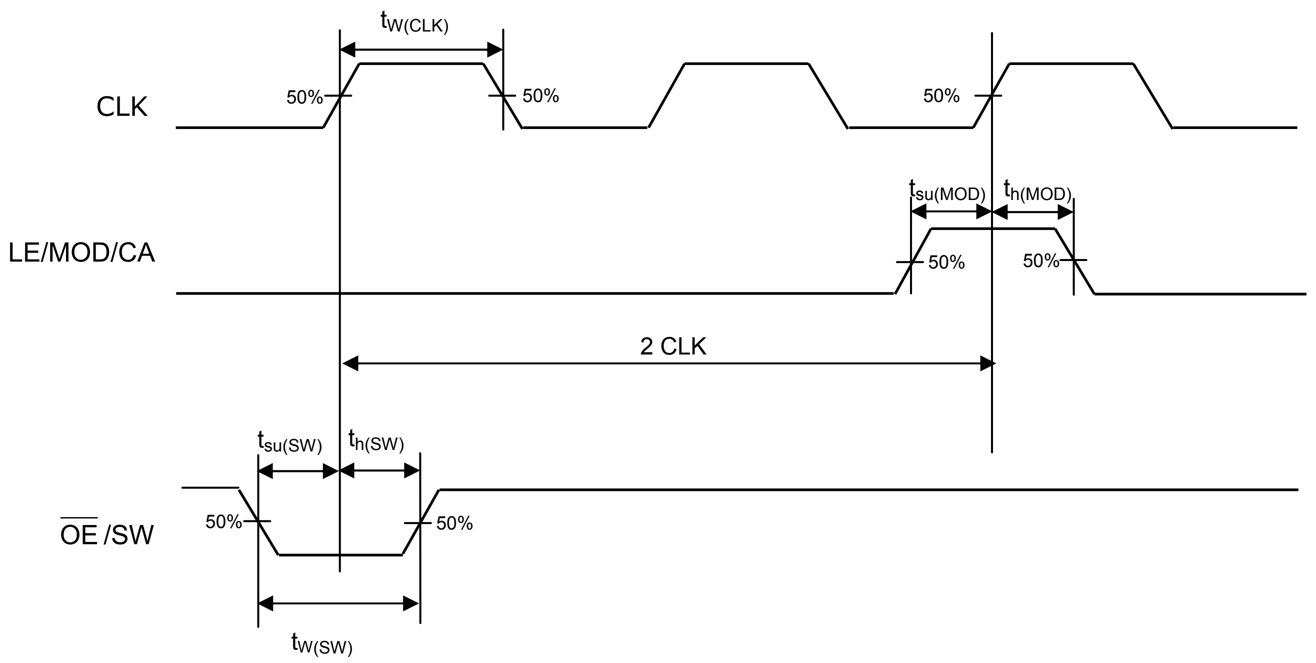
Timing Waveform

Normal Mode and Current Adjust Mode





Switching to Current Adjust Mode

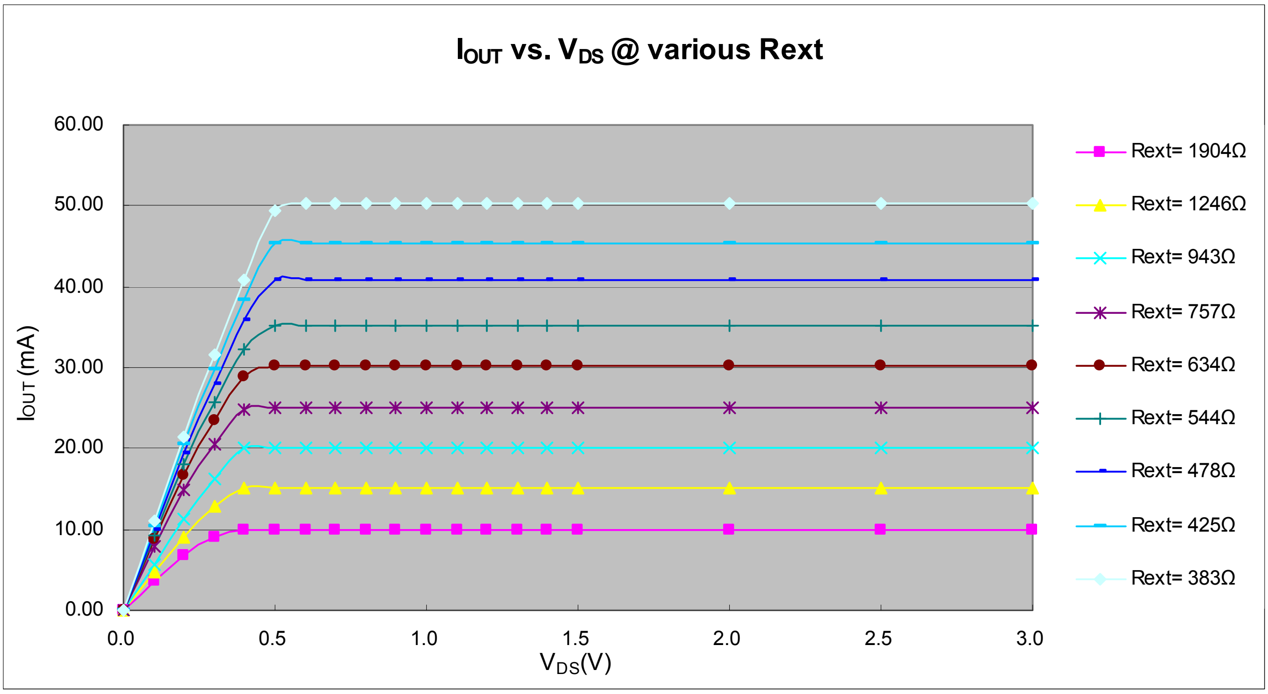


Application Information

Constant Current

In LED display application, MBI5368 provides nearly no variations in current from channel to channel and from IC to IC. This can be achieved by:

1) While $I_{OUT} \leqq$ 60mA, the maximum current variation between channels is less than ±5%, and that between ICs is less than ±6%.
2) In addition, the characteristics curve of output stage in the saturation region is flat and users can refer to the figure as shown below. Thus, the output current can be kept constant regardless of the variations of LED forward voltages (V_F).



Adjusting Output Current

The output current, I_{OUT}, of MBI5368 at each output port can be easily determined by the external resistor, R_{ext}. Users can follow the following formulas to calculate the output current I_{OUT}:

$V_{R\text{-}EXT}$ = 1.25Volt x VG

$I_{rext} = V_{R\text{-}EXT} / R_{ext}$ if another end of the external resistor R_{ext} is connected to ground.

$I_{OUT} = I_{rext}$ x 15 x 3^(CM-1)

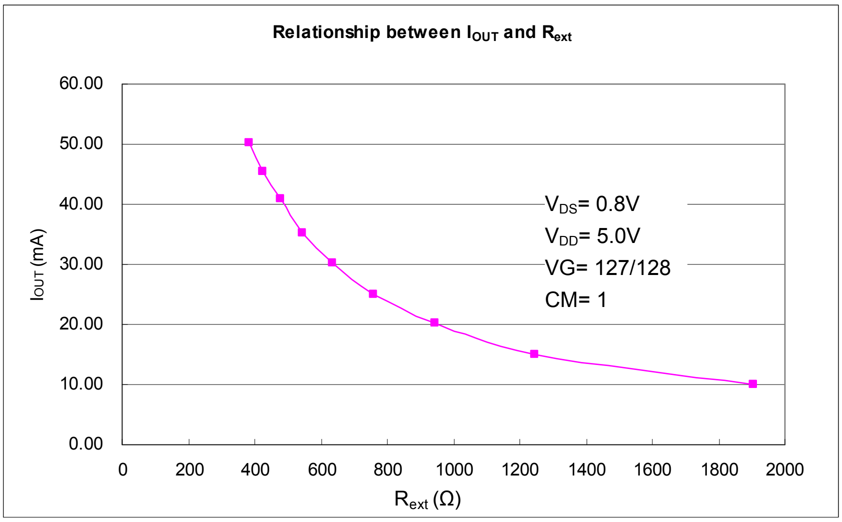
where R_{ext} is the resistance of the external resistor connected to the R-EXT terminal, I_{rext} is the reference current and set by the internal generated voltage, V_{ref}(= 1.25V) and R_{ext}, and $V_{R\text{-}EXT}$ is the voltage of the R-EXT terminal and controlled by the programmable voltage gain VG, which is defined by the Configuration Code. The Current Multiplier, CM, determines the ratio of I_{OUT}/I_{rext}. After power-on, the default value of VG is 127/128 = 0.992 and the default value of CM is 1, so that the ratio I_{OUT}/I_{rext} is 15. Based on the default VG and CM,

$V_{R\text{-}EXT}$ = 1.25Volt x 127/128= 1.24Volt

I_{OUT} = (1.24Volt / R_{ext}) x 15

Hence, the default magnitude of current is around 50.52mA at 372Ω and 25.26mA at 744Ω. The default relationship after power-on between I_{OUT} and R_{ext} is shown in the following figure.

The output current of each channel (I_{OUT}) is set by an external resistor, R_{ext}. The relationship between I_{OUT} and R_{ext} is shown in the following figure.

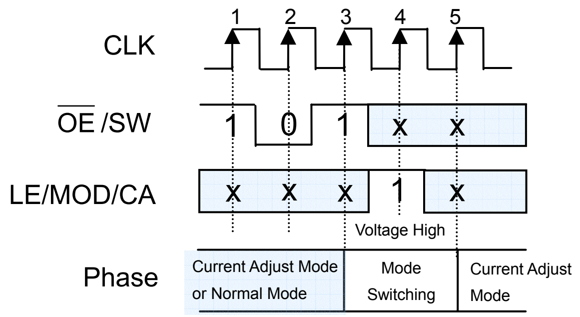


Operation Phases

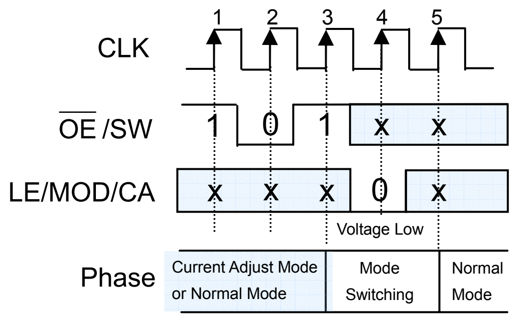
MBI5368 exploits the **Share-I-O™** technique to provide run-time programmable LED driving current in the Current Adjust Mode phase as well as the Normal Mode phase. In order to switch between the two modes, MBI5368 monitors the signal $\overline{OE}$/SW. Once a one-clock-wide pulse of $\overline{OE}$/SW appears, MBI5368 would enter the two-clock-period transition phase---the Mode Switching phase. After power-on, the default operation mode is the Normal Mode.

Operation Mode Switching

Switching to the Current Adjust Mode



Switching to the Normal



As shown in the above figures, once a one-clock-wide short pulse "**101**" of $\overline{OE}$/SW appears, MBI5368 would enter the Mode Switching phase. At the 4th rising edge of CLK, if LE/MOD/CA is sampled as "Voltage High", MBI5368 would switch to the Current Adjust Mode; otherwise, it would switch to the Normal Mode. Worthwhile noticing, the signal LE/MOD/CA between the 3rd and the 5th rising edges of CLK can not latch any data. Its level is just used for determining which mode to switch. However, the short pulse of $\overline{OE}$/SW can still enable the output ports. During the mode switching, the serial data can still be transferred through the pin SDI and shifted out from the pin SDO.

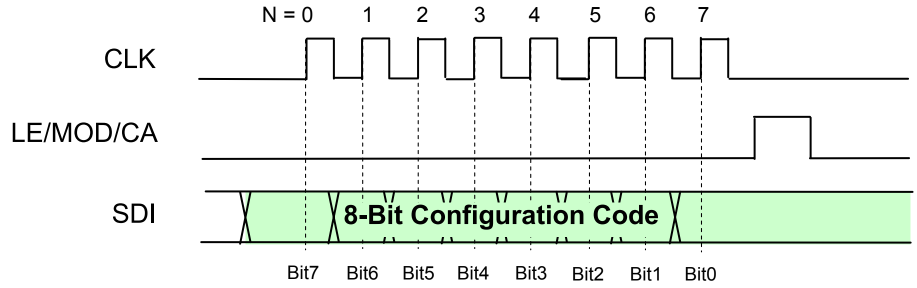
Note:

1. The signal sequence for the mode switching could be frequently used for making sure under which mode MBI5368 is working.
2. The aforementioned "1" and "0" are sampled at the rising edge of CLK. The "X" means its level would not affect the result of mode switching mechanism.

Normal Mode Phase

MBI5368 in the Normal Mode phase has similar functionality to MBI5168. The only difference is short pulse $\overline{OE}$/SW signal monitoring. The short pulse would trigger MBI5368 to switch its operation mode. However, as long as the signal LE/MOD/CA is not Voltage High in the Mode Switching phase, MBI5368 would still remain in the Normal Mode as if no mode switching occurs.

Current Adjust Mode Phase and Writing Configuration Code



In the Current Adjust Mode phase, the serial data could be transferred into MBI5368 via the pin SDI, shifted in the Shift Register, and go out via the pin SDO. The active low signal $\overline{OE}$/SW can enable the output drivers to sink current. These are the same as those in the Normal Mode. The difference is that the active high signal LE/MOD/CA latches the serial data in the Shift Register to the Configuration Latch, instead of the Output Latch. The latched serial data is regarded as the Configuration Code. The code would be memorized until power off or the Configuration Latch is re-written. As shown above, the timing for writing the Configuration Code is the same as that in the Normal Mode for latching output channel data.

8-Bit Configuration Code and Current Gain CG

	Bit Definition of 8-Bit Configuration Code							
	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Meaning	CM	HC	CC0	CC1	CC2	CC3	CC4	CC5
Default Value	1	1	1	1	1	1	1	1

Bit definition of the Configuration Code in the Configuration Latch is shown above. Bit 7 is first sent into MBI5368 via the pin SDI. Bit 1 ~ 7, {HC, CC[0:5]}, would determine the voltage gain (VG), that affects the voltage at R-EXT terminal and indirectly the reference current I_{rext} flowing through the external resistor at terminal R-EXT. Bit 0 is the Current Multiplier (CM) bit, that determines the ratio I_{out}/I_{rext}. Each combination of VG and CM would give a Current Gain (CG).

- VG: the relationship between {HC,CC[0:5]} and the Voltage Gain G can be formulated as below:

  $VG = (1 + HC) \times (1 + D/64) / 4$

  $D = CC0 \times 2^5 + CC1 \times 2^4 + CC2 \times 2^3 + CC3 \times 2^2 + CC4 \times 2^1 + CC5 \times 2^0$

  where HC is 1 or 0, and D is the binary value of CC[0:5]. So, the VG could be regarded as a floating-point number with one bit exponent HC and 6-bit mantissa CC[0:5]. {HC,CC[0:5]} divides the programmable voltage gain VG into 128 steps and two sub-bands:

  Low voltage sub-band (HC=0): VG = 1/4 ~ 127/256, linearly divided into 64 steps;

  High voltage sub-band (HC=1): VG = 1/2 ~ 127/128, linearly divided into 64 steps, too.

- CM: as well as determining the ratio I_{out}/I_{rext}, the CM bit would limit the output current range.

  High Current Multiplier (CM=1): I_{out}/I_{rext} = 15 and suitable for output current range I_{out} = 10 ~ 60mA.

  Low Current Multiplier (CM=0): I_{out}/I_{rext} = 5 and suitable for output current range I_{out} = 5 ~ 40mA.

- CG: the total Current Gain is defined as the following.

$V_{R\text{-}EXT}$ = 1.25Volt * VG

$I_{rext} = V_{R\text{-}EXT} / R_{ext}$ if another end of the external resistor R_{ext} is connected to ground.

$I_{out} = I_{rext}$ * 15 * 3^(CM-1) = 1.25Volt / R_{ext} * VG * 15 * 3^(CM-1) = (1.25Volt / R_{ext} * 15) * CG

We define CG = VG * 3^(CM-1). Hence CG = (1/12) ~ (127/128) and it is divided into 256 steps, totally. If CG = 127/128 = 0.992, the I_{out}-R_{ext} relationship is similar to that in MBI5168.

For example,

a) When the Configuration Code {CM, HC, CC[0:5]} = {1,1,111111},

VG = 127/128 = 0.992; and CG = VG * 3^0 = VG = 0.992

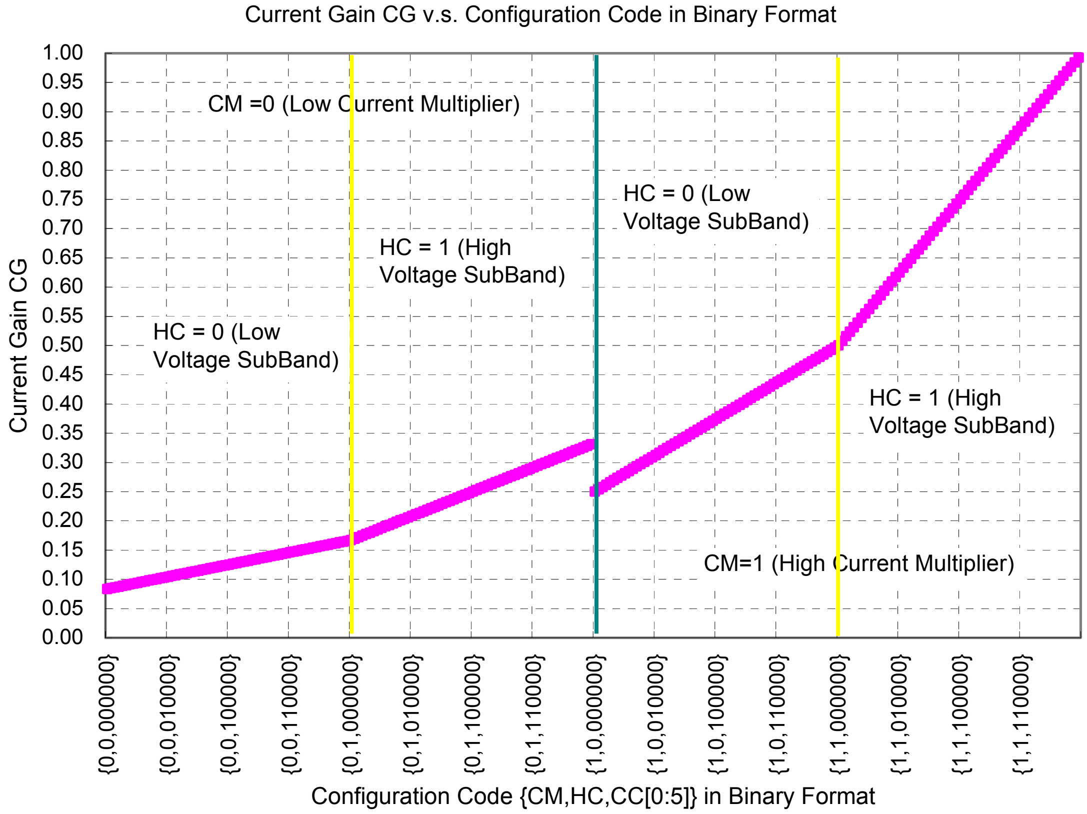
b) When the Configuration Code is {1,1,000000},

VG = (1+1)*(1+0/64)/4 = 1/2 = 0.5; and CG = 0.5

c) When the Configuration Code is {0,0,000000},

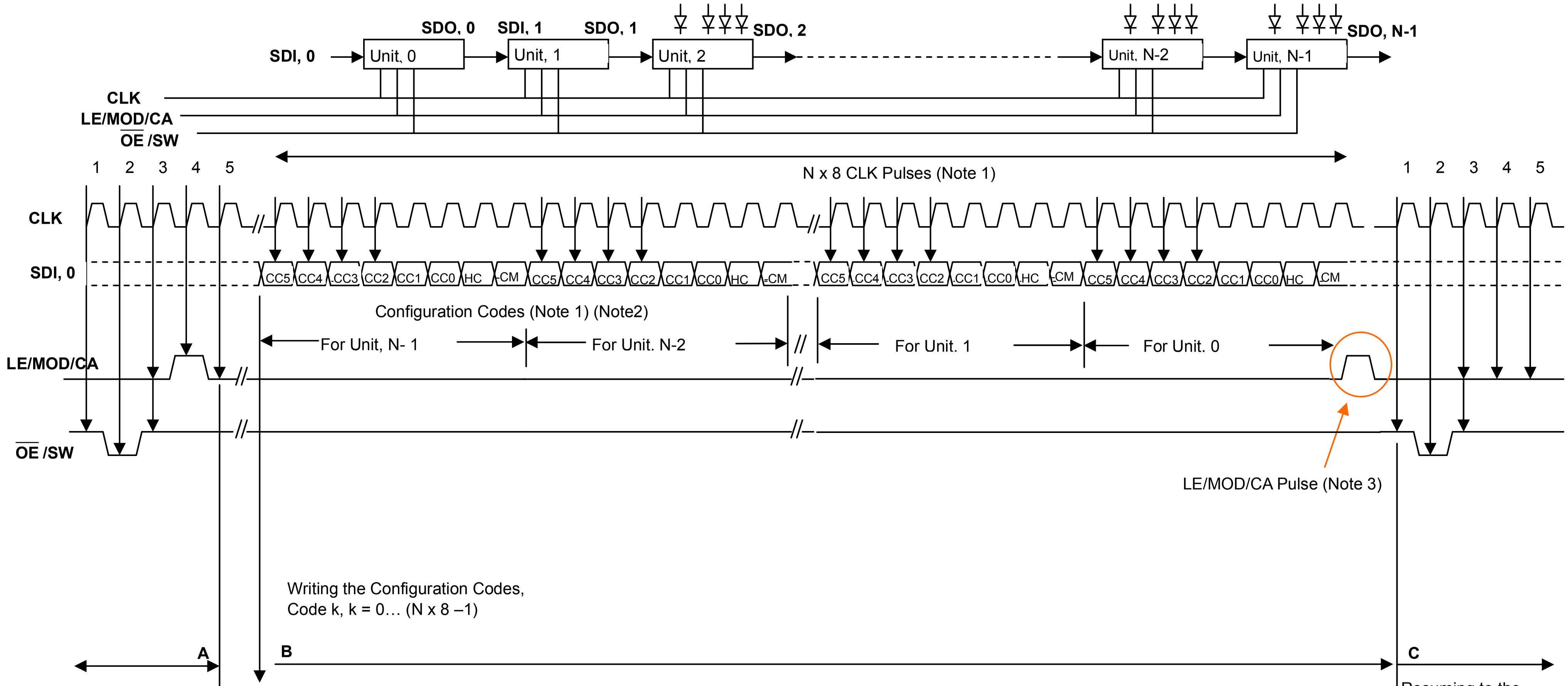
VG = (1+0)*(1+ 0/64)/4 = 1/4; and CG = (1/4)*3^-1 = 1/12

After power on, the default value of the Configuration Code {CM, HC, CC[0:5]} is {1,1,111111}. Thus, VG = CG = 0.992. The relationship between the Configuration Code and the Current Gain CG is shown in the following.



Timing Chart for Current Adjust Mode (An Example)

N of MBI5368 are connected in cascade, i.e., SDO, k --> SDI, k+1.
And, all MBI5368 are connected to the same signal bus CLK, LE/MOD/CA and $\overline{OE}$ /SW.



Entering the Current Adjust Mode

N x 8CLK pulses are required to shift the 8-bit Configuration Codes needed by N x Unit.

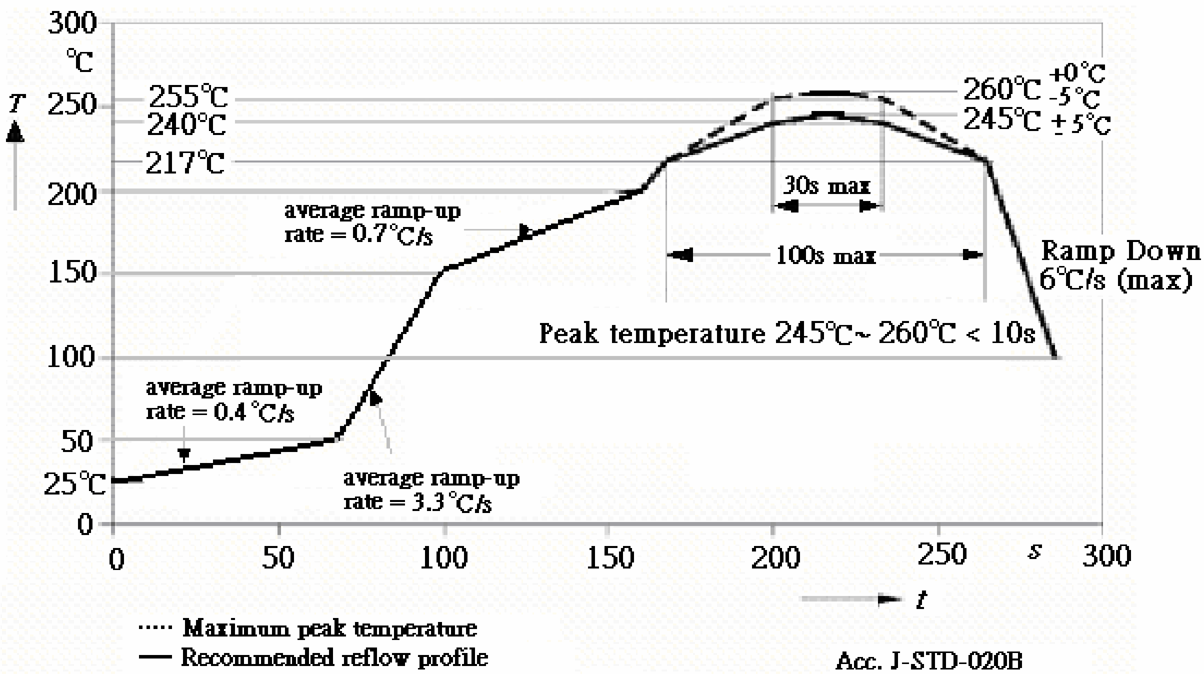
Note 2:
Voltage Gain VG = (1+ HC) x (1 + D/64)/4
D = CC0 x 2^5+ CC1 x 2^4 + CC2 x 2^3 + CC3 x 2^2 + CC4 x 2^1 + CC5 x 2^0 .
Current Gain CG = VG * 3^(CM-1)

Note 3:
The LE/MOD/CA pulse writes the Configuration Codes to each unit.

Resuming to the Normal Mode

Soldering Process of "Pb-free & Green" Package Plating*

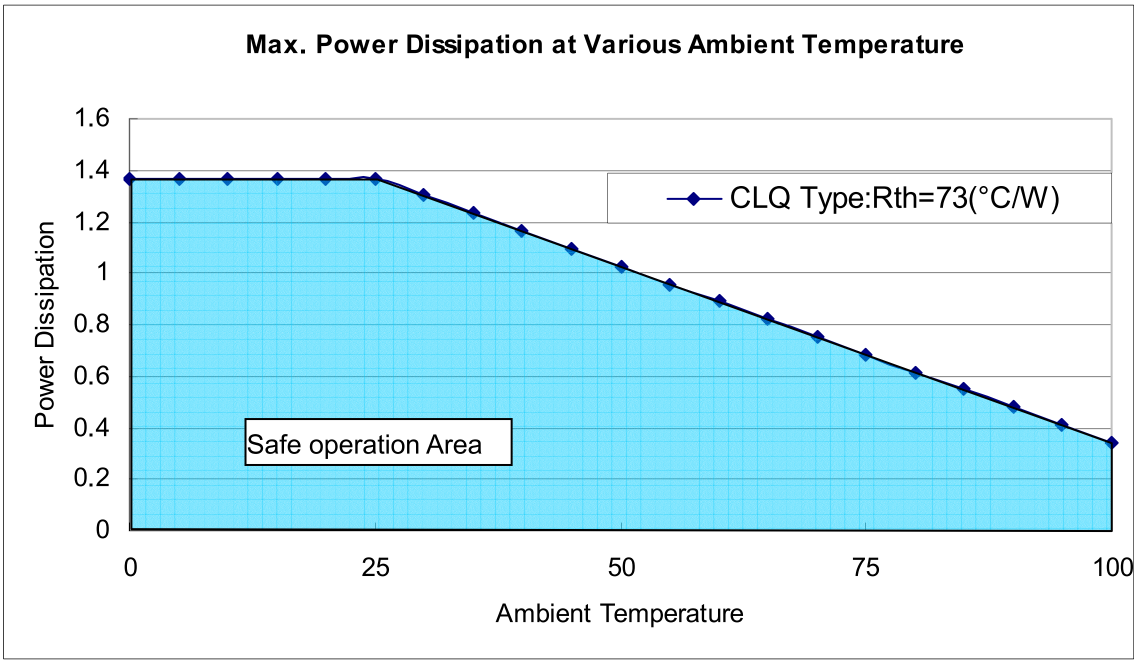
Macroblock has defines "Pb-Free & Green" to mean semiconductor products that are compatible with the current RoHS requirements and selected **100% pure tin** (Sn) to provide forward and backward compatibility with both the current industry-standard SnPb-based soldering processes and higher-temperature Pb-free processes. Pure tin is widely accepted by customers and suppliers of electronic devices in Europe, Asia and the US as the lead-free surface finish of choice to replace tin-lead. Also, it is backward compatible to standard 215ºC to 240ºC reflow processes which adopt tin/lead (SnPb) solder paste. However, in the whole Pb-free soldering processes and materials, 100% pure tin (Sn), will all require up to 260°C for proper soldering on boards, referring to J-STD-020B as shown below.



*Note1: For details, please refer to Macroblock's "Policy on Pb-free & Green Package".

Package Power Dissipation (P_D)

The maximum power dissipation, $P_D(max) = (Tj – Ta) / R_{th(j-a)}$, decreases as the ambient temperature increases.



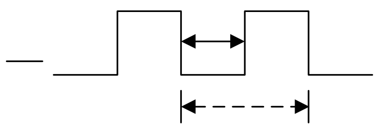
The maximum allowable package power dissipation is determined as $P_D(max) = (Tj – Ta) / R_{th(j-a)}$. When 24 output channels are turned on simultaneously, the actual package power dissipation is $P_D(act) = (I_{DD} \times V_{DD}) + (I_{OUT} \times Duty \times V_{DS} \times 24)$. Therefore, to keep $P_D(act) \le P_D(max)$, the allowable maximum output current as a function of duty cycle is:

$I_{OUT} = \{ [(Tj – Ta) / R_{th(j-a)}] – (I_{DD} \times V_{DD}) \} / V_{DS} / Duty / 24$,

where Tj = 150°C.

Duty= t_{ON} / T;

t_{ON}: the time of LEDs turning on; T: $\overline{OE}$ signal period

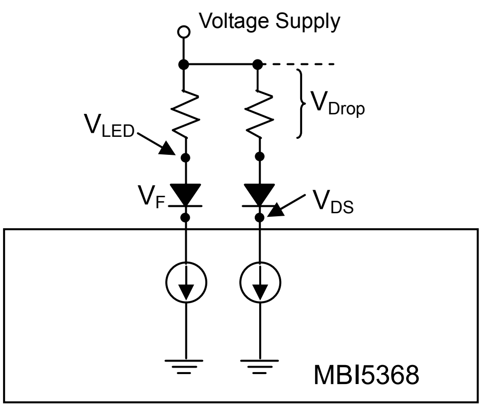


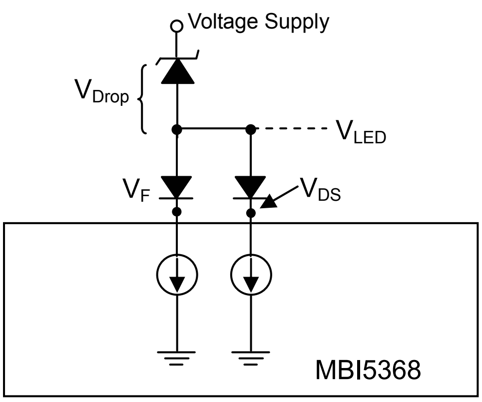
Load Supply Voltage (V_{LED})

Considering the package power dissipating limits, MBI5368 are designed to operate with V_{DS} ranging from 0.4V to 1.0V. V_{DS} may be so high as to make $P_{D(act)} > P_{D(max)}$ under higher V_{LED} , for instance, than 5V, where $V_{DS} = V_{LED} – V_F$ and V_{LED} is the load supply voltage. In this case, it is recommended to use the lowest possible supply voltage or to set an external voltage reducer, V_{DROP}.

A voltage reducer lets $V_{DS} = (V_{LED} – V_F) – V_{DROP}$.

Resistors or Zener diode can be used in the applications as shown in the following figures.

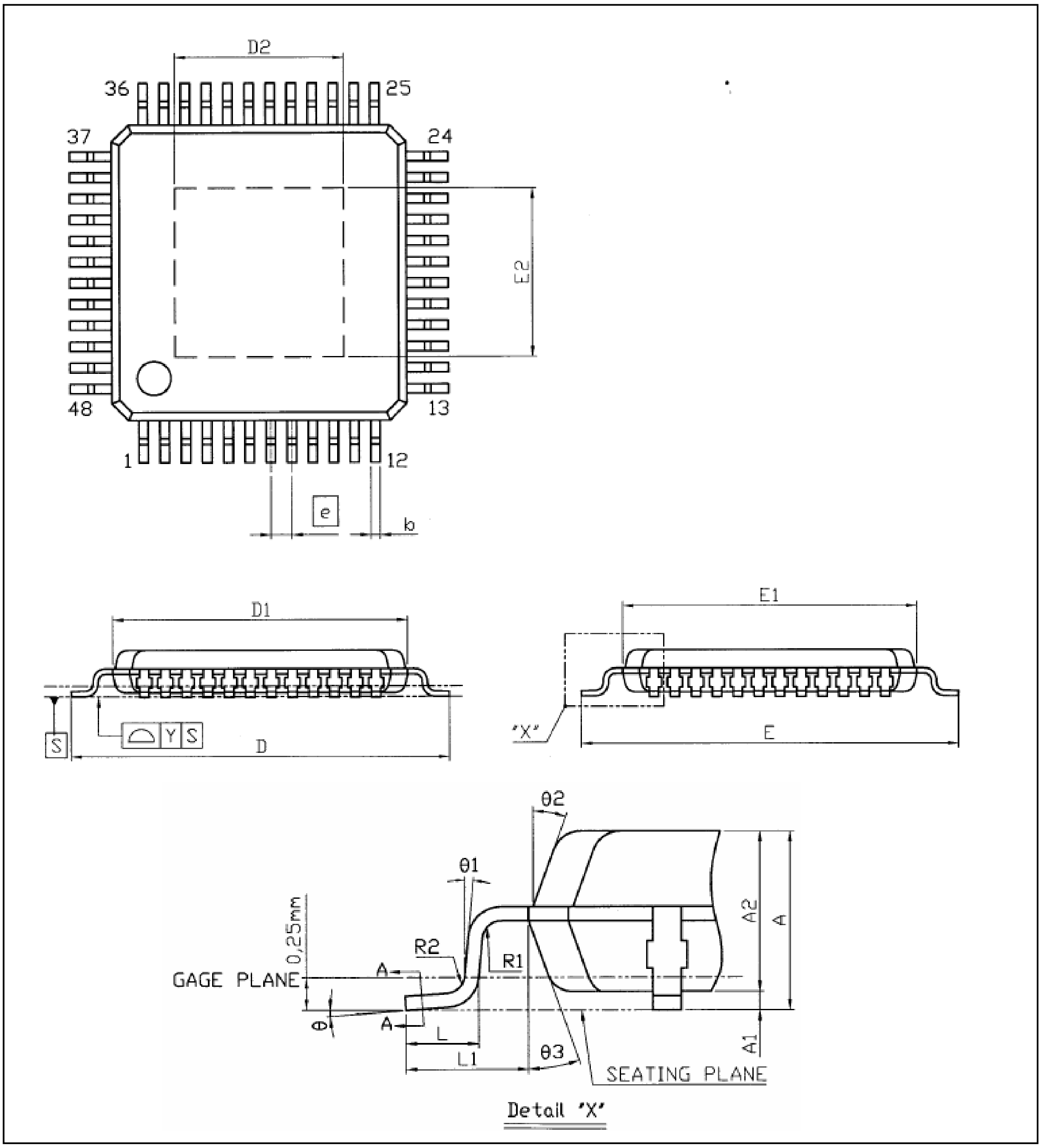




Switching Noise Reduction

LED Driver ICs are frequently used in switch-mode applications which always behave with switching noise due to the parasitic inductance on PCB. To eliminate switching noise, refer to “Application Note for 8-bit and 16-bit LED Drivers- Overshoot”.

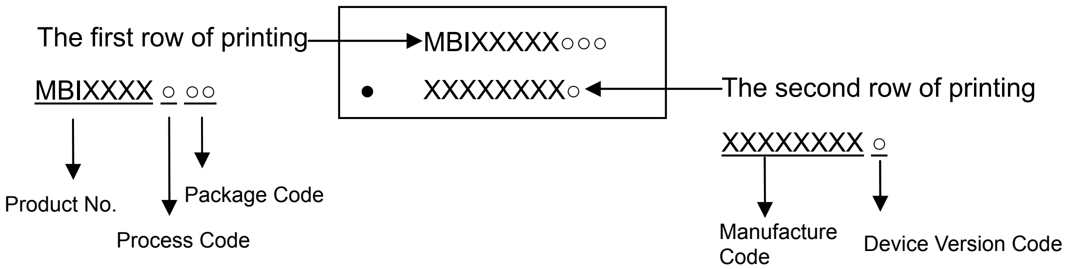
Package Outline



MBI5368 GLQ Outline Drawing

Symbol	Dimension (mm)			Dimension (MIL)		
	Min.	Normal	Max.	Min.	Normal	Max.
A			1.60			63
A1	0.05		0.15	2		6
A2	1.35	1.40	1.45	53	55	57
b	0.17	0.22	0.27	7	9	11
D		9.00 BSC			354 BSC	
D1		7.00 BSC			276 BSC	
D2	4	4.5	5	157	177	197
E		9.00 BSC			354 BSC	
E1		7.00 BSC			276 BSC	
E2	4	4.5	5	157	177	197
$\boxed{e}$		0.50 BSC			20 BSC	
L	0.45	0.60	0.75	18	24	30
L1		1.00 REF			39 REF	
R1	0.08			3		
R2	0.08		0.20	3		8
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°

Product Top-mark Information



Product Revision History

Datasheet version	Device version code
V1.00	*Not defined*
V1.02	A

Product Ordering Information

Part Number	"Pb-free & Green" Package Type	Weight (g)
MBI5368GLQ	LQFP48-7x7-0.5	0.268