STRUCTURE Silicon Monolithic Integrated Circuit

NAME OF PRODUCT DC-AC Inverter Control IC

TYPE **ＢＤ９２７５Ｆ**

FUNCTION

- Using 20V process / 1ch control with Push-Pull
- Accuracy of drive output frequency : 3.5% (IC Only/Built-in CT Capacitor)
- High accuracy timer latch current(±15%)
- Built-in FAIL function
- Adjustable latch timing
- Adjustable slow start time
- Lamp current and voltage sense feedback control
- Mode-selectable the operating or stand-by mode by STB pin (Typ.=0uA)

○Absolute Maximum Ratings (Ta = 25℃)

Parameter	Symbol	Limits	Unit
Supply Voltage	Vcc	20	V
OUTPUT PIN Voltage	N1, N2	20	V
Operating Temperature Range	Topr	-40～+85	℃
Storage Temperature Range	Tstg	-55～+150	℃
Maximum Junction Temperature	Tjmax	+150	℃
Power Dissipation	Pd	SOP18:562*	mW

*1Pd derate at -4.5mW/℃ for temperature above Ta = 25℃ (When mounted on a PCB 70.0mm×70.0mm×1.6mm)

○動作範囲

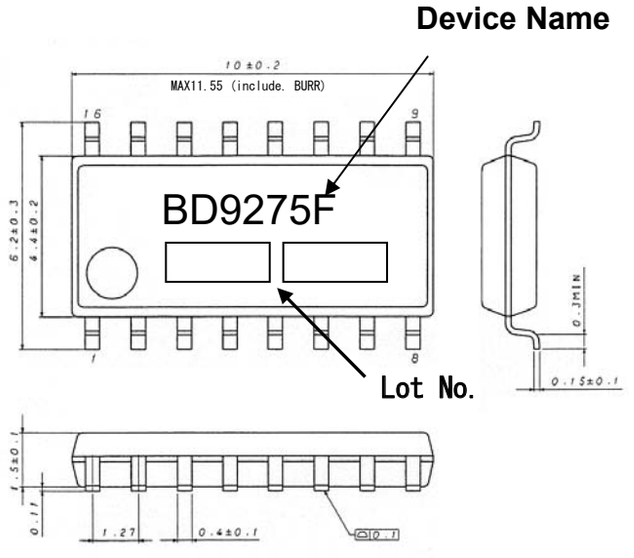
項目	記号	範囲	単位
Supply voltage	VCC	8.0 ～ 18.0	V
Input Frequency Ratio PWM_IN PIN	F_PWM_IN	0.060～0.5	kHz
DRIVER frequency	F_OUT	20 ～ 90	kHz

○Electric Characteristics (Ta=25℃、VCC=12V、STB=3.0V)

Item	SYMBOL	LIMIT MIN.	LIMIT TYP.	LIMIT MAX.	UNIT	CONDITION
((WHOLE DEVICE))						
Operating current	Icc1	—	2.0	4.0	mA	RT=100kΩ, FB=GND, IS=1.5V
Stand-by current	Icc2	—	0	20	μA	VSTB=0V
((STAND BY CONTROL))						
Stand-by voltage H	VSTBH	2	-	VCC	V	System ＯＮ
Stand-by voltage L	VSTBL	-0.3	-	0.8	V	System ＯＦＦ
STB PIN pull down resistor	RSTB	180	375	750	kΩ	VSTB=2V
((VCC UVLO BLOCK)))						
Operating voltage	VCC_UVLO	7.2	7.5	7.8	V	VCC=6V→8V sweep
Hesteresis width	⊿UVLO_HYS	0.3	0.5	0.7	V	VCC=8V→6V sweep
((OSC BLOCK))						
RT pin Voltage	VRT	1.300	1.500	1.700	V	RT=100kΩ
SRT ON resistance	RSRT	—	75	150	Ω	VSRT=0.1V
((PWM Dimming Block))						
PWM_IN PIN voltage H	VPWMIN_H	2.4	-	5	V	VPWM_IN=0V⇒3.0V
PWM_IN PIN voltage L	VPWMIN_L	-0.3	-	0.8	V	VPWM_IN=3.0V⇒0V
PWM_IN PIN pull down resistor	R_PWMIN	1000	2000	4000	kΩ	VPWM_I=5V
((FEED BACK BLOCK))						
IS threshold voltage	VIS	1.225	1.250	1.275	V	
VS threshold voltage	VVS	1.200	1.250	1.300	V	
IS source current	IIS	16	20	24	μA	IS=1.0V
IS COMP detect voltage	VISCOMP	0.565	0.625	0.685	V	IS=1.3V→0.5V
((SLOW START BLOCK))						
SS term END Voltage	VSS	2.400	2.500	2.600	V	VSS=0V⇒3V
Soft start current	ISS	1.7	2.0	2.3	μA	VSS=1.0V IS=1.5V
((COMP BLOCK))						
COMP over voltage detect voltage	VCOMPH	1.900	2.000	2.100	V	VSS＞2.5V VCOMP=1.5V→2.5V
Hysterisis width (COMP)	⊿VCOMPH	0.100	0.200	0.300	V	VSS＜2.0V VCOMP=2.5V→1.5V
COMP PIN pull down resistor	RCOMP	1000	2000	4000	kΩ	COMP=5V
FAIL ON resistance	RFAIL	—	75	150	Ω	VFAIL=0.1V
((OUTPUT BLOCK))						
N1,N2 PIN output sink resistance	RsinkN	1.5	3.0	6.0	Ω	IIN=100mA
N1,N2 PIN output source resistance	RsourceN	4.5	9	18	Ω	IIN=-100mA
MAX DUTY	MAX DUTY	45	47.0	49.5	%	FOUT=50kHz
Drive output frequency	FOUT	48.25	50	51.75	kHz	RT=100kΩ
((TIMER BLOCK))						
Timer Latch setting voltage	VCP	2.900	3.000	3.100	V	VCP=0V⇒3.2V
Timer Latch setting current	ICP	1.7	2.0	2.3	μA	CP=1.0V IS=1.5V COMP=3.0V

(This product is not designed to be radiation-resistant.)

○Package Dimensions



SOP-16 (Unit:mm)

○PIN No. ・PIN NAME・FUNCTION

BD9275F					
No.	**PIN**	**Function**	**No.**	**PIN**	**Function**
1	VCC	Supply voltage input	16	N1	NMOS FET driver
2	STB	Stand-by switch	15	N2	NMOS FET driver
3	SRT	External resistor from SRT to RT for adjusting the triangle oscillator	14	PGND	Ground for FET drivers
4	RT	External resistor from SRT to RT for adjusting the triangle oscillator	13	PWM_IN	Dimming pulse signal input pin
5	GND	GROUND	12	SS	External capacitor from SS to GND for Soft Start Control
6	FB	Error amplifier output	11	CP	External capacitor from CP to GND for Timer Latch
7	IS	Error amplifier input	10	FAIL	Error signal output pin
8	VS	Error amplifier input	9	COMP	Over voltage detect pin

○NOTE FOR USE

1. This product is produced with strict quality control, but might be destroyed if used beyond its absolute maximum ratings. Once IC is destroyed, failure mode will be difficult to determine, like short mode or open mode. Therefore, physical protection countermeasure, like fuse is recommended in case operating conditions go beyond the expected absolute maximum ratings.
2. The circuit functionality is guaranteed within of ambient temperature operation range as long as it is within recommended operating range. The standard electrical characteristic values cannot be guaranteed at other voltages in the operating ranges, however the variation will be small.
3. Mounting failures, such as misdirection or miscounts, may harm the device.
4. A strong electromagnetic field may cause the IC to malfunction.
5. The GND pin should be the location within ±0.3V compared with the PGND pin. ALL voltage should be under VCC voltage +0.3V
6. BD9275F incorporate a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation of the thermal shutdown circuit is assumed.
7. When modifying the external circuit components, make sure to leave an adequate margin for external components actual value and tolerance as well as dispersion of the IC.
8. About the external FET, the parasitic Capacitor may cause the gate voltage to change, when the drain voltage is switching. Make sure to leave adequate margin for this IC variation.
9. Under operating CP charge (under error mode) analog dimming and burst dimming are not operate.
10. Under operating Slow Start Control (SS is less than 2.5V), It does not operate Timer Latch.
11. By STB voltage is changed to 2 states. Therefore, do not input STB pin voltage between one state and the other state (0.8～2.0V).
12. The pin connected a connector need to connect to the resistor for electrical surge destruction.
13. This IC is a monolithic IC which (as shown is Fig-1) has P+ substrate and between the various pins. A P-N junction is formed from this P layer of each pin. For example, the relation between each potential is as follows,

    ○(When GND > PinB and GND > PinA, the P-N junction operates as a parasitic diode.)

    ○(When PinB > GND > PinA, the P-N junction operates as a parasitic transistor.)

    Parasitic diodes can occur inevitably in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits as well as operation faults and physical damage. Accordingly you must not use methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin.

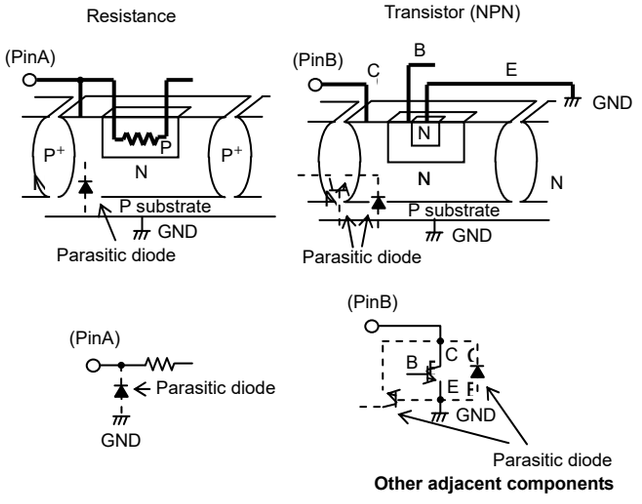


Fig-1 Simplified structure of a Bipolar IC