**TEXAS INSTRUMENTS**

# TPS7A8101-Q1 Low-Noise, Wide-Bandwidth, High PSRR, Low-Dropout 1-A Linear Regulator

## 1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C4B
- Low-Dropout 1-A Regulator with Enable
- Adjustable Output Voltage: 0.8 V to 6 V
- Wide-Bandwidth High PSRR:
  - 80 dB at 1 kHz
  - 60 dB at 100 kHz
  - 54 dB at 1 MHz
- Low Noise: 23.5 $\mu V_{RMS}$ typical (100 Hz to 100 kHz)
- Stable With 4.7-µF Output Capacitance
- Excellent Load and Line Transient Response
- 3% Overall Accuracy (Over Load, Line, Temperature)
- Over-Current and Overtemperature Protection
- Very Low Dropout: 170 mV Typical at 1 A
- Package: 3-mm × 3-mm SON-8

## 2 Applications

- RF Power in Automotive Applications
- Automotive ADAS ECUs
- Telematic Control Units
- Audio
- High-Speed I/F (PLL and VCO)

## 3 Description

The TPS7A8101-Q1 low-dropout linear regulator (LDO) offers very good performance in output noise and power-supply rejection ratio (PSRR). This LDO uses an advanced BiCMOS process and a PMOSFET pass device to achieve very low noise, excellent transient response, and excellent PSRR performance.

The TPS7A8101-Q1 device is stable with a 4.7-µF ceramic output capacitor and uses a precision voltage reference and feedback loop to achieve a worst-case accuracy of 3% over all load, line, process, and temperature variations.
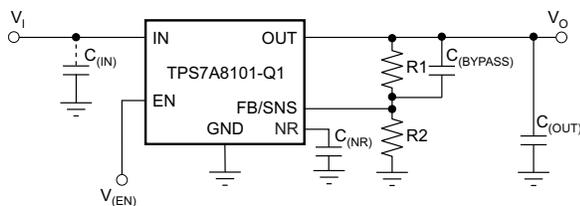
This device is fully specified over the temperature range of $T_A$ = –40°C to 125°C and is offered in a 3-mm × 3-mm, SON-8 package with a thermal pad.

### Device Information[(1)]

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPS7A8101-Q1 | SON (8) | 3.00 mm × 3.00 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

## 4 Typical Application Circuit
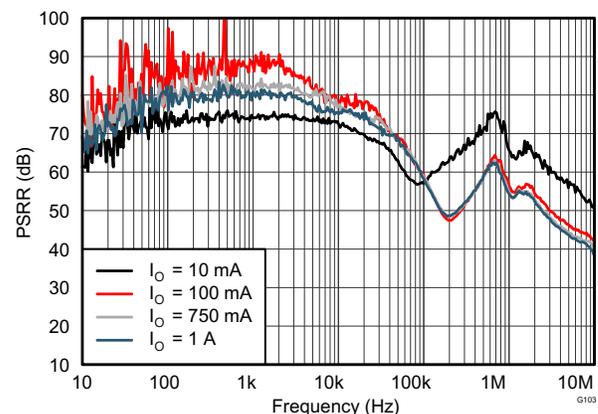




**Typical Power-Supply Ripple Rejection**

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## 5 Revision History

**Changes from Original (April 2014) to Revision A**                                                                      **Page**

# 6 Pin Configuration and Functions

**8-Pin SON
DRB Package
(Top View)**

```
OUT   1        8   IN
OUT   2        7   IN
FB/SNS 3       6   NR
GND   4        5   EN
```
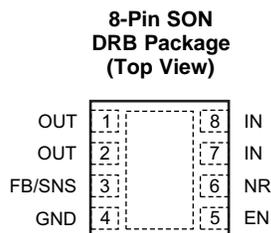
## Pin Functions

| PIN | | DESCRIPTION |
|---|---|---|
| **NAME** | **NO.** | |
| EN | 5 | Driving this pin high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. See to the *Shutdown* section for more details. The EN pin must not be left floating and can be connected to the IN pin if not used. |
| FB/SNS | 3 | This pin is the input to the error amplifier and is used to set the output voltage of the device. |
| GND | 4 | Ground |
| IN | 7 | Unregulated input supply |
| | 8 | |
| NR | 6 | Connect an external capacitor between this pin and ground to reduce output noise to very low levels. The capacitor also slows down the $V_O$ ramp (RC soft start). |
| OUT | 1 | Regulator output. A 4.7-µF or larger ceramic capacitor is required for stability. |
| | 2 | |
| Thermal Pad | — | The Thermal Pad should be connected to GND. |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).[1]

|         |          | MIN  | MAX | UNIT |
|---------|----------|------|-----|------|
| Voltage | IN       | −0.3 | 7   | V    |
|         | FB/SNS, NR | −0.3 | 3.6 | V    |
|         | EN       | −0.3 | $V_I$ + 0.3[2] | V    |
|         | OUT      | −0.3 | 7   | V    |
| Current | OUT      | Internally Limited | | A |
| Operating junction temperature, $T_J$ | | −55 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.

(2) $V_{(EN)}$ absolute maximum rating is $V_I$ + 0.3 V or + 7 V, whichever is smaller.

## 7.2 Handling Ratings

|           |                       |                                                                      |                          | MIN  | MAX | UNIT |
|-----------|-----------------------|----------------------------------------------------------------------|--------------------------|------|-----|------|
| $T_{stg}$ | Storage temperature range | | | −55 | 150 | °C |
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002, classification level H2[1] | | −2 | 2 | kV |
|           |                       | Charged device model (CDM), per JEDEC specification JESD22-C101, classification level C4B | Corner pins (1, 4, 5, and 8) | −750 | 750 | V |
|           |                       |                                                                      | Other pins | −500 | 500 |  |

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 Specification.

## 7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

|       |                            | MIN  | MAX | UNIT |
|-------|----------------------------|------|-----|------|
| $V_I$ | Input voltage              | 2.2  | 6.5 | V    |
| $I_O$ | Output current             | 0    | 1   | A    |
| $T_A$ | Operating free air temperature | −40 | 125 | °C   |

## 7.4 Thermal Information

| THERMAL METRIC[1] | | DRB (8 PINS) | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 45.7 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 53.1 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 21.2 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.9 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 21.4 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 5.2 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953A.

## 7.5 Electrical Characteristics

Over the temperature range of –40°C ≤ $T_A$, $T_J$ ≤ 125°C, $V_I$ = $V_{Onom}$ + 0.5 V or 2.2 V (whichever is greater), $I_O$ = 1 mA, $V_{(EN)}$ = 2.2 V, $C_{(OUT)}$ = 4.7 µF, $C_{(NR)}$ = 0.01 µF, and $C_{(BYPASS)}$ = 0 µF, unless otherwise noted. The device is tested at $V_O$ = 0.8 V and $V_O$ = 6 V. Typical values are at $T_J$ = 25°C.

| | PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_I$ | Input voltage range[1] | | | 2.2 | | 6.5 | V |
| $V_{(NR)}$ | Internal reference | | | 0.79 | 0.8 | 0.81 | V |
| $V_O$ | Output voltage range | | | 0.8 | | 6 | V |
| | Output accuracy[2] | $V_O$ + 0.5 V ≤ $V_I$ ≤ 6 V, $V_I$ ≥ 2.5 V, 100 mA ≤ $I_O$ ≤ 500 mA, 0°C ≤ $T_J$ ≤ 85°C | | –2% | | 2% | |
| | | $V_O$ + 0.5 V ≤ $V_I$ ≤ 6.5 V, $V_I$ ≥ 2.2 V, 100 mA ≤ $I_O$ ≤ 1 A | | –3% | ±0.3% | 3% | |
| $\Delta V_{O(\Delta VI)}$ | Line regulation | $V_{Onom}$ + 0.5 V ≤ $V_I$ ≤ 6.5 V, $V_I$ ≥ 2.2 V, $I_O$ = 100 mA | | | 150 | | µV/V |
| $\Delta V_{O(\Delta IL)}$ | Load regulation | 100 mA ≤ $I_O$ ≤ 1 A | | | 2 | | µV/mA |
| $V_{DO}$ | Dropout voltage[3] | $V_O$ + 0.5 V ≤ $V_I$ ≤ 6.5 V, $V_I$ ≥ 2.2 V, $I_O$ = 500 mA, $V_{(FB/SNS)}$ = GND | | | | 250 | mV |
| | | $V_O$ + 0.5 V ≤ $V_I$ ≤ 6.5 V, $V_I$ ≥ 2.5 V, $I_O$ = 750 mA, $V_{(FB/SNS)}$ = GND | | | | 350 | mV |
| | | $V_O$ + 0.5 V ≤ $V_I$ ≤ 6.5 V, $V_I$ ≥ 2.5 V, $I_O$ = 1 A, $V_{(FB/SNS)}$ = GND | | | | 500 | mV |
| $I_L$ | Output current-limit | $V_O$ = 0.85 × $V_{Onom}$, $V_I$ ≥ 3.3 V | | 1100 | 1400 | 2000 | mA |
| $I_{(GND)}$ | Ground pin current | $I_O$ = 1 mA | | | 60 | 100 | µA |
| | | $I_O$ = 1 A | | | | 350 | µA |
| $I_{L(sd)}$ | Shutdown current ($I_{(GND)}$) | $V_{(EN)}$ ≤ 0.4 V, $V_I$ ≥ 2.2 V, $R_L$ = 1 kΩ, 0°C ≤ $T_J$ ≤ 125°C | | | 0.2 | 2.5 | µA |
| $I_{(FB/SNS)}$ | Feedback pin current | $V_I$ = 6.5 V, $V_{(FB/SNS)}$ = 0.8 V | | | 0.02 | 1 | µA |
| PSRR | Power-supply rejection ratio | $V_I$ = 4.3 V, $V_O$ = 3.3 V, $I_O$ = 750 mA | $f$ = 100 Hz | | 80 | | dB |
| | | | $f$ = 1 kHz | | 82 | | dB |
| | | | $f$ = 10 kHz | | 78 | | dB |
| | | | $f$ = 100 kHz | | 60 | | dB |
| | | | $f$ = 1 MHz | | 54 | | dB |
| $V_n$ | Output noise voltage | BW = 100 Hz to 100 kHz, $V_I$ = 3.8 V, $V_O$ = 3.3 V, $I_O$ = 100 mA, $C_{(NR)}$ = $C_{(BYPASS)}$ = 470 nF | | | 23.5 | | µV$_{RMS}$ |
| $V_{(EN)H}$ | Enable high (enabled) | 2.2 V ≤ $V_I$ ≤ 3.6 V, $R_L$ = 1 kΩ | | 1.2 | | | V |
| | | 3.6 V < $V_I$ ≤ 6.5 V, $R_L$ = 1 kΩ | | 1.35 | | | V |
| $V_{(EN)L}$ | Enable low (shutdown) | $R_L$ = 1 kΩ | | 0 | | 0.4 | V |
| $I_{(EN)}$ | Enable pin current, enabled | $V_I$ = $V_{(EN)}$ = 6.5 V | | | 0.02 | 1 | µA |
| $t_{st}$ | Startup time | $V_{Onom}$ = 3.3 V, $V_O$ = 0% to 90% $V_{Onom}$, R1 = 3.3 kΩ, $C_{(OUT)}$ = 10 µF, $C_{(NR)}$ = 470 nF | | | 80 | | ms |
| UVLO | Undervoltage lockout | $V_I$ rising, $R_L$ = 1 kΩ | | 1.86 | 2 | 2.1 | V |
| | Hysteresis | $V_I$ falling, $R_L$ = 1 kΩ | | | 75 | | mV |
| $T_{sd}$ | Thermal shutdown temperature | Shutdown, temperature increasing | | | 160 | | °C |
| | | Reset, temperature decreasing | | | 140 | | °C |

(1) Minimum $V_I$ = $V_O$ + $V_{DO}$ or 2.2 V, whichever is greater.
(2) The TPS7A8101-Q1 does not include external resistor tolerances and it is not tested at this condition: $V_O$ = 0.8 V, 4.5 V ≤ $V_I$ ≤ 6.5 V, and 750 mA ≤ $I_O$ ≤ 1 A because the power dissipation is greater than the maximum rating of the package.
(3) $V_{DO}$ is not measured for fixed output voltage devices with $V_O$ < 1.7 V because minimum $V_I$ = 2.2 V.

## 7.6 Typical Characteristics

At $V_{Onom}$ = 3.3 V, $V_I$ = $V_{Onom}$ + 0.5 V or 2.2 V (whichever is greater), $I_O$ = 100 mA, $V_{(EN)}$ = $V_I$, $C_{(IN)}$ = 1 µF, $C_{(OUT)}$ = 4.7 µF, and $C_{(NR)}$ = 0.01 µF; all temperature values refer to $T_J$, unless otherwise noted.



NOTE: The Y-axis shows 1% $V_O$ per division
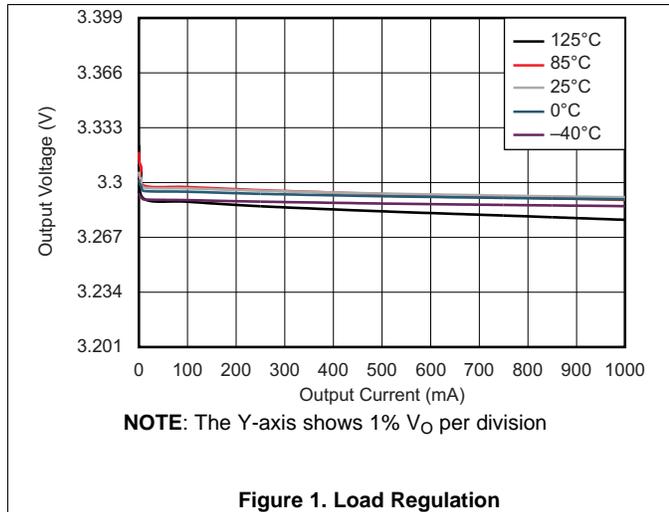
**Figure 1. Load Regulation**



NOTE: The Y-axis shows 1% $V_O$ per division
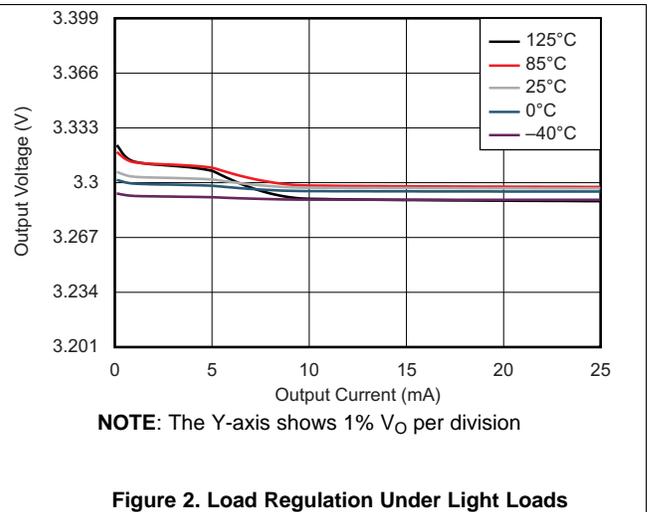
**Figure 2. Load Regulation Under Light Loads**



$V_O$ = 0.8 V          $I_O$ = 750 mA

NOTE: The Y-axis shows 1% $V_O$ per division
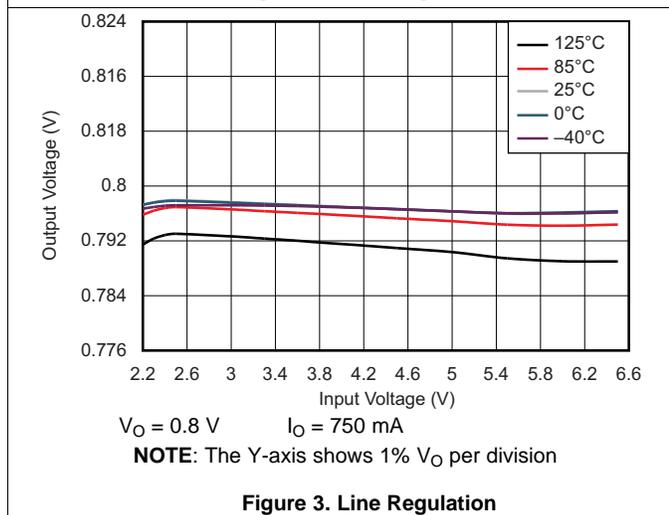
**Figure 3. Line Regulation**



$V_O$ = 0.8 V          $I_O$ = 5 mA

NOTE: The Y-axis shows 1% $V_O$ per division
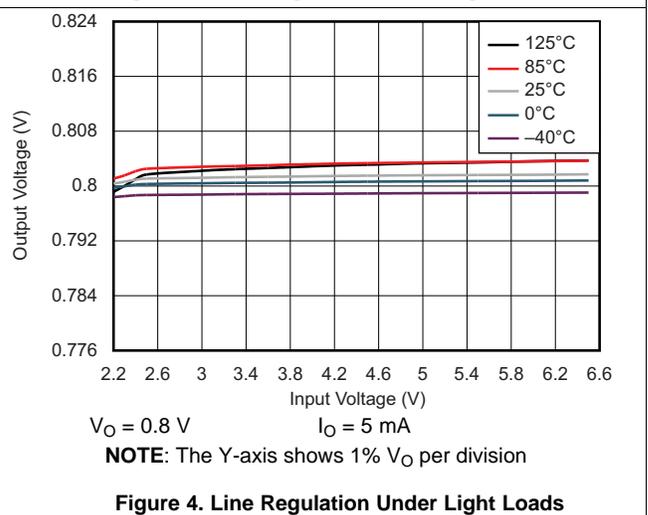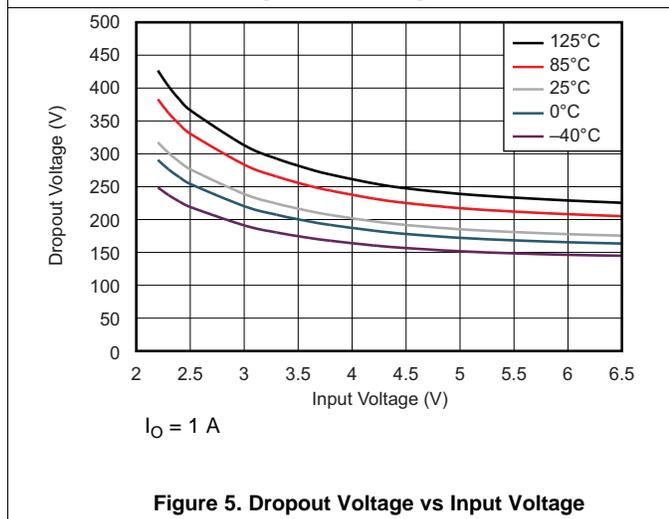
**Figure 4. Line Regulation Under Light Loads**



$I_O$ = 1 A

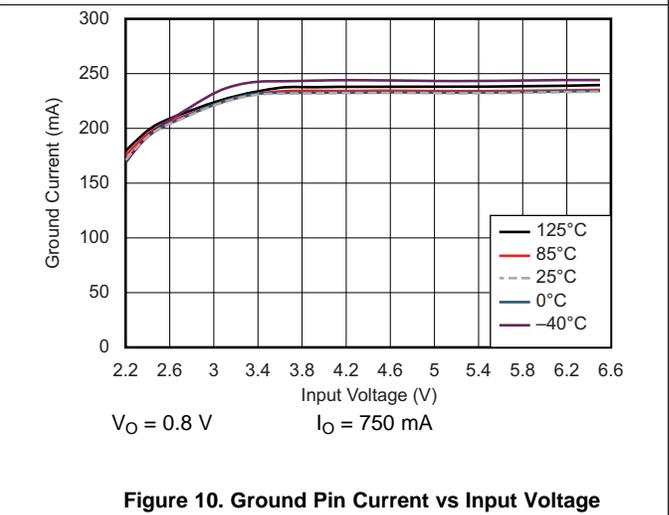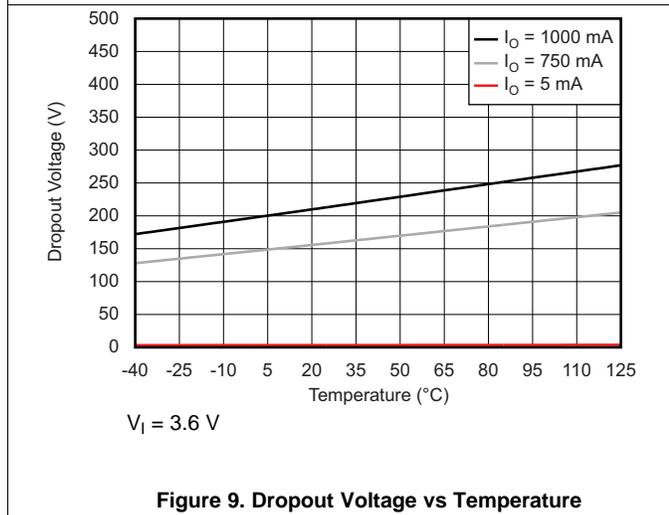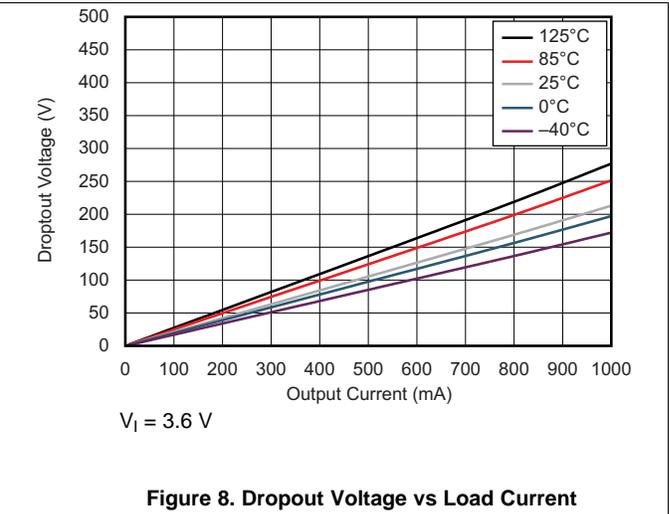**Figure 5. Dropout Voltage vs Input Voltage**



$I_O$ = 750 mA
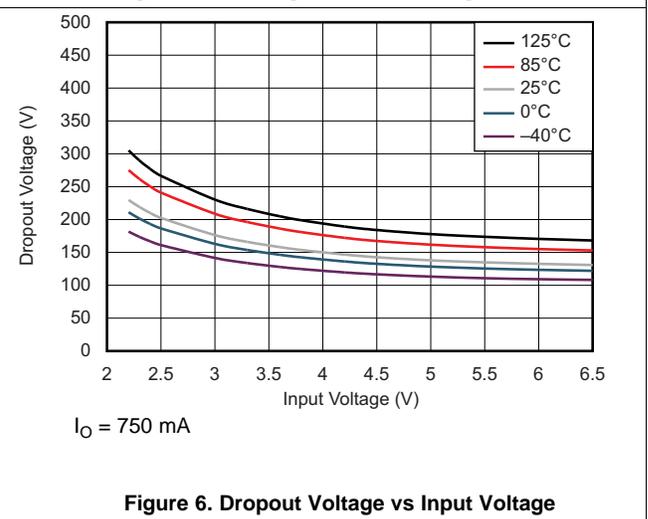
**Figure 6. Dropout Voltage vs Input Voltage**

## Typical Characteristics (continued)

At $V_{Onom}$ = 3.3 V, $V_I$ = $V_{Onom}$ + 0.5 V or 2.2 V (whichever is greater), $I_O$ = 100 mA, $V_{(EN)}$ = $V_I$, $C_{(IN)}$ = 1 µF, $C_{(OUT)}$ = 4.7 µF, and $C_{(NR)}$ = 0.01 µF; all temperature values refer to $T_J$, unless otherwise noted.



$I_O$ = 500 mA

**Figure 7. Dropout Voltage vs Input Voltage**



$V_I$ = 3.6 V

**Figure 8. Dropout Voltage vs Load Current**



$V_I$ = 3.6 V

**Figure 9. Dropout Voltage vs Temperature**



$V_O$ = 0.8 V          $I_O$ = 750 mA

**Figure 10. Ground Pin Current vs Input Voltage**



**Figure 11. Ground Pin Current vs Load Current**



$V_{(EN)}$ = 0.4 V

**Figure 12. Shutdown Current vs Temperature**

## Typical Characteristics (continued)

At $V_{Onom}$ = 3.3 V, $V_I$ = $V_{Onom}$ + 0.5 V or 2.2 V (whichever is greater), $I_O$ = 100 mA, $V_{(EN)}$ = $V_I$, $C_{(IN)}$ = 1 µF, $C_{(OUT)}$ = 4.7 µF, and $C_{(NR)}$ = 0.01 µF; all temperature values refer to $T_J$, unless otherwise noted.



$V_O = V_I – 0.5$ V
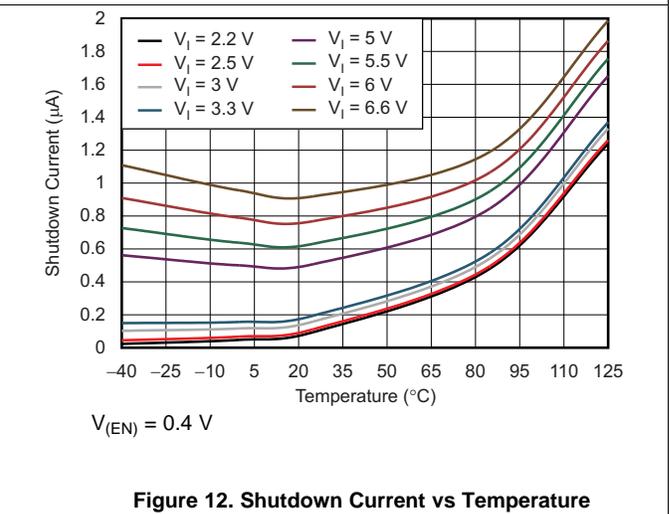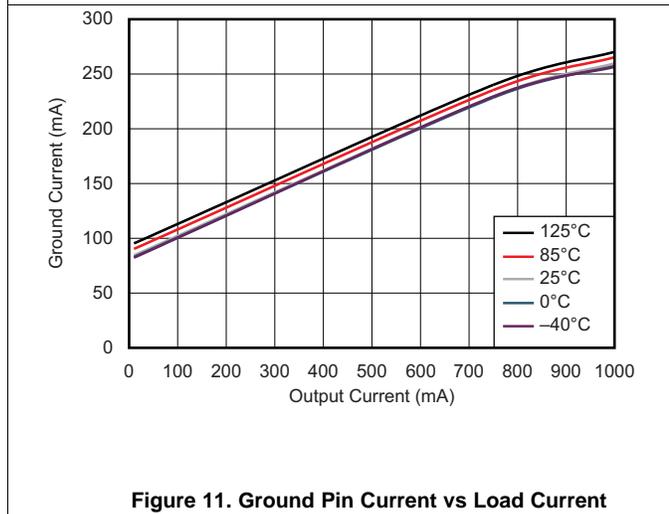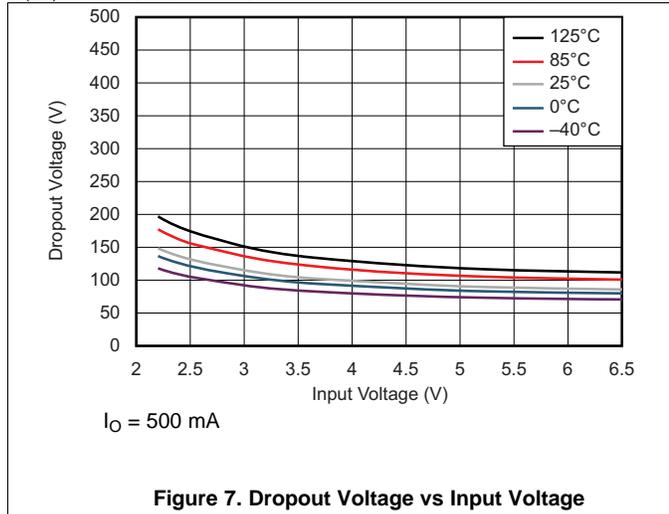
**Figure 13. Current-Limit vs Temperature**



$C_{(NR)} = C_{(BYPASS)}$ = 470 nF    $C_{(OUT)}$ = 10 µF    $C_{(IN)}$ = 0 F
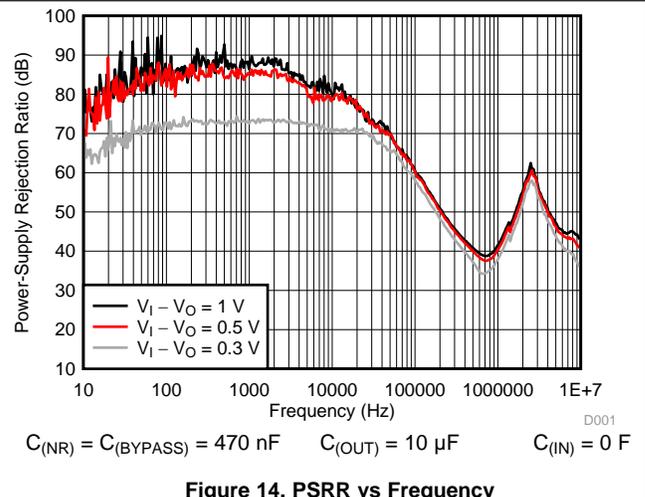
**Figure 14. PSRR vs Frequency**



$V_I – V_O = 1$ V    $C_{(IN)}$ = 0 F    $C_{(OUT)}$ = 10 µF
$C_{(NR)} = C_{(BYPASS)}$ = 470 nF
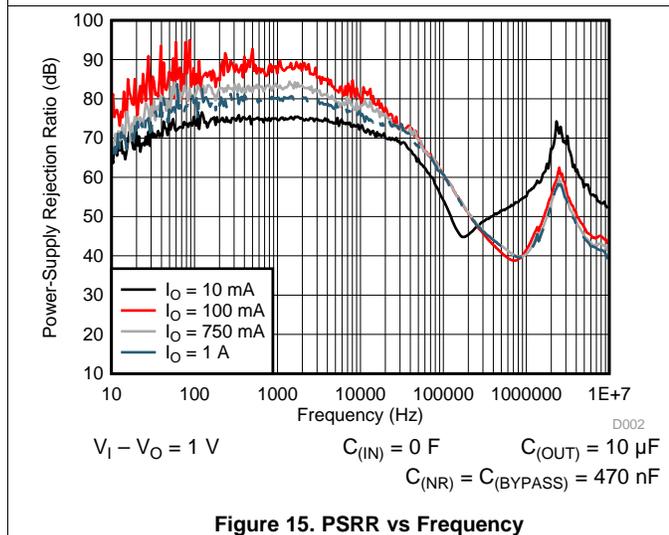
**Figure 15. PSRR vs Frequency**



$V_I – V_O = 0.5$ V    $C_{(IN)}$ = 0 F    $C_{(OUT)}$ = 10 µF
$C_{(NR)} = C_{(BYPASS)}$ = 470 nF
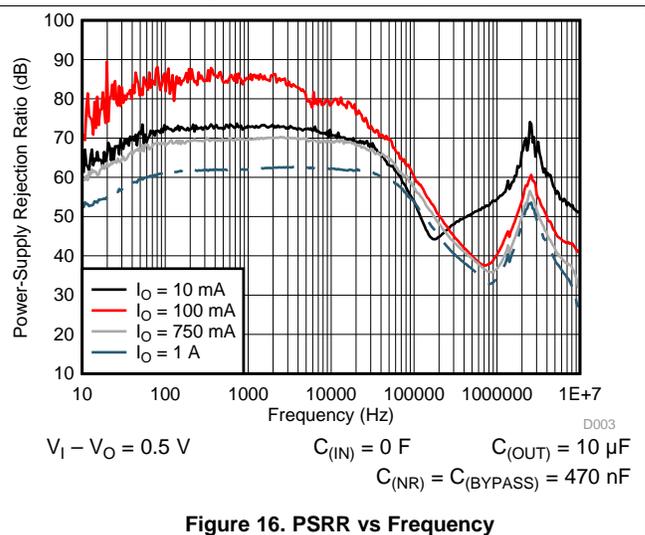
**Figure 16. PSRR vs Frequency**



$V_I – V_O = 1$ V    $C_{(IN)}$ = 0 F    $C_{(OUT)}$ = 10 µF
$C_{(NR)} = C_{(BYPASS)}$ = 470 nF
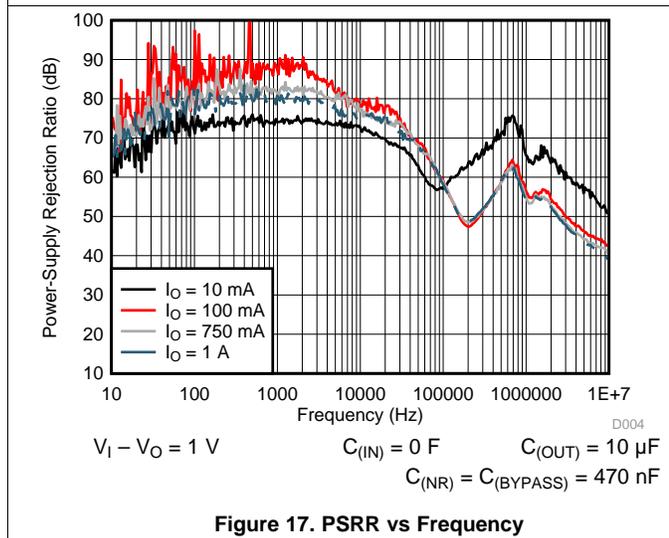
**Figure 17. PSRR vs Frequency**



$V_I – V_O = 0.5$ V    $C_{(IN)}$ = 0 F    $C_{(OUT)}$ = 10 µF
$C_{(NR)} = C_{(BYPASS)}$ = 470 nF

**Figure 18. PSRR vs Frequency**

## Typical Characteristics (continued)

At $V_{Onom}$ = 3.3 V, $V_I$ = $V_{Onom}$ + 0.5 V or 2.2 V (whichever is greater), $I_O$ = 100 mA, $V_{(EN)}$ = $V_I$, $C_{(IN)}$ = 1 µF, $C_{(OUT)}$ = 4.7 µF, and $C_{(NR)}$ = 0.01 µF; all temperature values refer to $T_J$, unless otherwise noted.

$I_O$ = 100 mA        $C_{(IN)}$ = 0 F
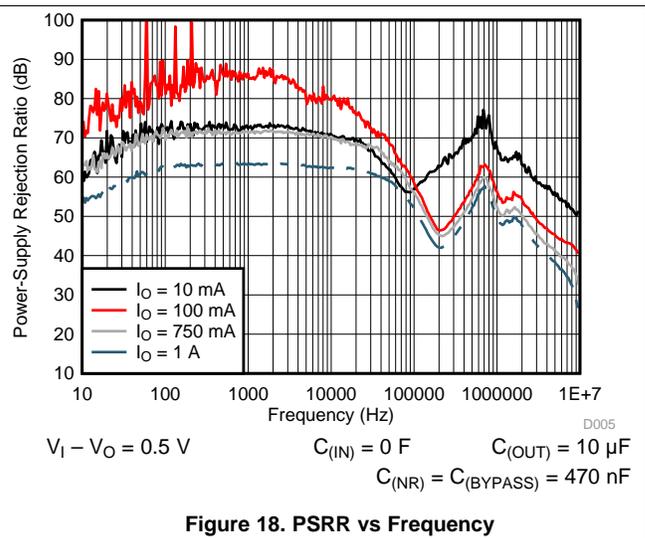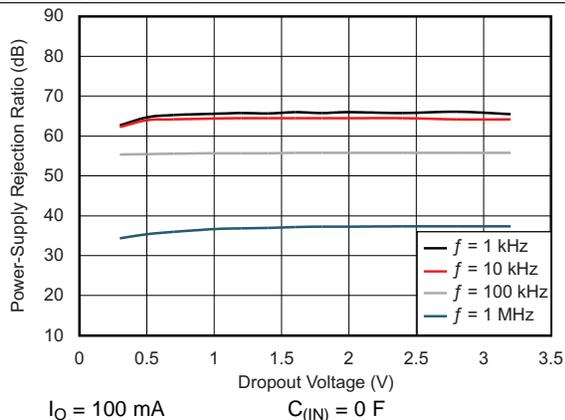
**Figure 19. PSRR vs Dropout Voltage**

$I_O$ = 750 mA        $C_{(IN)}$ = 0 F
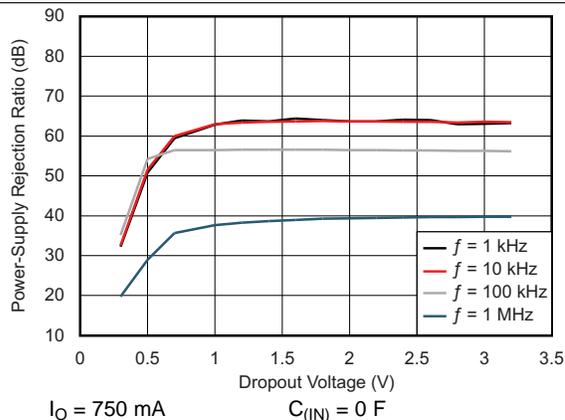
**Figure 20. PSRR vs Dropout Voltage**

$V_I – V_O$ = 0.5 V        $C_{(OUT)}$ = 10 µF        $C_{(IN)}$ = 10 µF
24.09 µV$_{RMS}$ ($C_{(NR)}$ = $C_{(BYPASS)}$ = 100 nF)
23.54 µV$_{RMS}$ ($C_{(NR)}$ = $C_{(BYPASS)}$ = 470 nF)
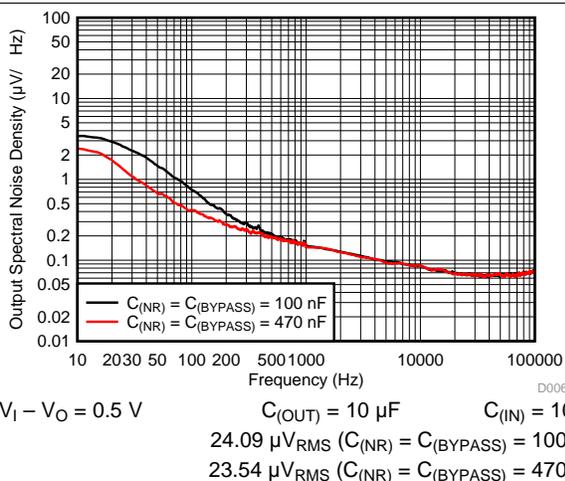
**Figure 21. Output Spectral Noise Density vs Frequency
(RMS noise (100 Hz to 100 kHz))**

25.89 µV$_{RMS}$ ($V_O$ = 1.8 V)        $C_{(IN)}$ = 10 µF        $V_I – V_O$ = 0.5 V
23.54 µV$_{RMS}$ ($V_O$ = 2.5 V)        $C_{(NR)}$ = 470 nF        $C_{(OUT)}$ = 10 µF
23.54 µV$_{RMS}$ ($V_O$ = 3.3 V)        $C_{(BYPASS)}$ = 470 nF
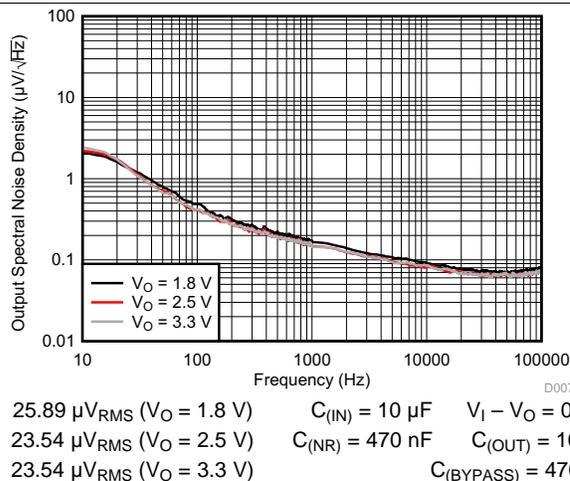
**Figure 22. Output Spectral Noise Density vs Frequency
(RMS noise (100 Hz to 100 kHz))**

23.54 µV$_{RMS}$ ($I_O$ = 100 mA)        $C_{(IN)}$ = 10 µF        $V_I – V_O$ = 0.5 V
23.71 µV$_{RMS}$ ($I_O$ = 750 mA)        $C_{(NR)}$ = 470 nF        $C_{(OUT)}$ = 10 µF
22.78 µV$_{RMS}$ ($I_O$ = 1 A)        $C_{(BYPASS)}$ = 470 nF

**Figure 23. Output Spectral Noise Density vs Frequency
(RMS noise (100 Hz to 100 kHz))**

23.54 µV$_{RMS}$ ($C_O$ = 10 µF)        $C_{(IN)}$ = 10 µF        $V_I – V_O$ = 0.5 V
23.91 µV$_{RMS}$ ($C_O$ = 22 µF)        $C_{(NR)}$ = 470 nF        $C_{(OUT)}$ = 10 µF
22.78 µV$_{RMS}$ ($C_O$ = 100 µF)        $C_{(BYPASS)}$ = 470 nF
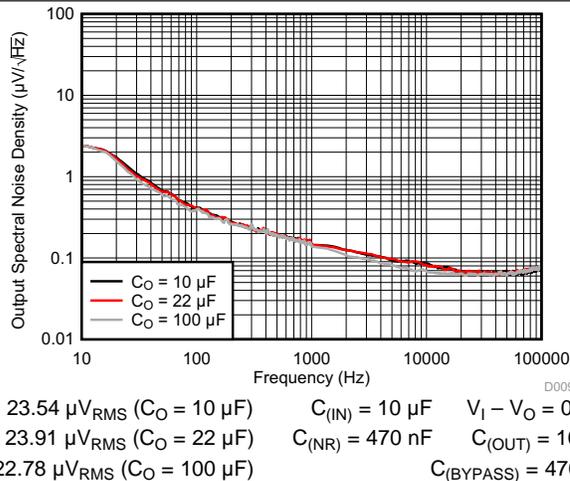
**Figure 24. Output Spectral Noise Density vs Frequency
(RMS noise (100 Hz to 100 kHz))**

## Typical Characteristics (continued)

At $V_{Onom}$ = 3.3 V, $V_I$ = $V_{Onom}$ + 0.5 V or 2.2 V (whichever is greater), $I_O$ = 100 mA, $V_{(EN)}$ = $V_I$, $C_{(IN)}$ = 1 µF, $C_{(OUT)}$ = 4.7 µF, and $C_{(NR)}$ = 0.01 µF; all temperature values refer to $T_J$, unless otherwise noted.
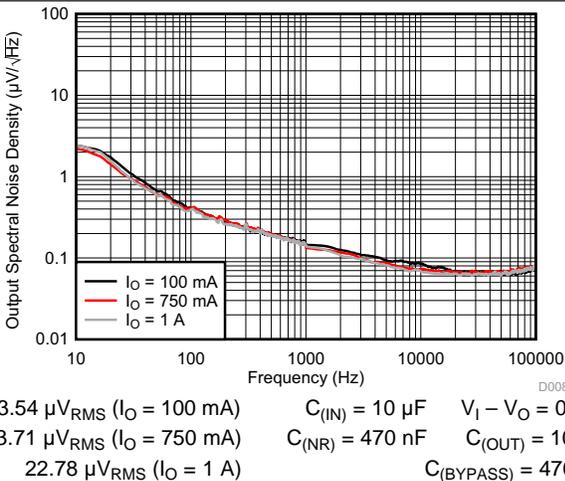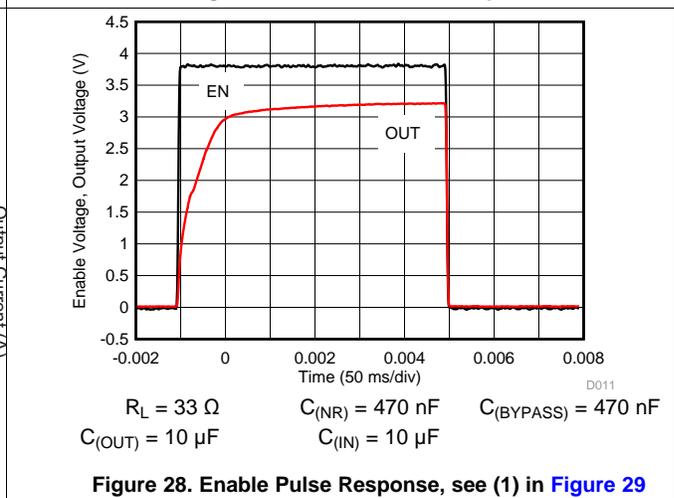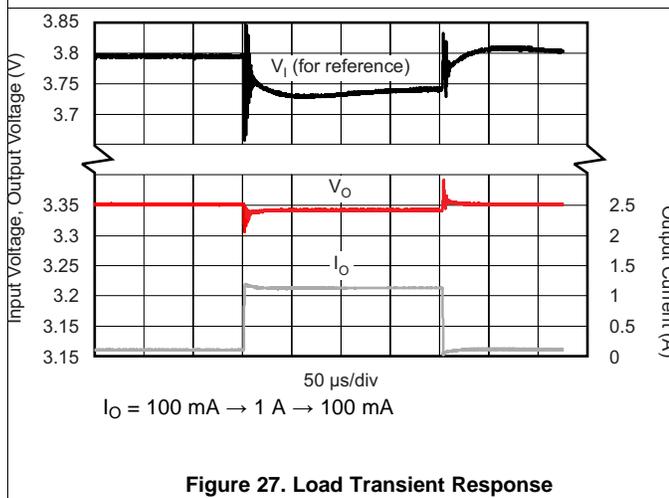


Using the same value of $C_{(NR)}$ and $C_{(BYPASS)}$ in the X-Axis

**Figure 25. Startup Time vs Noise Reduction Capacitance**



$V_I$ = 3.8 V → 4.8 V → 3.8 V

$I_O$ = 500 mA

**Figure 26. Line Transient Response**



$I_O$ = 100 mA → 1 A → 100 mA

**Figure 27. Load Transient Response**



| $R_L$ = 33 Ω | $C_{(NR)}$ = 470 nF | $C_{(BYPASS)}$ = 470 nF |
| $C_{(OUT)}$ = 10 µF | $C_{(IN)}$ = 10 µF | |

**Figure 28. Enable Pulse Response, see (1) in Figure 29**



| $R_L$ = 33 Ω | $C_{(NR)}$ = 470 nF | $C_{(BYPASS)}$ = 470 nF |
| $C_{(OUT)}$ = 10 µF | $C_{(IN)}$ = 10 µF | |

(1) The internal reference requires approximately 80 ms of rampup time (see Startup) from the enable event; therefore, $V_O$ fully reaches the target output voltage of 3.3 V in 80 ms from startup.

**Figure 29. Power-Up and Power-Down Response**

Product Folder Links: *TPS7A8101-Q1*

# 8 Detailed Description

## 8.1 Overview

The TPS7A8101-Q1 device belongs to a family of new-generation LDO regulators that use innovative circuitry to achieve wide bandwidth and high loop gain, resulting in extremely high PSRR (over a 1-MHz range) even with very low headroom ($V_I – V_O$). A noise-reduction capacitor ($C_{(NR)}$) at the NR pin and a bypass capacitor ($C_{(BYPASS)}$) decrease noise generated by the bandgap reference in order to improve PSRR, while a quick-start circuit fast-charges the noise-reduction capacitor. This family of regulators offers sub-bandgap output voltages, current-limit, and thermal protection, and is fully specified from –40°C to 125°C.
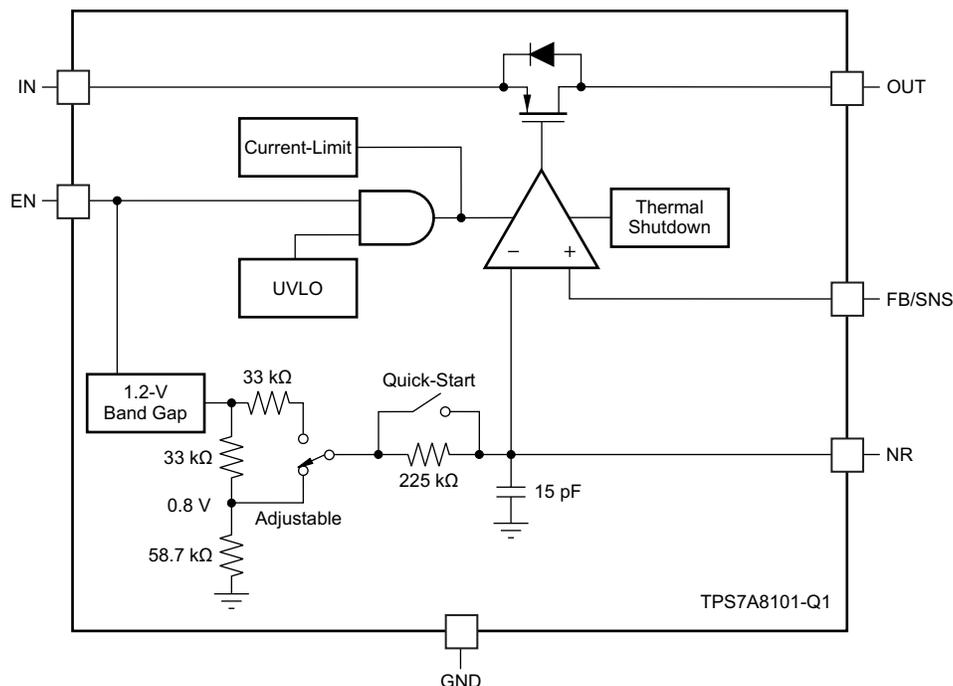
## 8.2 Functional Block Diagram



**Figure 30. Functional Block Diagram**

## 8.3 Feature Description

### 8.3.1 Internal Current-Limit

The TPS7A8101-Q1 internal current-limit helps protect the regulator during fault conditions. During the current-limit, the output sources a fixed amount of current that is largely independent of the output voltage. For reliable operation, the device should not be operated in a current-limit state for extended periods of time.

The PMOS pass element in the TPS7A8101-Q1 device has a built-in body diode that conducts current when the voltage at the OUT pin ($V_{(OUT)}$) exceeds the voltage at the IN pin ($V_{(IN)}$). This current is not limited, so if extended reverse-voltage operation is anticipated, external limiting may be appropriate.

### 8.3.2 Shutdown

The enable pin (EN) is active high and is compatible with standard-voltage and low-voltage TTL-CMOS levels. When shutdown capability is not required, the EN pin can connect to the IN pin.

## Feature Description (continued)

### 8.3.3 Startup

Through a lower resistance, the bandgap reference can quickly charge the noise-reduction capacitor ($C_{(NR)}$). The TPS7A8101-Q1 device has a *quick-start* circuit to quickly charge $C_{(NR)}$, if present; see Figure 30. At startup, this quick-start switch is closed, with only 33 kΩ of resistance between the bandgap reference and the NR pin. The quick-start switch opens approximately 100 ms after any device-enabling event, and the resistance between the bandgap reference and the NR pin becomes higher in value (approximately 250 kΩ) to form a very-good low-pass (RC) filter. This low-pass filter reduces the noise present on the reference voltage; therefore, reducing the noise on the output.

Inrush current can cause problems in many applications. The 33-kΩ resistance during the startup period is intentionally placed between the bandgap reference and the NR pin in order to slow down the reference voltage rampup, thus reducing the inrush current.

Use Equation 1 to calculate the startup time with other $C_{(NR)}$ values. For example, the capacitance of connecting the recommended $C_{(NR)}$ value of 0.47 µF along with the 33-kΩ resistance causes an 80-ms RC delay (approximately).

$$t_{st} \text{ (s)} = 170000 \times C_{(NR)} \text{ (F)} \tag{1}$$

Although the noise-reduction effect is nearly saturated at 0.47 µF, connecting a $C_{(NR)}$ value greater than 0.47 µF can additionally help reduce noise. However, when connecting a $C_{(NR)}$ value greater than 0.47 µF, the startup time is extremely long because the quick-start switch opens after approximately 100 ms. That is, if $C_{(NR)}$ is not fully charged during this 100-ms period, $C_{(NR)}$ finishes charging through a higher resistance of 250 kΩ, and takes much longer to fully charge.

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**NOTE**

A low-leakage capacitor should be used for $C_{(NR)}$. Most ceramic capacitors are suitable

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### 8.3.4 Undervoltage Lockout (UVLO)

The TPS7A8101-Q1 device uses an undervoltage-lockout (UVLO) circuit to ensure that the output is shut off until the internal circuitry has enough voltage to operate properly. The UVLO circuit has a deglitch feature so that the circuit typically ignores undershoot transients on the input if the duration is less than 50-µs.

## 8.4 Device Functional Modes

Driving the EN pin over 1.2 V for $V_I$ between 2.2 V to 3.6 V or 1.35 V for $V_I$ between 3.6 V and 6.5 V turns on the regulator. Driving the EN pin below 0.4 V causes the regulator to enter shutdown mode.

In shutdown, the current consumption of the device is reduced to 0.02 µA typically.

Product Folder Links: *TPS7A8101-Q1*

# 9 Application and Implementation

## 9.1 Application Information

The TPS7A8101-Q1 device belongs to a family of new-generation LDO regulators that use innovative circuitry to achieve wide bandwidth and high loop gain, resulting in extremely high PSRR (over a 1-MHz range) even with very low headroom ($V_I – V_O$). A noise-reduction capacitor ($C_{(NR)}$) at the NR pin and a bypass capacitor ($C_{(BYPASS)}$) decrease noise generated by the bandgap reference in order to improve PSRR, while a quick-start circuit fast-charges the noise-reduction capacitor. This family of regulators offers sub-bandgap output voltages, current-limit, and thermal protection, and is fully specified from –40°C to 125°C.

## 9.2 Typical Application

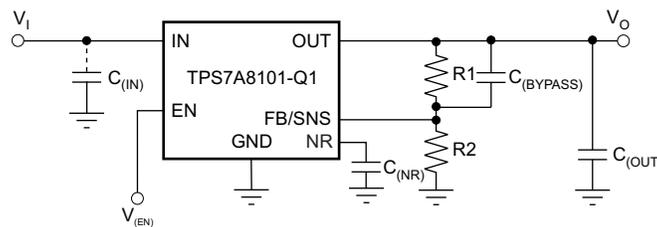Figure 31 shows the connections for the device.



**Figure 31. Typical Application Circuit**

The voltage on the FB pin sets the output voltage and is determined by the values of the resistors R1 and R2. Use Equation 2 to calculate the values of R1 and R2 any voltage.

$$V_O = \frac{(R1+R2)}{R2} \times 0.8$$

(2)

Table 1 lists sample resistor values for common output voltages. In Table 1, E96 series resistors are used, and all values meet 1% of the target $V_O$, assuming resistors with zero error. For the actual design, pay attention to any resistor error-factors. Using lower values for R1 and R2 reduces the noise injected into the FB pin.

### 9.2.1 Design Requirements

#### 9.2.1.1 Dropout Voltage

The TPS7A8101-Q1 device uses a PMOS pass transistor to achieve low dropout. When ($V_I – V_{Onom}$) is less than the dropout voltage ($V_{DO}$), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $r_{DS(on)}$ of the PMOS pass element. $V_{DO}$ is proportional to the output current because the PMOS device in dropout functions in the same way as a resistor.

As with any linear regulator, PSRR and transient responses are degraded as ($V_I – V_O$) approaches dropout. Figure 19 and Figure 20 in the *Typical Characteristics* section shown this effect.

#### 9.2.1.2 Minimum Load

The TPS7A8101-Q1 device is stable and functions well with no output load. Traditional PMOS-LDO regulators suffer from lower loop gain at very light output loads. The TPS7A8101-Q1 device employs an innovative low-current mode circuit to increase loop gain under very light or no-load conditions, resulting in improved output voltage regulation performance down to zero output current.

#### 9.2.1.3 Input And Output Capacitor Requirements

Although an input capacitor is not required for stability, connecting a 0.1-µF to 1-µF low-equivalent series-resistance (ESR) capacitor from the input supply near the regulator to ground is good analog-design practice. This capacitor counteracts reactive input sources and improves transient response and ripple rejection. A higher-value capacitor may be necessary if large, fast load transients are anticipated or if the device is located several inches from the power source. If source impedance is not sufficiently low, a 0.1-µF input capacitor may be necessary to ensure stability.

## Typical Application (continued)

The TPS7A8101-Q1 device is designed to be stable with standard ceramic capacitors of capacitance values 4.7 µF or larger. This device was evaluated using a 10-µF ceramic capacitor of 10-V rating, 10% tolerance, X5R type, and 0805 size (2 mm × 1,25 mm).

X5R-type and X7R-type capacitors are highly recommended because they have minimal variation in capacitance and ESR over temperature. The maximum ESR should be less than 1 Ω.

**Table 1. Recommended Feedback Resistor Values for Common Output Voltages**

| $V_O$ | R1 | R2 |
|---|---|---|
| 0.8 V | 0 Ω (Short) | 10 kΩ |
| 1 V | 2.49 kΩ | 10 kΩ |
| 1.2 V | 4.99 kΩ | 10 kΩ |
| 1.5 V | 8.87 kΩ | 10 kΩ |
| 1.8 V | 12.5 kΩ | 10 kΩ |
| 2.5 V | 21 kΩ | 10 kΩ |
| 3.3 V | 30.9 kΩ | 10 kΩ |
| 5 V | 52.3 kΩ | 10 kΩ |

**Table 2. Recommended Capacitor Values**

| NAME | DESCRIPTION | VALUE |
|---|---|---|
| $C_{(NR)}$ | Noise-reduction capacitor between the NR and GND pins | 470 nF |
| $C_{(BYPASS)}$ | Noise-reduction capacitor across R1 | 470 nF |
| $C_{(OUTPUT)}$ | Output capacitor | 10 µF |
| $C_{(IN)}$ | Input capacitor | 10 µF |

### 9.2.1.4 Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude but increases the duration of the transient response. Using a larger noise-reduction capacitor ($C_{(NR)}$), bypass capacitor ($C_{(BYPASS)}$), or both types of capacitors can improve line-transient performance.

### 9.2.2 Detailed Design Procedure

### 9.2.2.1 Output Noise

In most LDOs, the bandgap is the dominant noise source. If a noise reduction capacitor ($C_{(NR)}$) is used with the TPS7A8101-Q1 device, the bandgap does not contribute significantly to noise. Instead, noise is dominated by the output resistor-divider and the error-amplifier input. If a bypass capacitor ($C_{(BYPASS)}$) across the high-side feedback resistor (R1) is used with the TPS7A8101-Q1 device, noise from these other sources can also be significantly reduced.

To maximize noise performance in a given application, use a 0.47-µF noise-reduction capacitor plus a 0.47-µF bypass capacitor.
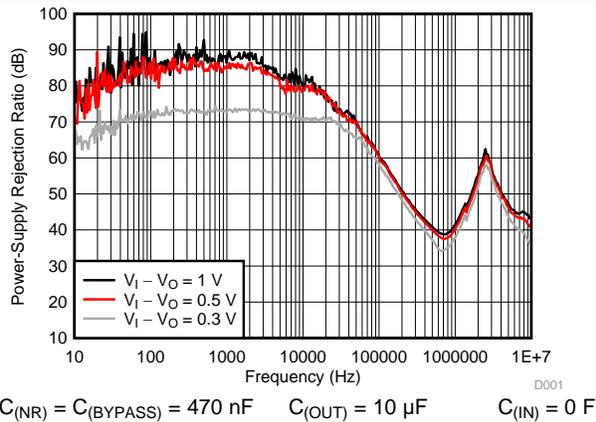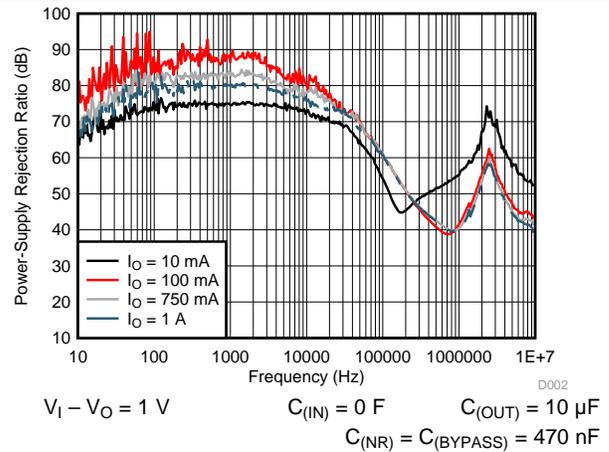
### 9.2.3 Application Curves



$C_{(NR)} = C_{(BYPASS)} = 470$ nF        $C_{(OUT)} = 10$ μF        $C_{(IN)} = 0$ F

**Figure 32. PSRR vs Frequency**



$V_I − V_O = 1$ V        $C_{(IN)} = 0$ F        $C_{(OUT)} = 10$ μF

$C_{(NR)} = C_{(BYPASS)} = 470$ nF

**Figure 33. PSRR vs Frequency**



$V_I − V_O = 0.5$ V        $C_{(IN)} = 0$ F        $C_{(OUT)} = 10$ μF

$C_{(NR)} = C_{(BYPASS)} = 470$ nF
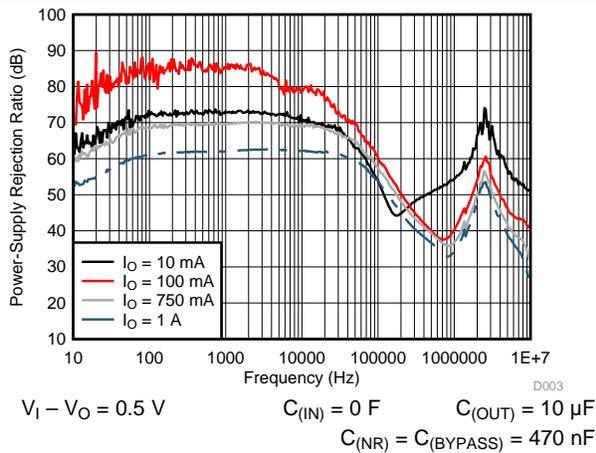
**Figure 34. PSRR vs Frequency**



$V_I − V_O = 0.5$ V        $C_{(OUT)} = 10$ μF        $C_{(IN)} = 10$ μF

24.09 μV$_{RMS}$ ($C_{(NR)} = C_{(BYPASS)} = 100$ nF)

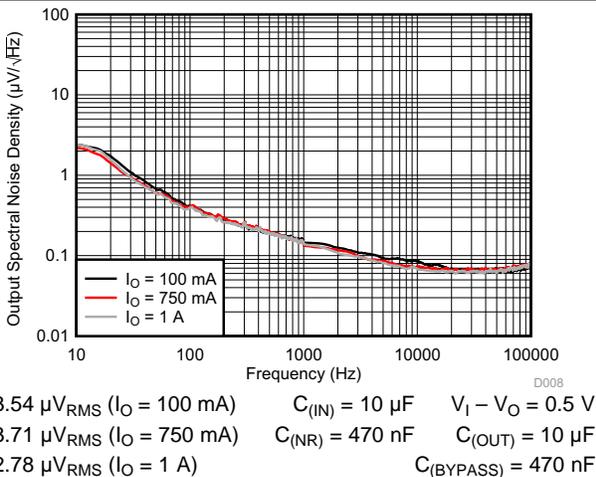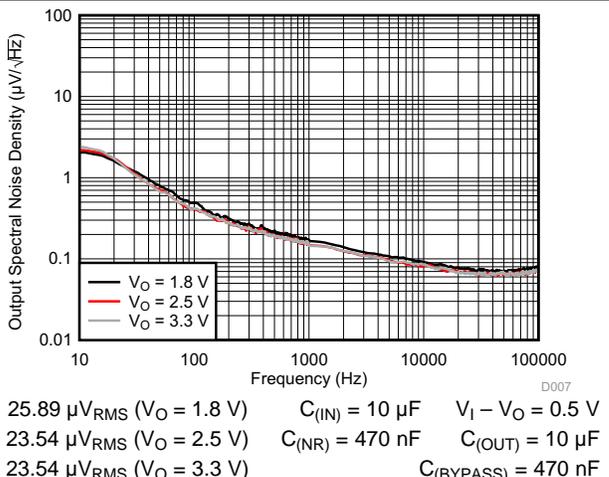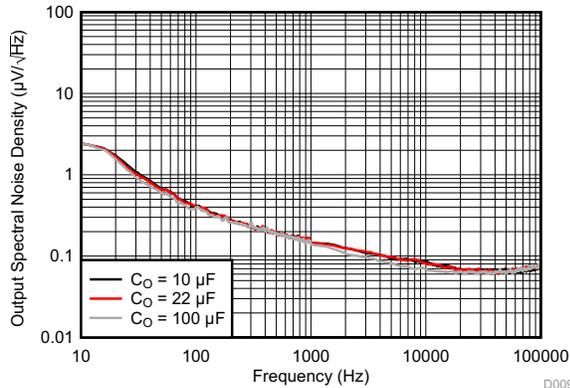23.54 μV$_{RMS}$ ($C_{(NR)} = C_{(BYPASS)} = 470$ nF)
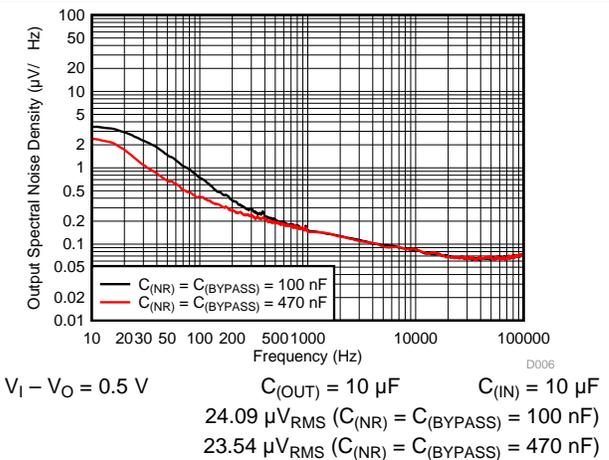
**Figure 35. Output Spectral Noise Density vs Frequency**
**(RMS noise (100 Hz to 100 kHz))**



23.54 μV$_{RMS}$ ($I_O = 100$ mA)        $C_{(IN)} = 10$ μF        $V_I − V_O = 0.5$ V

23.71 μV$_{RMS}$ ($I_O = 750$ mA)        $C_{(NR)} = 470$ nF        $C_{(OUT)} = 10$ μF

22.78 μV$_{RMS}$ ($I_O = 1$ A)        $C_{(BYPASS)} = 470$ nF

**Figure 36. Output Spectral Noise Density vs Frequency**
**(RMS noise (100 Hz to 100 kHz))**



25.89 μV$_{RMS}$ ($V_O = 1.8$ V)        $C_{(IN)} = 10$ μF        $V_I − V_O = 0.5$ V

23.54 μV$_{RMS}$ ($V_O = 2.5$ V)        $C_{(NR)} = 470$ nF        $C_{(OUT)} = 10$ μF

23.54 μV$_{RMS}$ ($V_O = 3.3$ V)        $C_{(BYPASS)} = 470$ nF

**Figure 37. Output Spectral Noise Density vs Frequency**
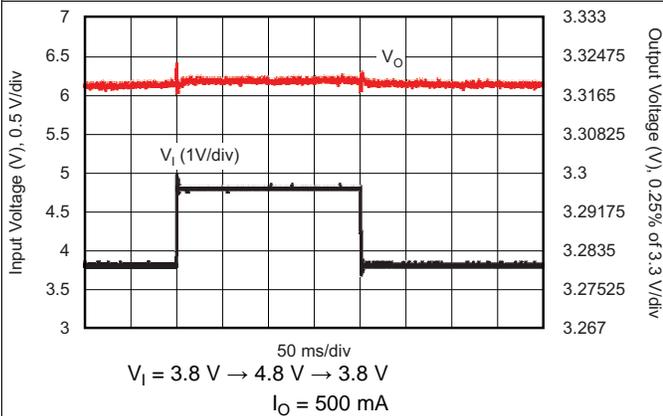**(RMS noise (100 Hz to 100 kHz))**

23.54 μV$_{RMS}$ (C$_O$ = 10 μF)         C$_{(IN)}$ = 10 μF         V$_I$ – V$_O$ = 0.5 V
23.91 μV$_{RMS}$ (C$_O$ = 22 μF)         C$_{(NR)}$ = 470 nF         C$_{(OUT)}$ = 10 μF
22.78 μV$_{RMS}$ (C$_O$ = 100 μF)                                              C$_{(BYPASS)}$ = 470 nF

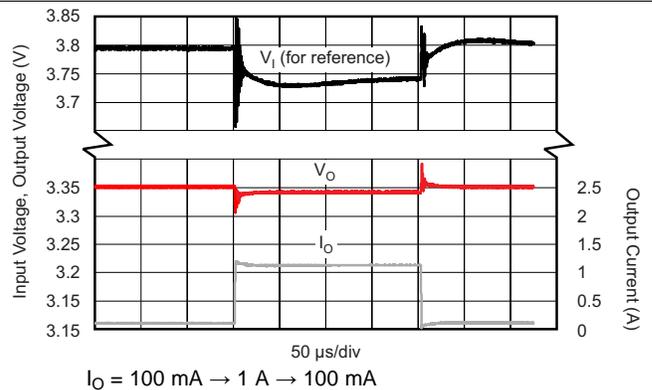**Figure 38. Output Spectral Noise Density vs Frequency (RMS noise (100 Hz to 100 kHz))**
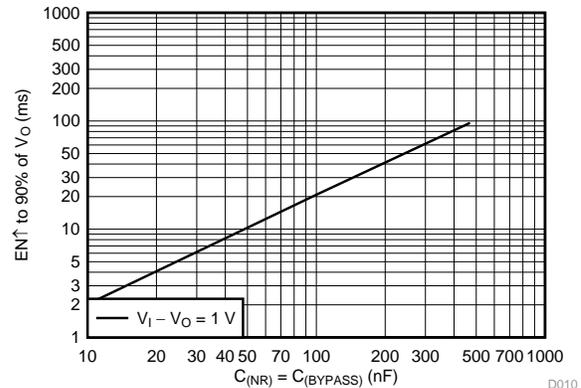


Using the same value of C$_{(NR)}$ and C$_{(BYPASS)}$ in the X-Axis
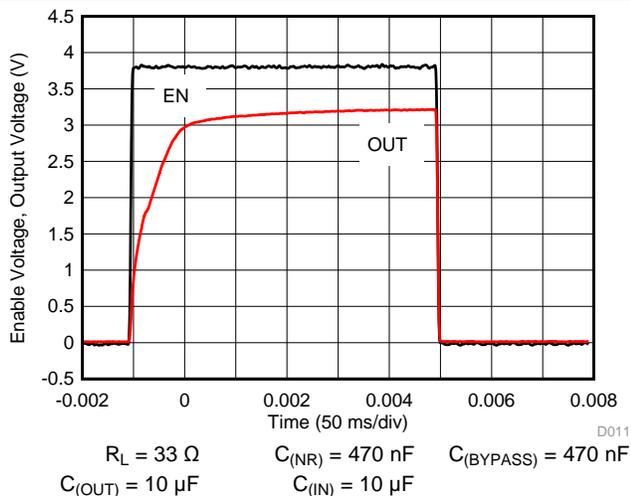
**Figure 39. Startup Time vs Noise Reduction Capacitance**



V$_I$ = 3.8 V → 4.8 V → 3.8 V
I$_O$ = 500 mA

**Figure 40. Line Transient Response**



I$_O$ = 100 mA → 1 A → 100 mA

**Figure 41. Load Transient Response**



R$_L$ = 33 Ω         C$_{(NR)}$ = 470 nF         C$_{(BYPASS)}$ = 470 nF
C$_{(OUT)}$ = 10 μF         C$_{(IN)}$ = 10 μF

**Figure 42. Enable Pulse Response, See (1) in Figure 43**
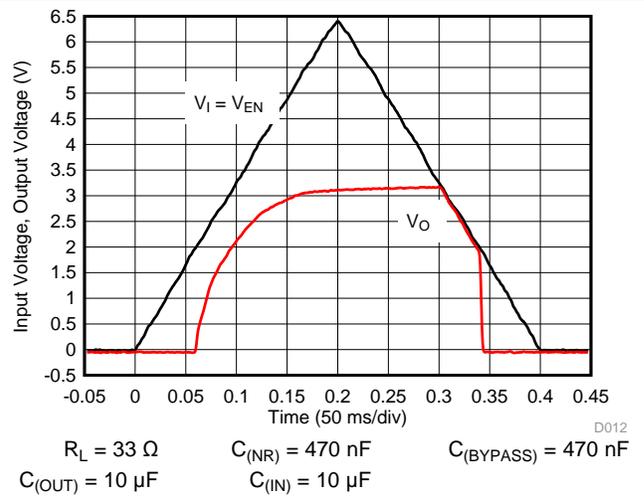


R$_L$ = 33 Ω         C$_{(NR)}$ = 470 nF         C$_{(BYPASS)}$ = 470 nF
C$_{(OUT)}$ = 10 μF         C$_{(IN)}$ = 10 μF

(1) The internal reference requires approximately 80 ms of rampup time (see Startup) from the enable event; therefore, V$_O$ fully reaches the target output voltage of 3.3 V in 80 ms from startup.

**Figure 43. Power-Up and Power-Down Response**

# 10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.2 V and 6.5 V. The input voltage range should provide adequate headroom in order for the device to have a regulated output. This input supply should be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

# 11 Layout

## 11.1 Layout Guidelines

### 11.1.1 Board Layout Recommendations To Improve PSRR And Noise Performance

To improve AC performance such as PSRR, output noise, and transient response, designing with separate ground planes for $V_I$ and $V_O$, with each ground plane connected only at the GND pin of the device, is recommended. In addition, the ground connection for the noise-reduction capacitor should connect directly to the GND pin of the device.

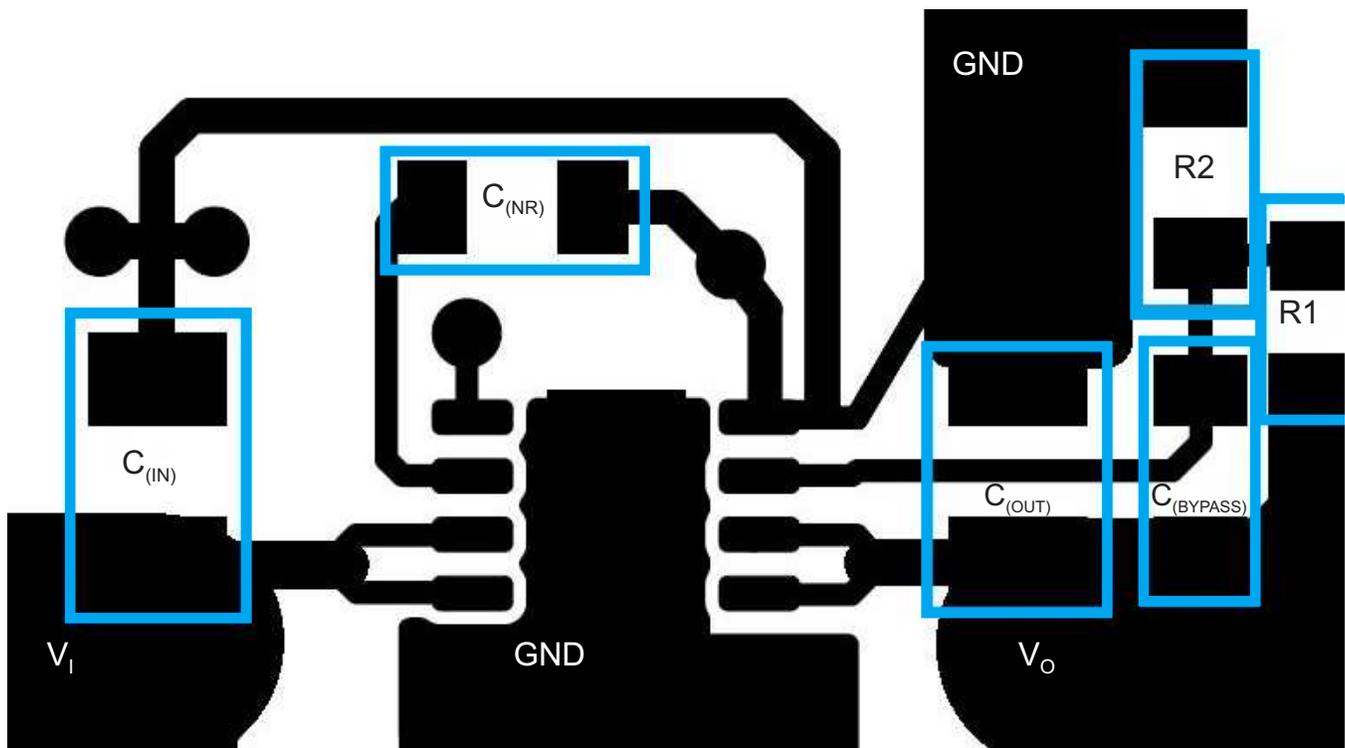High ESR capacitors may degrade PSRR.

## 11.2 Layout Example



**Figure 44. TPS7A8101-Q1 Layout Example**

## 11.3 Thermal Information

### 11.3.1 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage because of overheating.

Any activation of the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C (maximum). To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A8101-Q1 device has been designed to protect against overload conditions. The internal thermal protection circuitry was not intended to replace proper heatsinking. Continuously running the TPS7A8101-Q1 device into thermal shutdown degrades device reliability.

### 11.3.2 Package Mounting

See the Mechanical, Packaging, and Orderable Information section for solder pad footprint recommendations and recommended land patterns.

### 11.3.3 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the tab or pad is critical to avoiding thermal shutdown and ensuring reliable operation.

The power dissipation of the device depends on input voltage and load conditions. To calculate the device power dissipation, use Equation 3.

$$P_D = (V_I - V_O) \times I_O \tag{3}$$

Using the lowest possible input voltage necessary to achieve the required output voltage regulation minimizes power dissipation and achieves greater efficiency.

On the SON (DRB) package, the primary conduction path for heat is through the exposed pad to the printed circuit board (PCB). The pad can be connected to ground or can be left floating; however, the pad should be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device. Calculate the maximum junction-to-ambient thermal resistance using Equation 4.

$$R_{\theta JA} = \frac{(125°C - T_A)}{P_D} \tag{4}$$

Once the maximum $R_{\theta JA}$ value is calculated, use Figure 45 to estimate the minimum amount of PCB copper area needed for appropriate heatsinking.

## Thermal Information (continued)
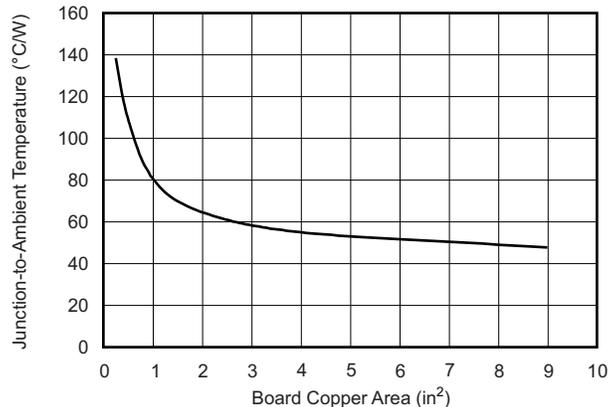


Note:    The $R_{\theta JA}$ value at board size of 9 in² (that is, 3 in × 3 in) is a JEDEC standard.

**Figure 45. $R_{\theta JA}$ vs Board Size**

Figure 45 shows the variation of $R_{\theta JA}$ as a function of ground plane copper area in the board. Figure 45 is intended as a guideline only to demonstrate the effects of heat spreading in the ground plane and should not be used to estimate actual thermal performance in real application environments.

> **NOTE**
>
> When the device is mounted on an application PCB, using $\Psi_{JT}$ and $\Psi_{JB}$, as explained in the section is strongly recommended.

### 11.3.4  Estimating Junction Temperature

Using the thermal metrics $\Psi_{JT}$ and $\Psi_{JB}$, as shown in the *Thermal Information* table, the junction temperature can be estimated with the corresponding equations, Equation 5 and Equation 6. For backwards compatibility, an older $\theta_{JC},Top$ parameter is listed as well.

$$\varphi_{JT}: T_J = T_T + \varphi_{JT} \times P_D$$

where

- $P_D$ is the power dissipation (see Equation 4)
- $T_T$ is the temperature at the center-top of the IC package                                    (5)

$$\varphi_{JB}: T_J = T_B + \varphi_{JB} \times P_D$$

where

- $T_B$ is the PCB temperature measured 1-mm away from the IC package *on the PCB surface* as shown in Figure 46                                                                                       (6)
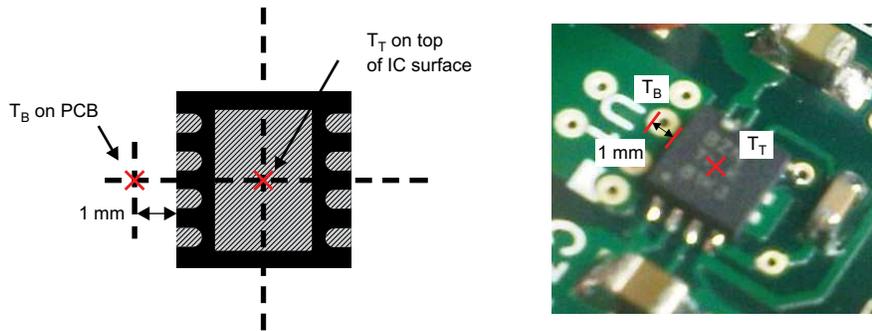
## Thermal Information (continued)



**Figure 46. Measuring Points for $T_T$ and $T_B$**

**NOTE**

Both $T_T$ and $T_B$ can be measured on actual application boards using an infrared thermometer.

For more information about measuring $T_T$ and $T_B$, see TI's application report SBVA025, *Using New Thermal Metrics*.

As shown in Figure 47, the new thermal metrics ($\Psi_{JT}$ and $\Psi_{JB}$) have very little dependency on board size. That is, using $\Psi_{JT}$ or $\Psi_{JB}$ with Equation 5 is a good way to estimate $T_J$ by simply measuring $T_T$ or $T_B$, regardless of the application board size.
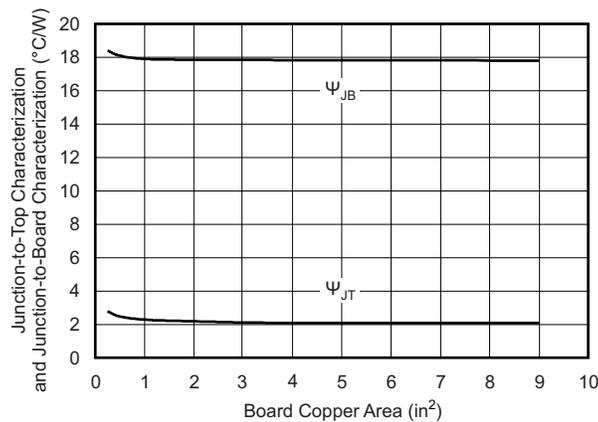


**Figure 47. $\Psi_{JT}$ and $\Psi_{JB}$ vs Board Size**

For a more detailed discussion of why TI does not recommend using $R_{\theta JC(top)}$ to determine thermal characteristics, refer to TI's application report SBVA025, *Using New Thermal Metrics.* For further information, refer to TI's application report SPRA953, *IC Package Thermal Metrics.*

# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation see the following:
- *LDO noise examined in detail*, SLYT489
- *LDO Performance Near Dropout*, SBVA029
- *TPS7A8101EVM Evaluation Module*, SLVU600
- *Wide Bandwidth PSRR of LDOs* by Nogawa and Van Renterghem in *Bodo's Power Systems®: Electronics in Motion and Conversion*, March 2011

## 12.2 Trademarks

Bodo's Power Systems is a registered trademark of Arlt Bodo.
All other trademarks are the property of their respective owners.

## 12.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS7A8101QDRBRQ1 | ACTIVE | SON | DRB | 8 | 3000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | SLY | Samples |

**(1)** The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPS7A8101-Q1 :**

● Catalog: TPS7A8101

NOTE: Qualified Version Definitions:

   ● Catalog - TI's standard catalog product

# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



| A0 | Dimension designed to accommodate the component width |
|----|---|
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS7A8101QDRBRQ1 | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

![TEXAS INSTRUMENTS]

# PACKAGE MATERIALS INFORMATION

**TAPE AND REEL BOX DIMENSIONS**
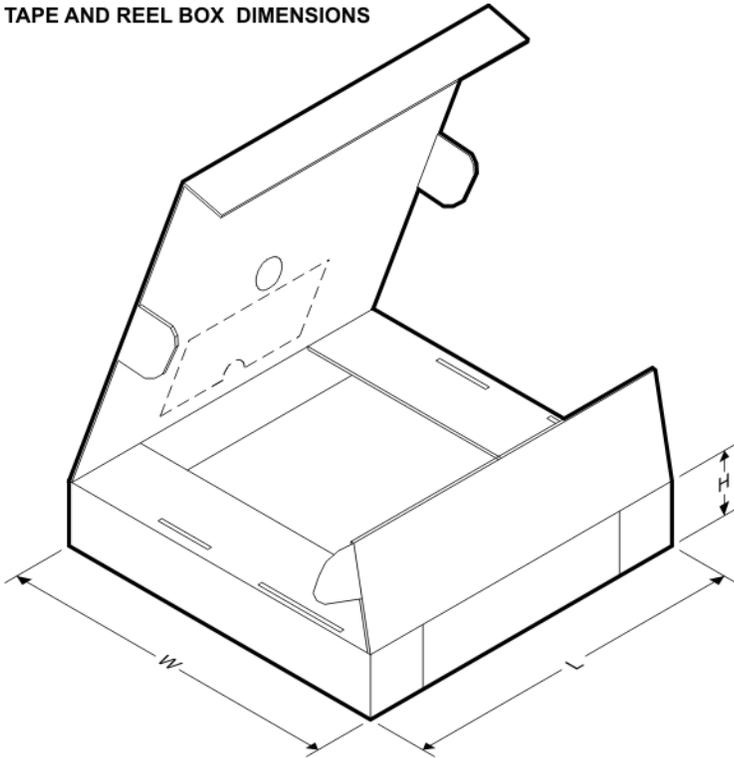


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS7A8101QDRBRQ1 | SON | DRB | 8 | 3000 | 367.0 | 367.0 | 35.0 |
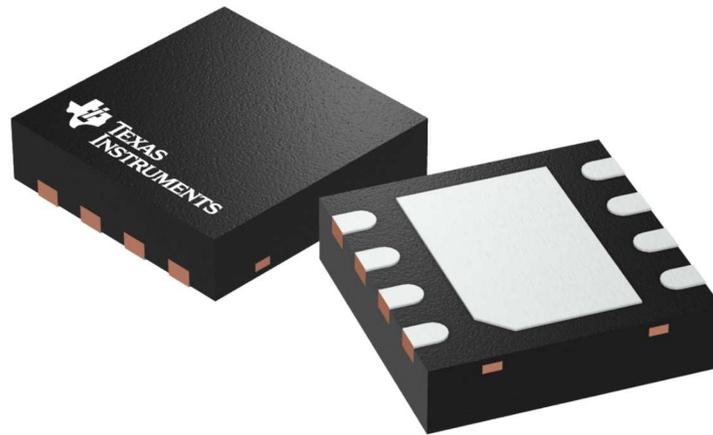
Images above are just a representation of the package family, actual package may vary.
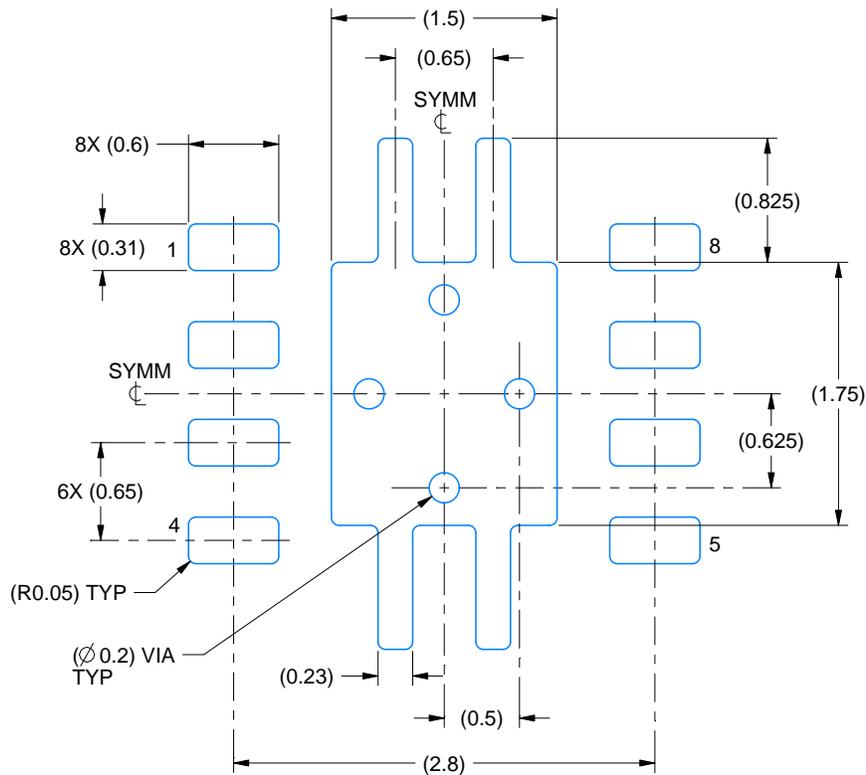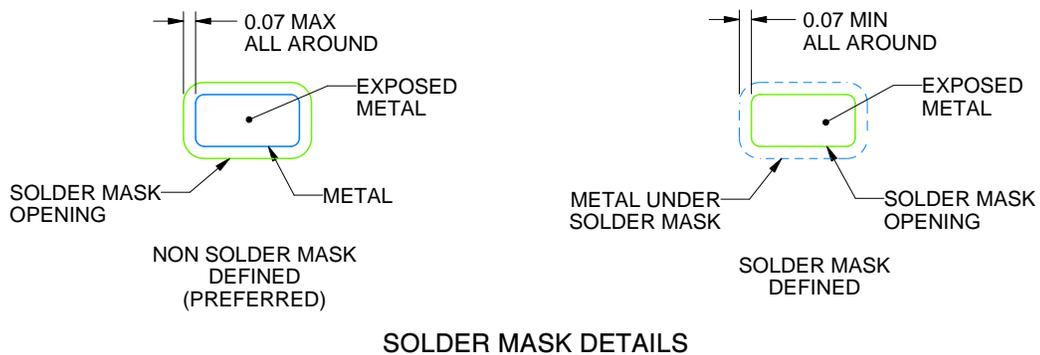Refer to the product data sheet for package details.

4203482/L

A
3.1
2.9
B

PIN 1 INDEX AREA

3.1
2.9

1 MAX

0.05
0.00

C

SEATING PLANE

⌒ 0.08 C

| DIM A | |
|---|---|
| OPT 1 | OPT 2 |
| (0.1) | (0.2) |

1.5±0.1

4X (0.23)

EXPOSED
THERMAL PAD

(DIM A) TYP

4

5

2X
1.95

1.75±0.1

1

8

6X 0.65

PIN 1 ID
(OPTIONAL)

(0.65)

8X 0.37
0.25

⊕ 0.1 Ⓜ C A B
0.05 Ⓜ C

8X 0.5
0.3

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

## DRB0008A

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

8X (0.6)

8X (0.31)

6X (0.65)

(R0.05) TYP

($\varnothing$ 0.2) VIA
TYP

(1.5)

(0.65)
SYMM

(0.825)

(1.75)

(0.625)

SYMM

(0.23)

(0.5)

(2.8)

0.07 MAX
ALL AROUND

EXPOSED
METAL

SOLDER MASK
OPENING

METAL

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

EXPOSED
METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

## DRB0008A

4X (0.23)

(0.65)

SYMM

8X (0.6)

4X (0.725)

METAL TYP

8X (0.31)    1

8

SYMM

(2.674)

(1.55)

6X (0.65)

4

5

(R0.05) TYP

(1.34)

(2.8)
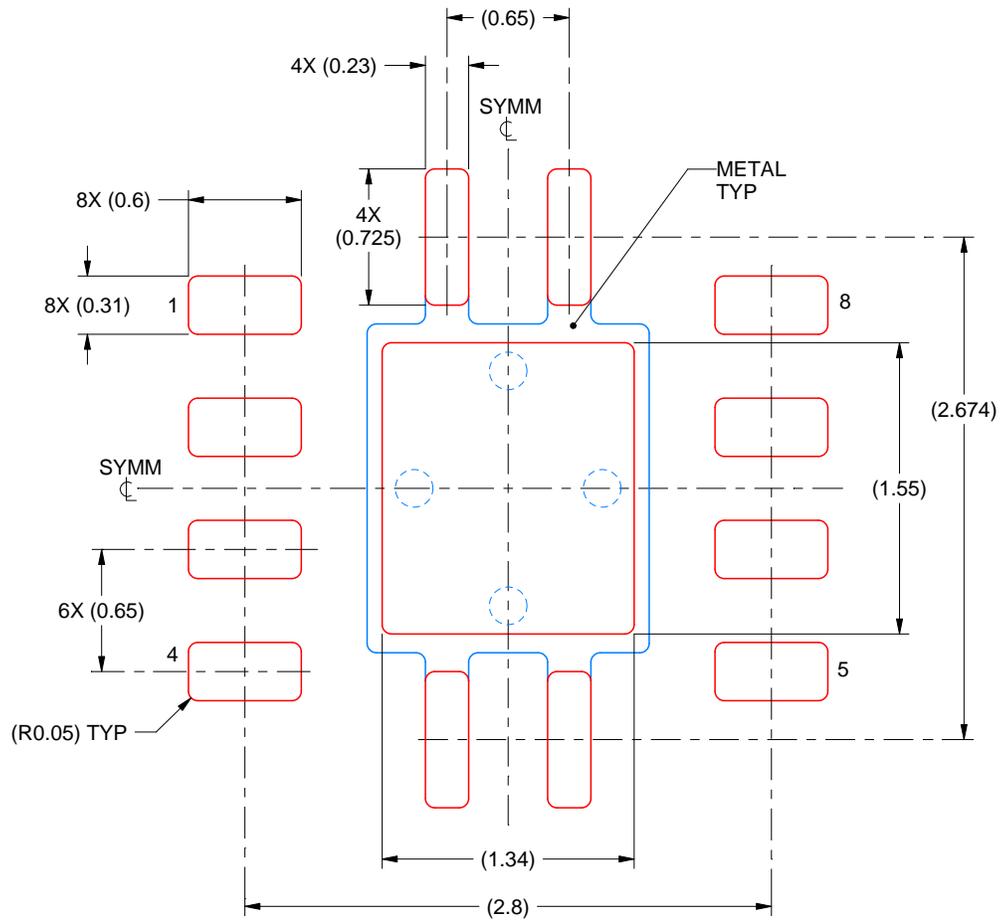
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.